DATA BOOK

NONVOLATILE DATA MEMORY

FPGA CONFIGURATION MEMORIES

PARALLEL EEPROM

SERIAL EEPROM

DATAFLASH®

905.670.5946
Fax 905.670.5947

ALL AMERICAN®

ISO 9002 CERTIFIED
Miami & Fremont Facilities

a leader in distribution technology

6375 Dixie Rd. North, Units 4-5-6
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ATMEL®

DECEMBER 1998

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Atmel Corporation
Nonvolatile Data Memory
Data Book
December 1998

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Parallel EEPROM
DataFlash®
FPGA Configuration Memories

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Nonvolatile Memory Overview

With the nonvolatile memories available from Atmel, you are given the ability to program devices late in a system's development cycle, or even after the system is complete. This feature gives you the flexibility for meeting changing market conditions. The principle products of nonvolatile memory are EPROMs (erasable programmable read-only memories), EEPROMs (electronically erasable programmable read-only memories) and Flash devices.

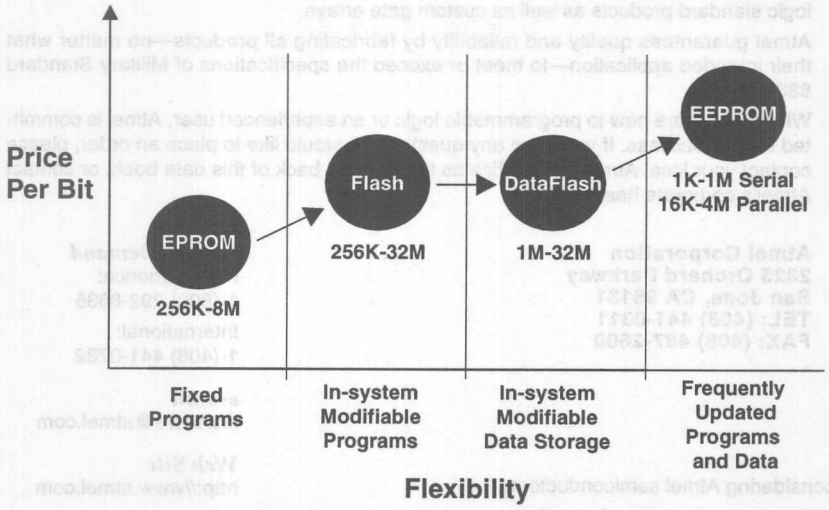
DataFlash®

The DataFlash product line represents one of the newest innovations in nonvolatile memory from Atmel. Arising out of a need for memory devices that fit between the requirements of serial-interface EEPROMs and standard Flash memories, Atmel began shipping DataFlash products in April 1997 and is already establishing market leadership. DataFlash products were designed to easily and efficiently handle large amounts of frequently changing data, ideally addressing the needs of digital voice storage, digital image storage, and text/data storage applications such as digital answering machines, cellular phones, fax machines, digital cameras and computer peripherals.

To minimize cost, DataFlash products utilize Atmel's latest EPROM-based Flash technology for the core memory array combined with a simple, easy-to-use interface (most devices incorporate an SPI interface like that used on serial-interface EEPROMs). Other unique features of the DataFlash include an extremely small-sectored Flash memory array, on-chip SRAM buffers that allow true EEPROM emulation, built-in error detection logic, hardware-controlled write protection, and single-cycle programming that doesn't require a separate erase command. Available in both 5.0-volt only and 2.7-volt only versions, Atmel offers DataFlash in densities ranging from 1 megabit to 32 megabits.

EPROMs

Atmel is a leading supplier of high-speed and low-voltage EPROMs and is recognized as the second largest worldwide supplier. EPROMs, the lowest cost user-programmable nonvolatile memory, can be programmed electrically in a programmer or its current system. These devices are used for program storage in computer and communications equipment, such as cellular phones, pagers, modems, and other computer peripherals. Atmel's EPROMs are manufactured in 2.7V, 3.0V, and 5.0V versions with capacities up to 8M bits and access times as fast as 45 ns.



Flash Memory

Known as the major volume supplier of 2.7V read and write Flash memories, Atmel leads the industry as one of the top three Flash makers in the world. Flash memories combine the electrically erasable flexibility of EEPROMs with the higher density and lower cost-per-bit of EPROMs—representing the fastest growing product sector in the semiconductor industry. What distinguishes Atmel's Flash products from its competitors is its use of a single low-voltage power source, for write and read functions. Atmel's Flash devices are used primarily to store operating programs in telecommunications, graphics, networking systems, and home video game systems. With Atmel's 2.7V low-voltage devices, you can extend battery life or reduce the number of batteries necessary for portable systems such as cellular telephones, pagers, laptop and palmtop devices.

Parallel EEPROMs

Since 1991 Atmel has been the world's largest supplier of these in-system, reprogrammable nonvolatile memories. EEPROMs' are distinguished as Parallel- or Serial-interface through their connection to the system's microcontroller or microprocessor. Atmel offers the industry's most complex full-featured Parallel EEPROM, the world's first single-chip 4M bit monolithic EEPROM, which is used extensively in many military and commercial avionics applications. Atmel produces the industry's only complete line of standard-voltage and battery-voltage Parallel devices that serve the growing portable equipment market. Parallel EEPROM leadership; first to market with battery-voltage devices and first to market with the largest density devices.

Serial EEPROMs

Serial-interface EEPROMs are used in a broad spectrum of consumer, telecommunication and automotive products, primarily for recording and holding personal preference data, such as programmable radio stations, seat comfort controls, autodial in telephones and program memory in camcorders. Key to Atmel's success in Serials is its 1.8V low-voltage family. Atmel is the only manufacturer to offer all Serial devices available in today's market.

Atmel Corporation designs, manufactures, and markets high-quality and high-performance CMOS memory, logic and analog integrated circuits. Founded in 1984, the Company serves the manufacturers of computation, communications and instrumentation equipment in commercial, industrial and military environments.

Atmel's broad line of products provide customers with a variety of solutions to their memory and logic applications. Atmel offers high-density, high-speed memory and logic standard products as well as custom gate arrays.

Atmel guarantees quality and reliability by fabricating all products—no matter what their intended application—to meet or exceed the specifications of Military Standard 883.

Whether you are new to programmable logic or an experienced user, Atmel is committed to your success. If you have any questions or would like to place an order, please contact your local Atmel sales office as listed in the back of this data book, or contact Atmel's corporate headquarters:

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1-(408) 436-4309

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ATMEL

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Explanation of Atmel's Part Number Code

All Atmel part numbers begin with the prefix "AT". The next four to nine digits are the part number. In addition, Atmel parts can be ordered in particular speeds, in specific packages, for particular temperature ranges and with the option of 883C level B military compliance. The available options for each part are listed at the back of its data sheet in its "Ordering Information" table. These options are designated by the following suffixes placed at the end of the Atmel part number, in the order given:

Prefix	Device-	Suffix
AT	XXXXX	X X X X

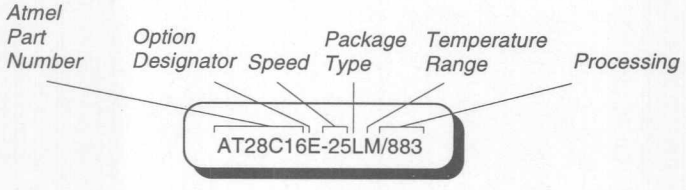
Processing
- Blank = Standard
- /883 = MIL-STD-883, Class B Fully Compliant
- B = MIL-STD-883, Class B Non-Compliant

Temperature Range
- C = Com Temp (0°C to 70°C)
- I = Ind Temp (-40°C to 85°C)
- M = Mil Temp (-55°C to 125°C)

Package
- A = TQFP
- B = Ceramic Side Braze Dual Inline
- C = CBGA
- D = Cerdip
- F = Flatpack
- G = Cerdip, One Time Programmable
- J = Plastic J-Lead Chip Carrier
- K = Ceramic J-Lead Chip Carrier
- L = Leadless Chip Carrier
- M = MSOP
- N = Leadless Chip Carrier, One Time Programmable
- P = Plastic DIP
- Q = Plastic Quad Flatpack
- R = SOIC
- S = SOIC
- T = TSOP (TSSOP for Serial EEPROM)
- U = µBGA
- V = VSOP (Small TSOP)
- W = Die
- X = TSSOP
- Y = Cerpack
- Z = Ceramic Multi-Chip Module

Speed

Here is an example Atmel part number:



Rev. 0538B–10/98

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AT93C57	256 x 8 or 128 x 16	3-Wire, 2K-bit Serial EEPROM	2-121
AT93C66	512 x 8 or 256 x 16	3-Wire, 4K-bit Serial EEPROM	2-121
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AT93C46C	64 x 16	3-Wire, 1K-bit Serial EEPROM	2-145
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AT59C13	512 x 8 or 256 x 16	4-Wire, 4K-bit Serial EEPROM	2-155
AT25010	128 x 8	SPI, 1K-bit Serial EEPROM	2-167
AT25020	256 x 8	SPI, 2K-bit Serial EEPROM	2-167
AT25040	512 x 8	SPI, 4K-bit Serial EEPROM	2-167
AT25080	1024 x 8	SPI, 8K-bit Serial EEPROM	2-181
AT25160	2048 x 8	SPI, 16K-bit Serial EEPROM	2-181
AT25320	4096 x 8	SPI, 32K-bit Serial EEPROM	2-181
AT25640	8192 x 8	SPI, 64K-bit Serial EEPROM	2-181
AT25128	16,384 x 8	SPI, 128K-bit Serial EEPROM	2-197
AT25256	32,768 x 8	SPI, 256K-bit Serial EEPROM	2-197
AT25HP256	32,768 x 8	SPI, 256K-bit Serial EEPROM	2-213
AT25HP512	65,536 x 8	SPI, 512K-bit Serial EEPROM	2-213
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2-Wire Serial EEPROM

1K (128 x 8)

AT24C01

Features

- **Low Voltage and Standard Voltage Operation**
  - **5.0 (V_{CC} = 4.5V to 5.5V)**
  - **2.7 (V_{CC} = 2.7V to 5.5V)**
  - **2.5 (V_{CC} = 2.5V to 5.5V)**
  - **1.8 (V_{CC} = 1.8V to 5.5V)**
- **Internally Organized 128 x 8**
- **2-Wire Serial Interface**
- **Bidirectional Data Transfer Protocol**
- **100 kHz (1.8V, 2.5V, 2.7V) and 400 kHz (5V) Compatibility**
- **4-Byte Page Write Mode**
- **Self-Timed Write Cycle (10 ms max)**
- **High Reliability**
  - **Endurance: 1 Million Write Cycles**
  - **Data Retention: 100 Years**
  - **ESD Protection: >3000V**
- **Automotive Grade and Extended Temperature Devices Available**
- **8-Pin PDIP, 8-Pin MSOP, 8-Pin TSSOP and 8-Pin JEDEC SOIC Packages**

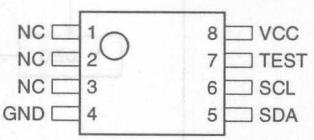
Description

The AT24C01 provides 1024 bits of serial electrically erasable and programmable read only memory (EEPROM) organized as 128 words of 8 bits each. The device is optimized for use in many industrial and commercial applications where low power and low voltage operation are essential. The AT24C01 is available in space saving 8-pin PDIP, 8-pin MSOP, 8-pin TSSOP, and 8-pin JEDEC SOIC packages and is accessed via a 2-wire serial interface. In addition, the entire family is available in 5.0V (4.5V to 5.5V), 2.7V (2.7V to 5.5V), 2.5V (2.5V to 5.5V) and 1.8V (1.8V to 5.5V) versions.

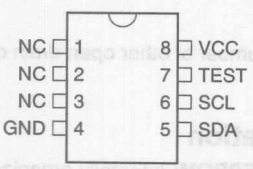
Pin Configurations

Pin Name	Function
NC	No Connect
SDA	Serial Data
SCL	Serial Clock Input
TEST	Test Input (GND or VCC)

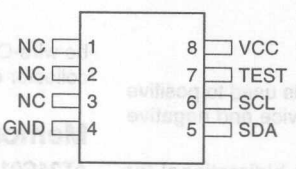
8-Pin MSOP
8-Pin TSSOP



8-Pin PDIP



8-Pin SOIC



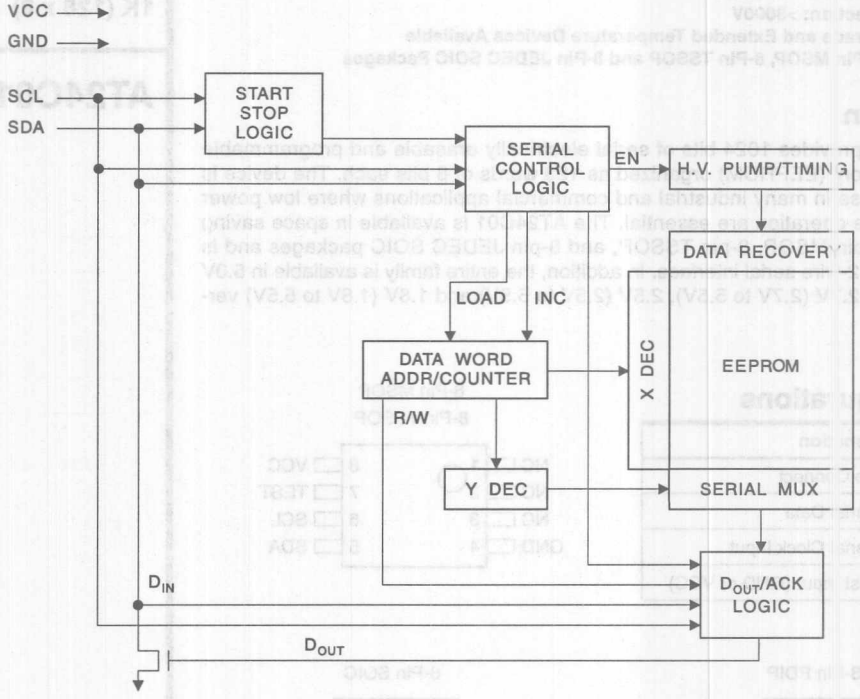
Rev. 0134C–07/98

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Block Diagram



Pin Description

SERIAL CLOCK (SCL): The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

SERIAL DATA (SDA): The SDA pin is bidirectional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open collector devices.

Memory Organization

AT24C01, 1K SERIAL EEPROM: Internally organized with 128 pages of 1 byte each. The 1K requires a 7-bit data word address for random word addressing.

Pin Capacitance

Applicable over recommended operating range from T_A = 25°C, f = 1.0 MHz, V_{CC} = +1.8V.

Symbol	Test Condition	Max	Units	Condition
$C_{I/O}$	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}	Input Capacitance (A0, A1, A2, SCL)	6	pF	V_{IN} = 0V

DC Characteristics

Applicable over recommended operating range from: T_{AI} = -40°C to +85°C, V_{CC} = +1.8V to +5.5V, T_{AC} = 0°C to +70°C, V_{CC} = +1.8V to +5.5V (unless otherwise noted).

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V_{CC1}	Supply Voltage		1.8		5.5	V
V_{CC2}	Supply Voltage		2.5		5.5	V
V_{CC3}	Supply Voltage		2.7		5.5	V
V_{CC4}	Supply Voltage		4.5		5.5	V
I_{CC}	Supply Current V_{CC} = 5.0V	READ at 100 kHz		0.4	1.0	mA
I_{CC}	Supply Current V_{CC} = 5.0V	WRITE at 100 kHz		2.0	3.0	mA
I_{SB1}	Standby Current V_{CC} = 1.8V	V_{IN} = V_{CC} or V_{SS}		0.6	3.0	µA
I_{SB2}	Standby Current V_{CC} = 2.5V	V_{IN} = V_{CC} or V_{SS}		1.4	4.0	µA
I_{SB3}	Standby Current V_{CC} = 2.7V	V_{IN} = V_{CC} or V_{SS}		1.6	4.0	µA
I_{SB4}	Standby Current V_{CC} = 5.0V	V_{IN} = V_{CC} or V_{SS}		8.0	18.0	µA
I_{LI}	Input Leakage Current	V_{IN} = V_{CC} or V_{SS}		0.10	3.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{CC} or V_{SS}		0.05	3.0	µA
V_{IL}	Input Low Level[1]		-0.6		V_{CC} × 0.3	V
V_{IH}	Input High Level[1]		V_{CC} × 0.7		V_{CC} + 0.5	V
V_{OL2}	Output Low Level V_{CC} = 3.0V	I_{OL} = 2.1 mA			0.4	V
V_{OL1}	Output Low Level V_{CC} = 1.8V	I_{OL} = 0.15 mA			0.2	V

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

AC Characteristics

Applicable over recommended operating range from T_A = -40°C to +85°C, V_{CC} = +1.8V to +5.5V, CL = 1 TTL Gate and 100 pF (unless otherwise noted).

Symbol	Parameter	2.7-, 2.5-, 1.8-volt		5.0-volt		Units
		Min	Max	Min	Max	
f_{SCL}	Clock Frequency, SCL		100		400	kHz
t_{LOW}	Clock Pulse Width Low	4.7		1.2		µs
t_{HIGH}	Clock Pulse Width High	4.0		0.6		µs
t_I	Noise Suppression Time(1)		100		50	ns
t_{AA}	Clock Low to Data Out Valid	0.1	4.5	0.1	0.9	µs
t_{BUF}	Time the bus must be free before a new transmission can start(1)	4.7		1.2		µs
$t_{HD.STA}$	Start Hold Time	4.0		0.6		µs
$t_{SU.STA}$	Start Set-up Time	4.7		0.6		µs
$t_{HD.DAT}$	Data In Hold Time	0		0		µs
$t_{SU.DAT}$	Data In Set-up Time	200		100		ns
t_R	Inputs Rise Time(1)		1.0		0.3	µs
t_F	Inputs Fall Time(1)		300		300	ns
$t_{SU.STO}$	Stop Set-up Time	4.7		0.6		µs
t_{DH}	Data Out Hold Time	100		50		ns
t_{WR}	Write Cycle Time		10		10	ms
Endurance(1)	5.0V, 25°C, Page Mode	1M		1M		Write Cycles

Note: 1. This parameter is characterized and is not 100% tested.

Device Operation

CLOCK and DATA TRANSITIONS: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (refer to Data Validity timing diagram). Data changes during SCL high periods will indicate a start or stop condition as defined below.

START CONDITION: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (refer to Start and Stop Definition timing diagram).

STOP CONDITION: A low-to-high transition of SDA with SCL high is a stop condition which terminates all communications. After a read sequence, the stop command will place the EEPROM in a standby power mode (refer to Start and Stop Definition timing diagram).

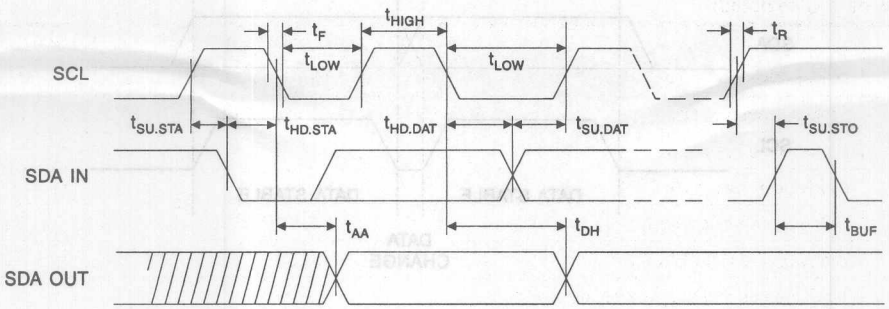
ACKNOWLEDGE: All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. Any device on the system bus receiving data (when communicating with the EEPROM) must pull the SDA bus low to acknowledge that it has successfully received each word. This must happen during the ninth clock cycle after each word received and after all other system devices have freed the SDA bus. The EEPROM will likewise acknowledge by pulling SDA low after receiving each address or data word (refer to Acknowledge Response from Receiver timing diagram).

STANDBY MODE: The AT24C01 features a low power standby mode which is enabled: (a) upon power-up and (b) after the receipt of the STOP bit and the completion of any internal operations.

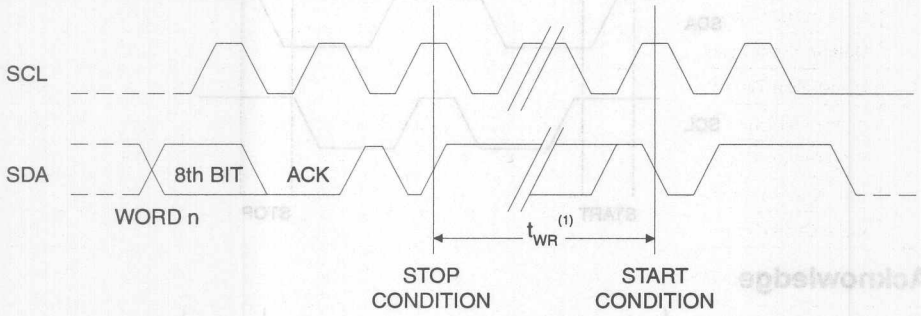
MEMORY RESET: After an interruption in protocol, power loss or system reset, any 2-wire part can be reset by following these steps:

(a) Clock up to 9 cycles, (b) look for SDA high in each cycle while SCL is high and then (c) create a start condition as SDA is high.

Bus Timing
SCL: Serial Clock, SDA: Serial Data I/O

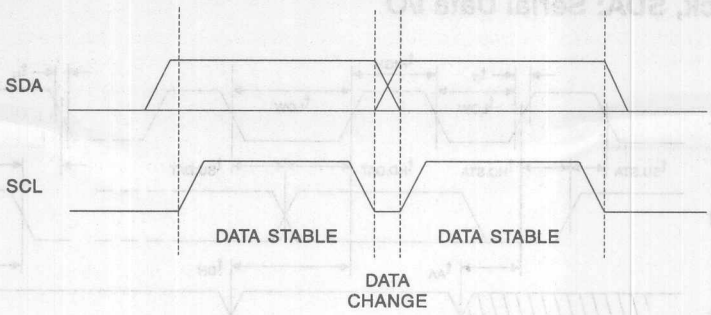


Write Cycle Timing
SCL: Serial Clock, SDA: Serial Data I/O

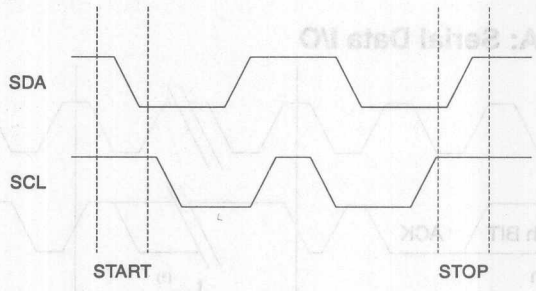


Note: 1. The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

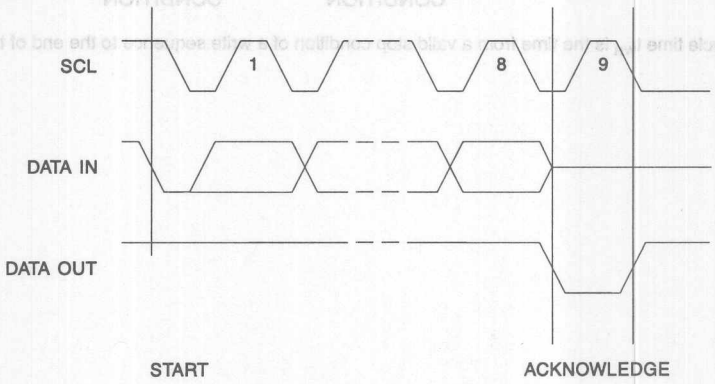
Data Validity



Start and Stop Definition



Output Acknowledge



Write Operations

BYTE WRITE: Following a start condition, a write operation requires a 7-bit data word address and a low write bit. Upon receipt of this address, the EEPROM will again respond with a zero and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a zero and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally-timed write cycle to the nonvolatile memory. All inputs are disabled during this write cycle , t_{WR}, and the EEPROM will not respond until the write is complete (refer to Figure 1).

PAGE WRITE: The AT24C01 is capable of a 4-byte page write.

A page write is initiated the same as a byte write but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to three more data words. The EEPROM will respond with a zero after each data word received. The microcontroller must terminate the page write sequence with a stop condition (refer to Figure 2).

The data word address lower 2 bits are internally incremented following the receipt of each data word. The higher five data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than four data words are transmitted to the EEPROM, the data word address will "roll over" and previous data will be overwritten.

ACKNOWLEDGE POLLING: Once the internally-timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a zero allowing the read or write sequence to continue.

Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to one. There are two read operations: byte read and sequential read.

BYTE READ: A byte read is initiated with a start condition followed by a 7-bit data word address and a high read bit. The AT24C01 will respond with an acknowledge and then serially output 8 data bits. The microcontroller does not respond with a zero but does generate a following stop condition (refer to Figure 3).

SEQUENTIAL READ: Sequential reads are initiated the same as a byte read. After the microcontroller receives an 8-bit data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will "roll over" and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with an input zero but does generate a following stop condition (refer to Figure 4).

Figure 1. Byte Write

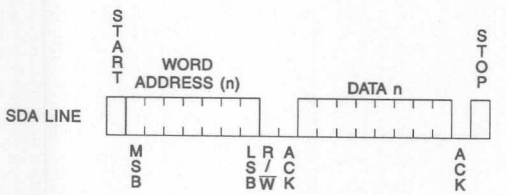


Figure 2. Page Write

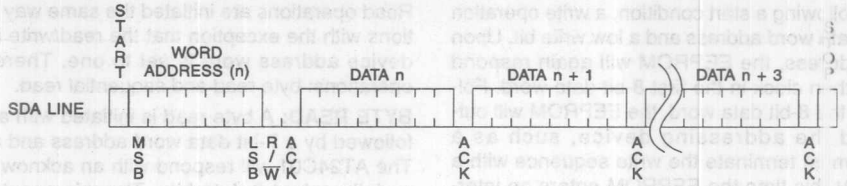


Figure 3. Byte Read

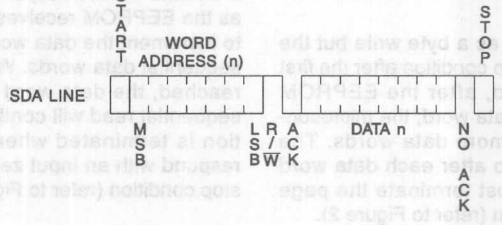
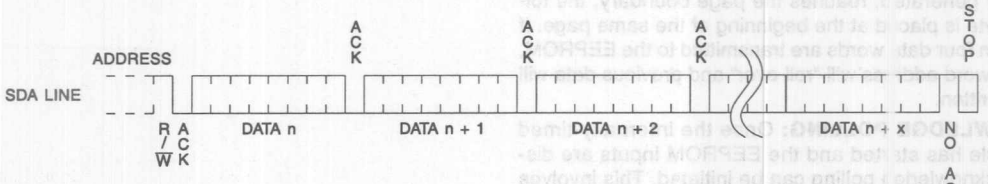


Figure 4. Sequential Read



Ordering Information

t_{WR} (max) (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	3000	18	400	AT24C01-10PC AT24C01-10SC AT24C01-10MC AT24C01-10TC	8P3 8S1 8M 8T	Commercial (0°C to 70°C)
	3000	18	400	AT24C01-10PI AT24C01-10SI AT24C01-10MI AT24C01-10TI	8P3 8S1 8M 8T	Industrial (-40°C to 85°C)
10	1500	4	100	AT24C01-10PC-2.7 AT24C01-10SC-2.7 AT24C01-10MC-2.7 AT24C01-10TC-2.7	8P3 8S1 8M 8T	Commercial (0°C to 70°C)
	1500	4	100	AT24C01-10PI-2.7 AT24C01-10SI-2.7 AT24C01-10MI-2.7 AT24C01-10TI-2.7	8P3 8S1 8M 8T	Industrial (-40°C to 85°C)
10	1000	4	100	AT24C01-10PC-2.5 AT24C01-10SC-2.5 AT24C01-10MC-2.5 AT24C01-10TC-2.5	8P3 8S1 8M 8T	Commercial (0°C to 70°C)
	1000	4	100	AT24C01-10PI-2.5 AT24C01-10SI-2.5 AT24C01-10MI-2.5 AT24C01-10TI-2.5	8P3 8S1 8M 8T	Industrial (-40°C to 85°C)
10	800	3	100	AT24C01-10PC-1.8 AT24C01-10SC-1.8 AT24C01-10MC-1.8 AT24C01-10TC-1.8	8P3 8S1 8M 8T	Commercial (0°C to 70°C)
	800	3	100	AT24C01-10PI-1.8 AT24C01-10SI-1.8 AT24C01-10MI-1.8 AT24C01-10TI-1.8	8P3 8S1 8M 8T	Industrial (-40°C to 85°C)

Package Type	
8M	8-Lead, 0.118" Wide, Miniature Small Outline Package (MSOP)
8P3	8-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8T	8-Lead, 0.170" Wide, Thin Shrink Small Outline Package (TSSOP)
Options	
Blank	Standard Operation (4.5V to 5.5V)
-2.7	Low-Voltage (2.7V to 5.5V)
-2.5	Low-Voltage (2.5V to 5.5V)
-1.8	Low-Voltage (1.8V to 5.5V)

Features

- 2-Wire Serial Interface
- Schmitt Trigger, Filtered Inputs For Noise Suppression
- DDC1™/ DDC2™ Interface Compliant for Monitor Identification
- Low Voltage Operation
  - 2.5 (V_{CC} = 2.5V to 5.5V)
- Internally Organized 128 x 8
- 100 kHz (2.5V) Compatibility
- 8-Byte Page Write Mode
- Write Protection Available
- Self-timed Write Cycle (10 ms max)
- High Reliability
  - Endurance: 1 Million Write Cycles
  - Data Retention: 100 Years
  - ESD Protection: >3000V
- 8-Pin PDIP and JEDEC SOIC Packages

2-Wire Serial EEPROM

1K (128 x 8)

AT24C21

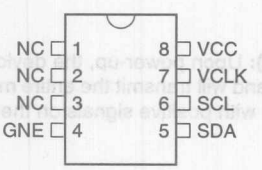
Description

The AT24C21 provides 1024 bits of serial electrically erasable and programmable read only memory (EEPROM) organized as 128 words of 8 bits each. The device is optimized for use in applications requiring data storage and serial transmission of configuration and control information. The AT24C21 features two modes of operation: Transmit-only Mode and Bidirectional Mode. Upon power-up, the AT24C21 will be in the Transmit-only Mode, sending a serial-bit stream of the entire memory contents, clocked via the VCLK pin. The Bidirectional Mode is selected by a valid high-to-low transition on the SCL pin and offers byte selectable read/write capability of the entire memory array. The AT24C21 is available in space saving 8-pin PDIP and 8-pin SOIC packages.

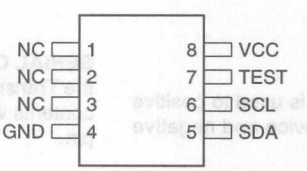
Pin Configurations

Pin Name	Function
NC	No Connect
SDA	Serial Data
SCL	Serial Clock Input (Bidirectional Mode)
VCLK	Serial Clock Input (Transmit-only Mode)

8-Pin PDIP



8-Pin SOIC



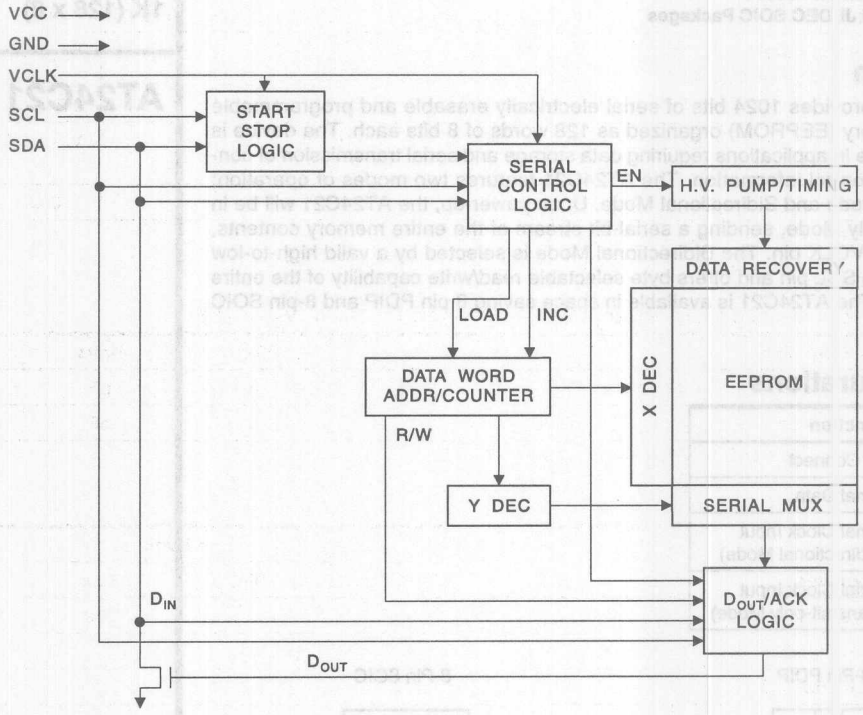
Rev. 0405E–07/98

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Block Diagram



Pin Description

SERIAL CLOCK (SCL): The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

SERIAL DATA (SDA): The SDA pin is bidirectional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open drain or open collector devices.

SERIAL CLOCK (VCLK): Upon power-up, the device is in the Transmit-only mode and will transmit the entire memory contents via the SDA pin with positive signals on the VCLK pin.

Memory Organization

AT24C21, 1K SERIAL EEPROM: Internally organized with 128 pages of one byte each. The 1K requires a 7-bit data word address for random word addressing.

DC Characteristics

Applicable over recommended operating range from: T_{AI} = -40°C to +85°C, T_{AC} = 0°C to +70°C, V_{CC} = +2.5 V to +5.5V (unless otherwise noted).

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V_{CC}	Supply Voltage		2.5		5.5	V
I_{CC}	Supply Current V_{CC} = 5.0V	READ at 100 kHz		0.4	1.0	mA
I_{CC}	Supply Current V_{CC} = 5.0V	WRITE at 100 kHz		2.0	3.0	mA
I_{SB}	Standby Current V_{CC} = 2.5V	$V_{IN} = V_{CC}$ or V_{SS}		3.0	4.0	µA
	V_{CC} = 5.0V	$V_{IN} = V_{CC}$ or V_{SS}		12.0	30.0	µA
I_{LI}	Input Leakage Current	$V_{IN} = V_{CC}$ or V_{SS}		0.10	1.0	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or V_{SS}		0.05	1.0	µA
V_{IL}	Input Low Level(1) SCL, SDA Pin		-0.6		$V_{CC} \times 0.3$	V
	Input Low Level VCLK Pin	$V_{CC} \geq 2.7V$			0.8	V
		$V_{CC} < 2.7V$			$0.2 \times V_{CC}$	V
V_{IH}	Input High Level(1) SCL, SDA Pin		$V_{CC} \times 0.7$		$V_{CC} + 0.5$	V
	Input High Level VCLK Pin		2.0			V
V_{OL}	Output Low Level V_{CC} = 3.0V	I_{OL} = 2.1 mA			0.40	V

Note: 1. V_{IL} min and V_{IH} max are for reference only and not tested.

Pin Capacitance(1)

Applicable over recommended operating range from T_A = 25°C, f = 1.0 MHz, V_{CC} = +1.8V.

Symbol	Test Condition	Max	Units	Conditions
$C_{I/O}$	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}	Input Capacitance (A_0, A_1, A_2, SCL, VCLK)	6	pF	V_{IN} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

Transmit-only Mode

		2.5-volt		
Symbol	Parameter	Min	Max	Units
T_{VAA}	Output Valid from VCLK		500	ns
T_{VHIGH}	VCLK High-time	4.0		µs
T_{VLOW}	VCLK Low-time	4.7		µs
T_{VHZ}	Mode Transition Time		500	ns
T_{VPU}	Transmit-only Power-up Time	0		ns

AC Characteristics

Applicable over recommended operating range from T_A = -40°C to +85°C, V_{CC} = +2.5V to +5.5V C_L = 1 TTL Gate and 100 pF (unless otherwise noted).

		2.5-volt		
Symbol	**Parameter**	**Min**	**Max**	**Units**
f_{SCL}	Clock Frequency, SCL	0	100	kHz
t_{LOW}	Clock Pulse Width Low	4.7		µs
t_{HIGH}	Clock Pulse Width High	4.0		µs
t_I	Noise Suppression Time(1) (SDA and SCL pins)		NA	ns
t_{AA}	Clock Low to Data Out Valid	0.1	3.5	µs
t_{BUF}	Time the bus must be free before a new transmission can start	4.7		µs
$t_{HD.STA}$	Start Hold Time	4.0		µs
$t_{SU.STA}$	Start Set-up Time	4.7		µs
$t_{HD.DAT}$	Data In Hold Time	0		µs
$t_{SU.DAT}$	Data In Set-up Time	250		ns
t_R	Inputs Rise Time(1)		1.0	µs
t_F	Inputs Fall Time(1)		300	ns
$t_{SU.STO}$	Stop Set-up Time	4.0		µs
t_{DH}	Data Out Hold Time	100		ns
t_{WR}	Write Cycle Time		10	ms
Endurance(1)	5.0V, 25°C, Page Mode	1M		Write Cycles

Note: 1. This parameter is characterized and is not 100% tested.

Functional Description

The AT24C21 has two modes of operation: the Transmit-only Mode and the Bidirectional Mode. There is a separate 2-wire protocol to support each mode, each having a separate clock input (SCL and VCLK) and both modes sharing a common Bidirectional data line (SDA). The AT24C21 enters the Transmit-only Mode upon powering up the device. In this mode, the device transmits data on the SDA pin upon a clock signal on the VCLK pin. The device will remain in the Transmit-only Mode until a valid high-to-low transition takes place on the SCL pin. The device will switch into the Bidirectional Mode when a valid transition on the SCL pin is recognized. Once the device has transitioned to the Bidirectional Mode, there is no way to return to the Transmit-only Mode, except to power down (reset) the device.

Transmit-only Mode (DDC1)

The AT24C21 will power up in the Transmit-only Mode. In this mode, the device will output one bit of data on the SDA pin on each rising edge on the VCLK pin. Data is transmitted in 8 bit words with the most significant bit first. Each word is followed by a 9th "don't care" bit which will be in high impedance state (refer to Figure 1). The AT24C21 will continuously cycle through the entire memory array in incremental sequence as long a VCLK is present and no falling edges on SCL are received. When the maximum address (7FH) is reached, the output will wrap around to the zero location (00H) and continue. The Bidirectional mode clock (SCL) pin must be held high for the device to remain in the Transmit-only mode.

Upon power-up, the AT24C21 will not output valid data until it has been initialized. During initialization, data will not be available until after the first nine clocks are sent to the device (refer to Figure 2). The starting address for the Transmit-only mode can be determined during initialization. If the SDA pin is held high during the first eight clocks (refer to Figure 2), the starting address will be 7FH. If the SDA pin is low during the first eight clocks, the starting address will be 00H. During the ninth clock, SDA should be in high impedance.

Figure 1. Transmit-only Mode

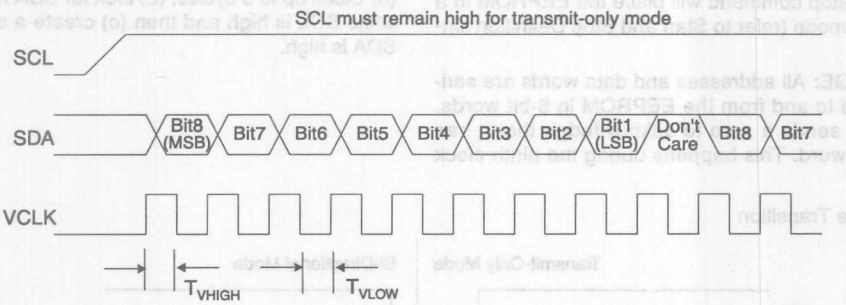
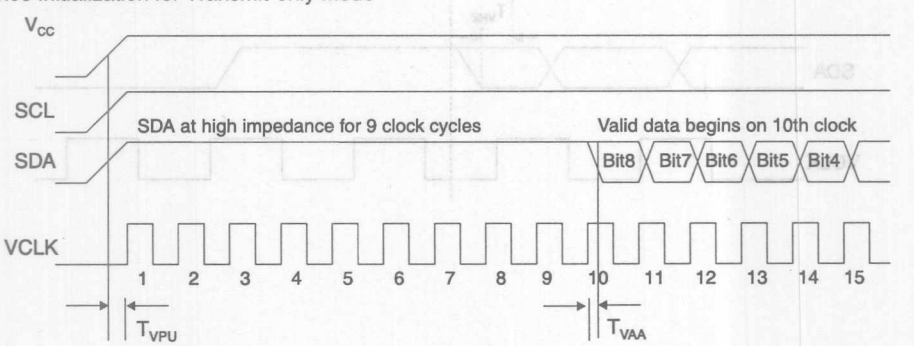


Figure 2. Device Initialization for Transmit-only Mode



Bidirectional Mode (DDC2)

This mode supports a 2-wire, Bidirectional data transmission protocol. The AT24C21 can be switched into the Bidirectional Mode by issuing a valid high to low transition on the SCL pin (refer to Figure 3). After the device is in the Bidirectional Mode, all inputs to the VCLK pin are ignored, except when a logic high is required to enable write capability. All byte and page writes and byte and sequential reads are supported in this mode.

Bidirectional Mode Operation

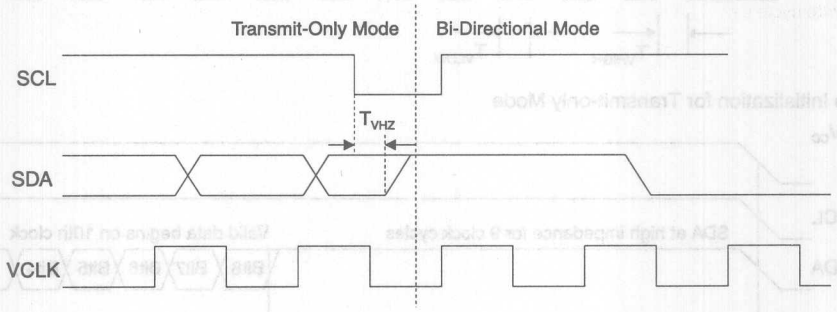
CLOCK and DATA TRANSITIONS: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (refer to Data Validity timing diagram). Data changes during SCL high periods will indicate a start or stop condition as defined below.

START CONDITION: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (refer to Start and Stop Definition timing diagram).

STOP CONDITION: A low-to-high transition of SDA with SCL high is a stop condition. After a read or write sequence, the stop command will place the EEPROM in a standby power mode (refer to Start and Stop Definition timing diagram).

ACKNOWLEDGE: All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a zero to acknowledge that it has received each word. This happens during the ninth clock cycle.

Figure 3. Mode Transition



Device Addressing

The AT24C21 requires an 8-bit device address word following a start condition to enable the chip for a read or write operation (refer to Figure 4).

The device address word consists of a mandatory one, zero sequence for the first four most significant bits as shown. This is common to all the EEPROM devices.

The next three bits are don't care for the AT24C21.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

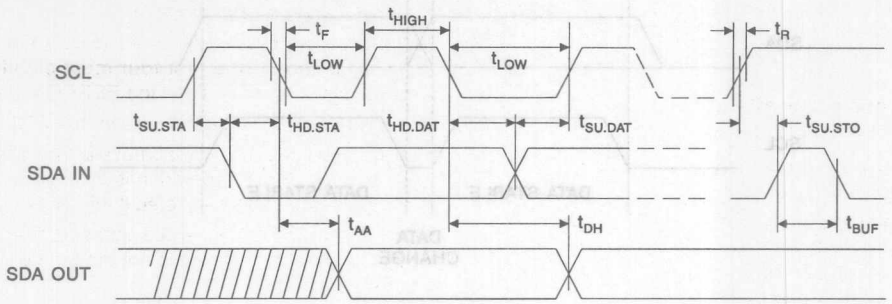
Upon a compare of the device address, the EEPROM will output a zero. If a compare is not made, the chip will return to a standby state.

STANDBY MODE: The AT24C21 features a low power standby mode which is enabled: (a) upon power-up and (b) after the receipt of the STOP bit and the completion of any internal operations.

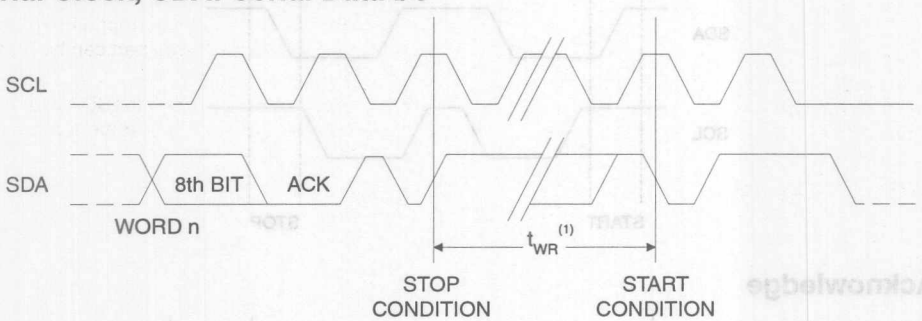
MEMORY RESET: After an interruption in protocol, power loss or system reset, any 2-wire part can be reset by following these steps:

(a) Clock up to 9 cycles, (b) look for SDA high in each cycle while SCL is high and then (c) create a start condition as SDA is high.

Bus Timing
SCL: Serial Clock, SDA: Serial Data I/O

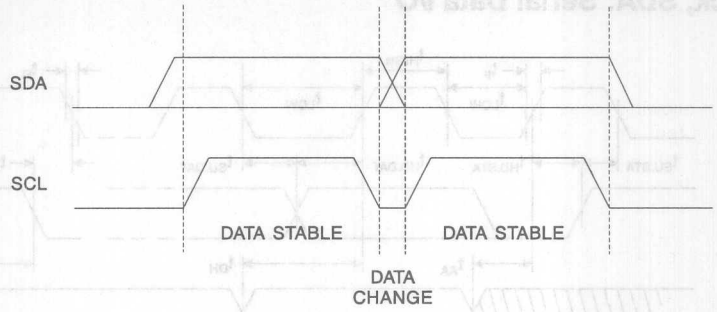


Write Cycle Timing
SCL: Serial Clock, SDA: Serial Data I/O

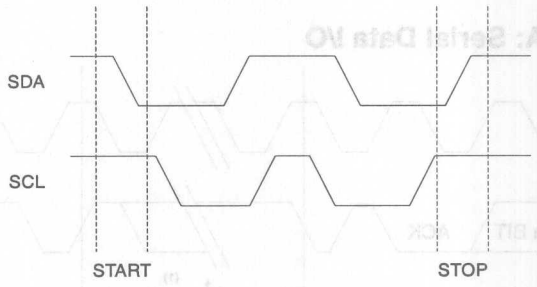


Note: 1. The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

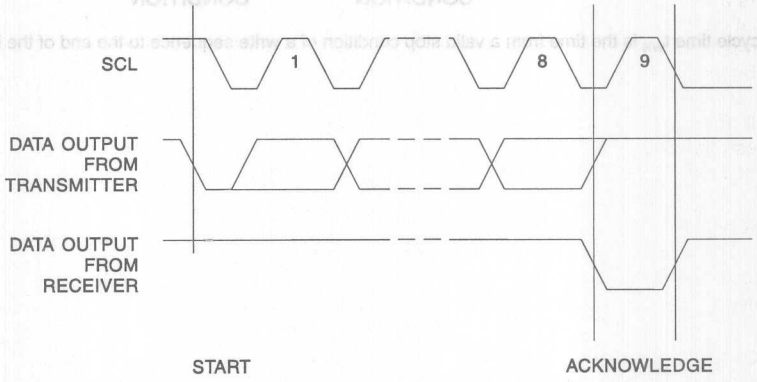
Data Validity



Start and Stop Definition



Output Acknowledge



Write Operations

BYTE WRITE: A write operation requires an 8-bit data word addresses following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a zero and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a zero and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally-timed write cycle , t_{WR}, to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (refer to Figure 5).

It is required that VCLK be held at a high logic level in order to program the device. This applies to byte write and page write operation. Note that VCLK can go low while the device is in its self-timed program operation and not affect programming.

PAGE WRITE: The AT24C21 is capable of an 8-byte page write.

A page write is initiated the same as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to seven more data words. The EEPROM will respond with a zero after each data word received. The microcontroller must terminate the page write sequence with a stop condition (refer to Figure 6).

The data word address lower three bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than eight data words are transmitted to the EEPROM, the data word address will "roll over" and previous data will be overwritten. The address "roll over" during write is from the last byte of the current page to the first byte of the same page.

It is required that VCLK be held at a high logic level in order to program the device. This applies to byte write and page write operation. Note that VCLK can go low while the device is in its self-timed program operation and not affect programming.

ACKNOWLEDGE POLLING: Once the internally-timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a zero allowing the read or write sequence to continue.

WRITE PROTECTION: When VCLK pin is connected to GND and in the Bidirectional Mode, the entire memory is protected and becomes ROM only. This protects the device memory from any inadvertent write operations.

NOISE PROTECTION: Special internal circuitry placed on the SDA and SCL pins prevent small noise spikes from activating the device. Furthermore, the AT24C21 employs a low V_{CC} detector circuit which disables the erase\write logic whenever V_{CC} falls below 1.5 volts.

2

Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to one. There are three read operations: current address read, random address read and sequential read.

CURRENT ADDRESS READ: The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address "roll over" during read is from the last byte of the last memory page to the first byte of the first page.

Once the device address with the read/write select bit set to one is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input zero but does generate a following stop condition (refer to Figure 7).

RANDOM READ: A random read requires a "dummy" byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a zero but does generate a following stop condition (refer to Figure 8).

SEQUENTIAL READ: Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will "roll over" and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a zero but does generate a following stop condition (refer to Figure 9).

Figure 4. Device Address

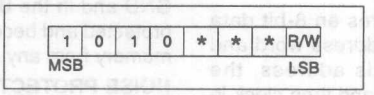


Figure 5. Byte Write

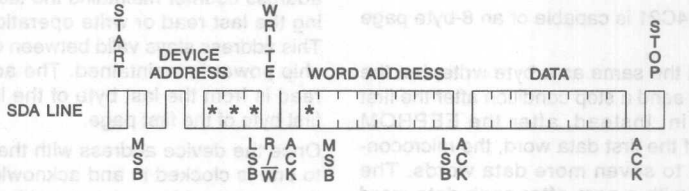
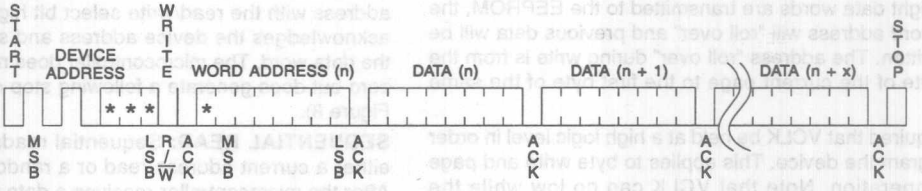


Figure 6. Page Write



(*=Don't care bits)

Figure 7. Current Address Read

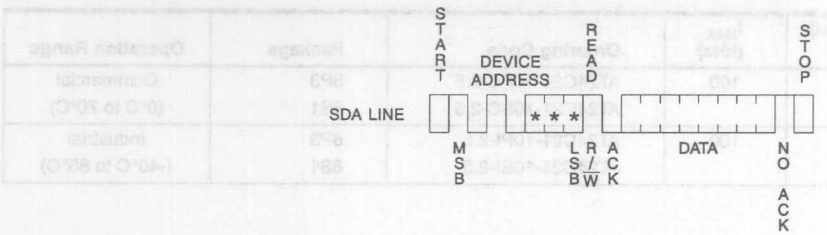


Figure 8. Random Read

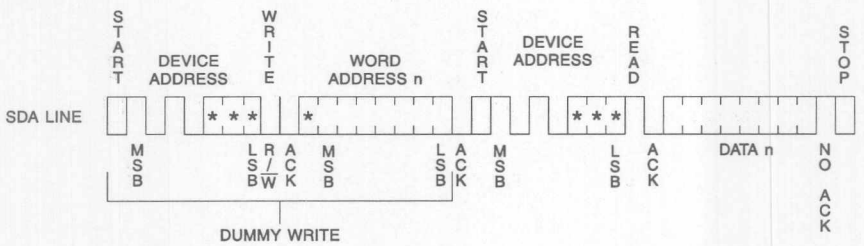
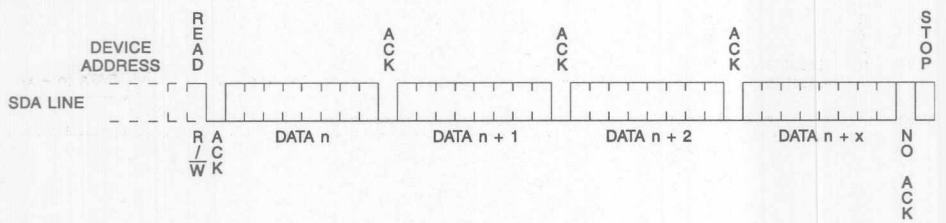


Figure 9. Sequential Read



(*=Don't care bits)

Ordering Information

t_{WR} (max) (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	3000	4	100	AT24C21-10PC-2.5 AT24C21-10SC-2.5	8P3 8S1	Commercial (0°C to 70°C)
	3000	4	100	AT24C21-10PI-2.5 AT24C21-10SI-2.5	8P3 8S1	Industrial (-40°C to 85°C)

Package Type	
8P3	8-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
Options	
-2.5	Low-Voltage (2.5V to 5.5V)

Features

- Permanent Software Write Protection for the First-Half of the Array
  - Software Procedure to Verify Write Protect Status
- Hardware Write Protection for the Entire Array
- Low Voltage and Standard Voltage Operation
  - 5.0 (V_{CC} = 4.5V to 5.5V)
  - 2.7 (V_{CC} = 2.7V to 5.5V)
  - 1.8 (V_{CC} = 1.8V to 5.5V)
- Internally Organized 256 x 8
- 2-Wire Serial Interface
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- Bidirectional Data Transfer Protocol
- 100 kHz (1.8V and 2.7V) and 400 kHz (5.0V) Compatibility
- 16-Byte Page Write Modes
- Partial Page Writes Are Allowed
- Self-Timed Write Cycle (10 ms max)
- High Reliability
  - Endurance: 1 Million Write Cycles
  - Data Retention: 100 Years
  - ESD Protection: >3,000V
- Automotive Grade and Extended Temperature Devices Available
- 8-Pin PDIP, 8-Pin JEDEC SOIC and 8-Pin TSSOP Packages

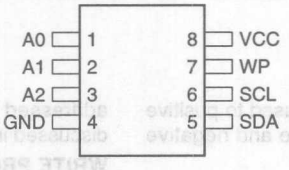
Description

The AT34C02 provides 2048 bits of serial electrically erasable and programmable read only memory (EEPROM) organized as 256 words of 8 bits each. The first-half of the device incorporates a software write protection feature while hardware write protection for the entire array is available via an external pin as well. Once the software write protection is enabled, by sending a special command to the device, it cannot be reversed. The hardware write protection is controlled with the WP pin and can be used to protect the entire array, whether or not the software write protection has been enabled. This allows the user to protect none, first-half, or all of the array depending on the application. The device is optimized for use in many industrial and commercial applications where low power and low voltage operations are essential. The AT34C02 is available in space saving 8-pin PDIP, 8-pin JEDEC SOIC, and 8-pin TSSOP packages and is accessed via a 2-wire serial interface. In addition, it is available in 5.0V (4.5V to 5.5V), 2.7V (2.7V to 5.5V), and 1.8V (1.8V to 5.5V) versions.

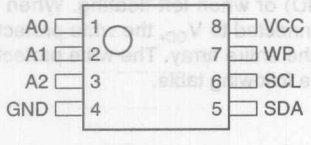
Pin Configurations

Pin Name	Function
A0 - A2	Address Inputs
SDA	Serial Data
SCL	Serial Clock Input
WP	Write Protect

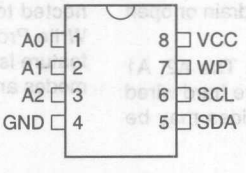
8-Pin SOIC



8-Pin TSSOP



8-Pin PDIP



2

2-Wire Serial EEPROM with Permanent Software Write Protect

2K (256 x 8)

AT34C02

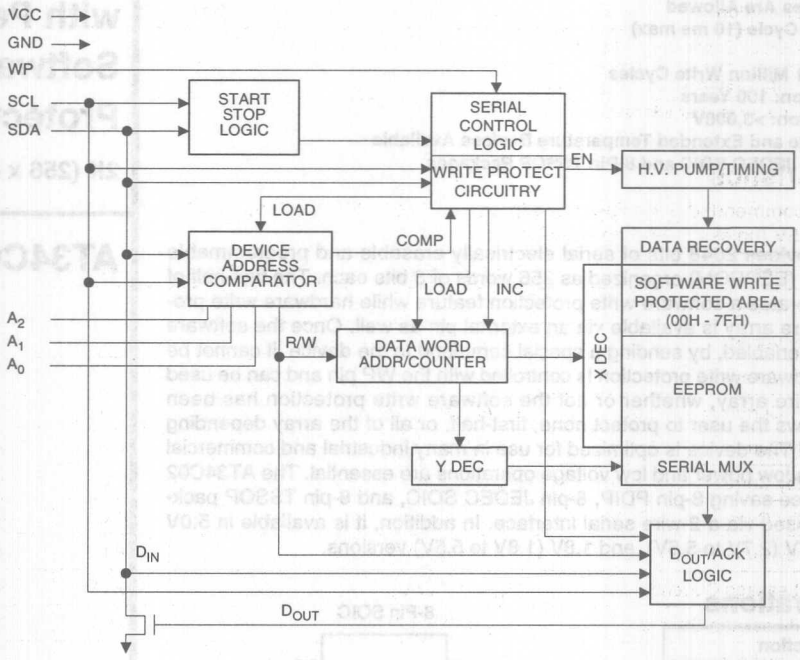
Rev. 0958D–07/98

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Block Diagram



Pin Description

SERIAL CLOCK (SCL): The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

SERIAL DATA (SDA): The SDA pin is bidirectional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open collector devices.

DEVICE/PAGE ADDRESSES (A2, A1, A0): The A2, A1 and A0 pins are device address inputs that are hard wired for the AT34C02. As many as eight 2K devices may be addressed on a single bus system (device addressing is discussed in detail under the Device Addressing section).

WRITE PROTECT (WP): The AT34C02 has a Write Protect pin that provides hardware data protection. The Write Protect pin allows normal read/write operations when connected to ground (GND) or when left floating. When the Write Protect pin is connected to V_{CC}, the write protection feature is enabled for the entire array. The write protection modes are shown in the following table.

AT34C02 Write Protection Modes

WP Pin Status	Write Protect Register	Part of the Array Write Protected
V_{CC}	—	Full Array (2K)
GND or Floating	Not Programmed	Normal Read/Write
GND or Floating	Programmed	First-Half of Array (1K: 00H - 7FH)

Pin Capacitance[1]

Applicable over recommended operating range from T_A = 25°C, f = 1.0 MHz, V_{CC} = +1.8V

Symbol	Test Condition	Max	Units	Conditions
$C_{I/O}$	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}	Input Capacitance (A_0, A_1, A_2, SCL)	6	pF	V_{IN} = 0V

Note: 1. This parameter is characterized and is not 100% tested

DC Characteristics

Applicable over recommended operating range from: T_{AI} = -40°C to +85°C, V_{CC} = +1.8V to +5.5V, T_{AC} = 0°C to +70°C, V_{CC} = +1.8V to +5.5V (unless otherwise noted).

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V_{CC1}	Supply Voltage		1.8		5.5	V
V_{CC2}	Supply Voltage		2.7		5.5	V
V_{CC3}	Supply Voltage		4.5		5.5	V
I_{CC}	Supply Current V_{CC} = 5.0V	READ at 100 kHz		0.4	1.0	mA
I_{CC}	Supply Current V_{CC} = 5.0V	WRITE at 100 kHz		2.0	3.0	mA
I_{SB1}	Standby Current V_{CC} = 1.8V	V_{IN} = V_{CC} or V_{SS}		0.6	3.0	µA
I_{SB2}	Standby Current V_{CC} = 2.7V	V_{IN} = V_{CC} or V_{SS}		1.6	4.0	µA
I_{SB3}	Standby Current V_{CC} = 5.0V	V_{IN} = V_{CC} or V_{SS}		8.0	18.0	µA
I_{LI}	Input Leakage Current	V_{IN} = V_{CC} or V_{SS}		0.10	3.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{CC} or V_{SS}		0.05	3.0	µA
V_{IL}	Input Low Level[1]		-0.6		V_{CC} x 0.3	V
V_{IH}	Input High Level[1]		V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL2}	Output Low Level V_{CC} = 3.0V	I_{OL} = 2.1 mA			0.4	V
V_{OL1}	Output Low Level V_{CC} = 1.8V	I_{OL} = 0.15 mA			0.2	V

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

AC Characteristics

Applicable over recommended operating range from T_A = -40°C to +85°C, V_{CC} = +1.8V to +5.5V, C_L = 1 TTL Gate and 100 pF (unless otherwise noted).

Symbol	Parameter	1.8V, 2.7V		5.0V		Units
		Min	Max	Min	Max	
f_{SCL}	Clock Frequency, SCL		100		400	kHz
t_{LOW}	Clock Pulse Width Low	4.7		1.2		µs
t_{HIGH}	Clock Pulse Width High	4.0		0.6		µs
t_I	Noise Suppression Time(1)		100		50	ns
t_{AA}	Clock Low to Data Out Valid	0.1	4.5	0.1	0.9	µs
t_{BUF}	Time the bus must be free before a new transmission can start(1)	4.7		1.2		µs
$t_{HD.STA}$	Start Hold Time	4.0		0.6		µs
$t_{SU.STA}$	Start Set-up Time	4.7		0.6		µs
$t_{HD.DAT}$	Data In Hold Time	0		0		µs
$t_{SU.DAT}$	Data In Set-up Time	200		100		ns
t_R	Inputs Rise Time(1)		1.0		0.3	µs
t_F	Inputs Fall Time(1)		300		300	ns
$t_{SU.STO}$	Stop Set-up Time	4.7		0.6		µs
t_{DH}	Data Out Hold Time	100		50		ns
t_{WR}	Write Cycle Time		10		10	ms
Endurance(1)	5.0V, 25°C, Page Mode	1M		1M		Write Cycles

Note: 1. This parameter is characterized and is not 100% tested.

Memory Organization

AT34C02, 2K Serial EEPROM: The 2K is internally organized with 256 pages of 1 byte each. Random word addressing requires a 8-bit data word address.

Device Operation

CLOCK and DATA TRANSITIONS: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (refer to Data Validity timing diagram). Data changes during SCL high periods will indicate a start or stop condition as defined below.

START CONDITION: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (refer to Start and Stop Definition timing diagram).

STOP CONDITION: A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode (refer to Start and Stop Definition timing diagram).

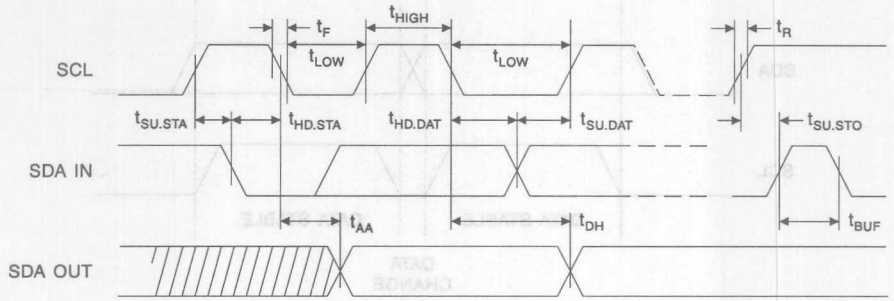
ACKNOWLEDGE: All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a zero to acknowledge that it has received each word. This happens during the ninth clock cycle.

STANDBY MODE: The AT34C02 features a low power standby mode which is enabled: (a) upon power-up or (b) after the receipt of the STOP bit and the completion of any internal operations.

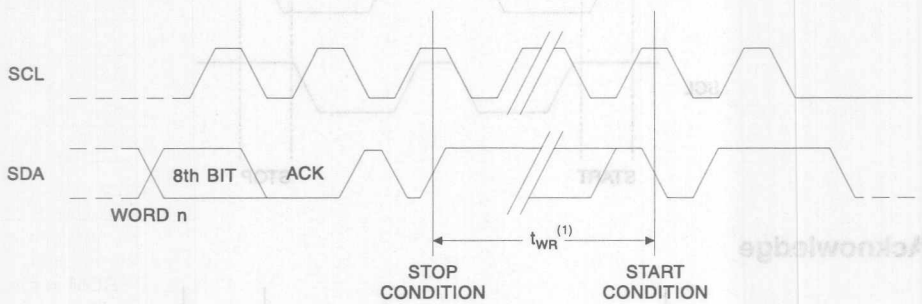
MEMORY RESET: After an interruption in protocol, power loss or system reset, any 2-wire part can be reset by following these steps:

(a) Clock up to 9 cycles, (b) look for SDA high in each cycle while SCL is high and then (c) create a start condition as SDA is high.

Bus Timing SCL: Serial Clock SDA: Serial Data I/O

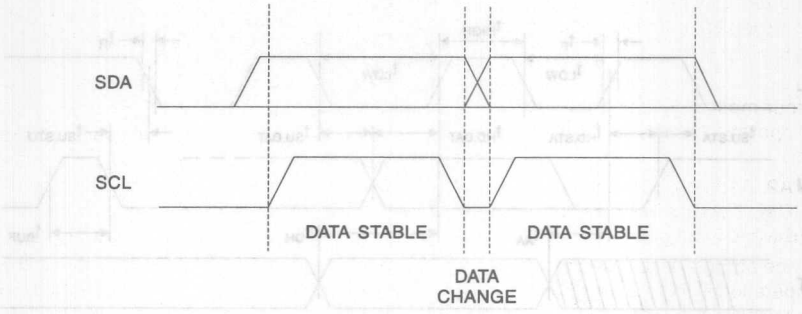


Write Cycle Timing SCL: Serial Clock SDA: Serial Data I/O

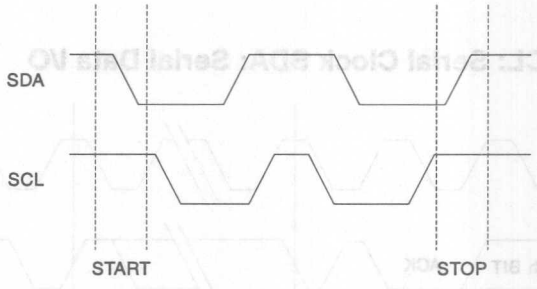


Note: 1. The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

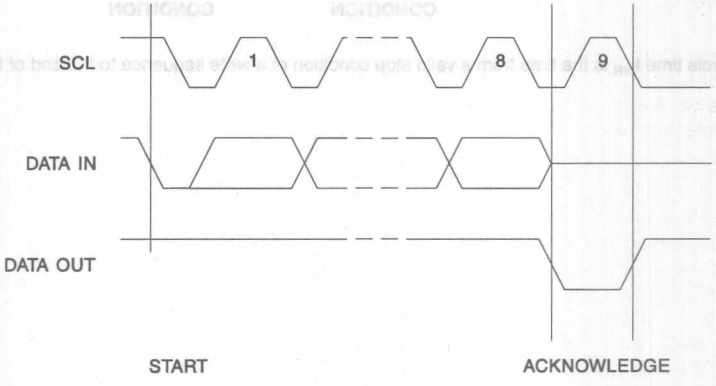
Data Validity



Start and Stop Condition



Output Acknowledge



Device Addressing

The 2K EEPROM device requires an 8-bit device address word following a start condition to enable the chip for a read or write operation (refer to Figure 2).

The device address word consists of a mandatory one-zero sequence for the first four most-significant bits (1010) for normal read and write operations and 0110 for writing to the write protect register.

The next 3 bits are the A2, A1 and A0 device address bits for the AT34C02 EEPROM. These 3 bits must compare to their corresponding hard-wired input pins.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

Upon a compare of the device address, the EEPROM will output a zero. If a compare is not made, the chip will return to a standby state. The device will not acknowledge if the write protect register has been programmed and the control code is 0110.

Write Operations

BYTE WRITE: A write operation requires an 8-bit data word address following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a zero and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a zero and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally-timed write cycle, t_{WR}, to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (refer to Figure 3).

The device will acknowledge a write command, but not write the data, if the software or hardware write protection has been enabled. The write cycle time must be observed even when the write protection is enabled.

PAGE WRITE: The 2K device is capable of 16-byte page write.

A page write is initiated the same as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to fifteen more data words. The EEPROM will respond with a zero after each data word received. The microcontroller must terminate the page write sequence with a stop condition (refer to Figure 4).

The data word address lower four bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than sixteen data words are transmitted to the EEPROM, the data word address will "roll over" and previous data will be overwritten. The address "roll over" during write is from the last byte of the current page to the first byte of the same page.

The device will acknowledge a write command, but not write the data, if the software or hardware write protection has been enabled. The write cycle time must be observed even when the write protection is enabled.

ACKNOWLEDGE POLLING: Once the internally-timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a zero allowing the read or write sequence to continue.

Write Protection

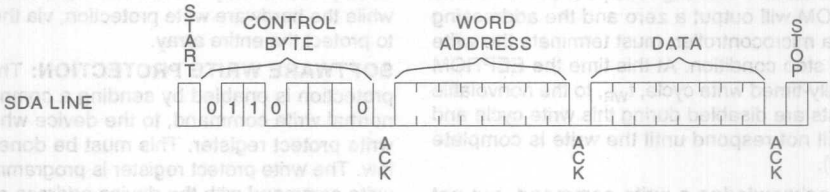
The software write protection, once enabled, permanently write protects only the first-half of the array (00H - 7FH) while the hardware write protection, via the WP pin, is used to protect the entire array.

SOFTWARE WRITE PROTECTION: The software write protection is enabled by sending a command, similar to a normal write command, to the device which programs the write protect register. This must be done with the WP pin low. The write protect register is programmed by sending a write command with the device address of 0110 instead of 1010 with the address and data bit being don't cares (refer to Figure 1). Once the software write protection has been enabled, the device will no longer acknowledge the 0110 control byte. The software write protection cannot be reversed even if the device is powered down. The write cycle time must be observed.

HARDWARE WRITE PROTECTION: The WP pin can be connected to V_{CC}, GND, or left floating. Connecting the WP pin to V_{CC} will write protect the entire array, regardless of whether or not the software write protection has been enabled. The software write protection register cannot be programmed when the WP pin is connected to V_{CC}. If the WP pin is connected to GND or left floating, the write protection mode is determined by the status of the software write protect register.

WP Connected to GND or Floating				
Start	**R/W Bit**	**Write Protect Register**	**Acknowledgment from Device**	**Action from Device**
1010	R	X	ACK	Read Array
1010	W	Programmed	ACK	Can Write to First Half Only
1010	W	Not Programmed	ACK	Can Write to Full Array
0110	R	Programmed	No ACK	Stop - Indicates Write Protect Register is Programmed
0110	R	Not Programmed	ACK	Read Out Data Don't Care. Indicates WP Register is Not Prog
0110	W	Programmed	No ACK	Stop - Indicates Write Protect Register is Programmed
0110	W	Not Programmed	ACK	Program Write Protect Register (irreversible)
WP Connected to V_{CC}				
1010	R	X	ACK	Read Array
1010	W	Programmed	ACK	Device Write Protect
1010	W	Not Programmed	ACK	Device Write Protect
0110	R	Programmed	No ACK	Stop - Indicates Write Protect Register is Programmed
0110	R	Not Programmed	ACK	Read Out Data Don't Care. Indicates WP Register is Not Prog
0110	W	Programmed	No ACK	Stop - Indicates Write Protect Register is Programmed
0110	W	Not Programmed	ACK	Cannot Program Write Protect Register

Figure 1. Setting Write Protect Register



Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to one. There are three read operations: current address read, random address read and sequential read.

CURRENT ADDRESS READ: The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address "roll over" during read is from the last byte of the last memory page to the first byte of the first page.

Once the device address with the read/write select bit set to one is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. To end the command, the microcontroller does not respond with an input zero but does generate a following stop condition (refer to Figure 5).

RANDOM READ: A random read requires a "dummy" byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. To end the command, the microcontroller does not respond with a zero but does generate a following stop condition (refer to Figure 6).

SEQUENTIAL READ: Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will "roll over" and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a zero but does generate a following stop condition (refer to Figure 7).

WRITE PROTECT REGISTER STATUS: To find out if the register has been programmed, the same procedure is used as to program the register except that the R/W bit is set to 1. If the device acknowledges, then the write protect register has not been programmed. Otherwise, it has been programmed and the device is permanently write protected at the first half of the array.

Figure 2. Device Address

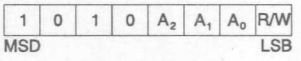


Figure 3. Byte Write

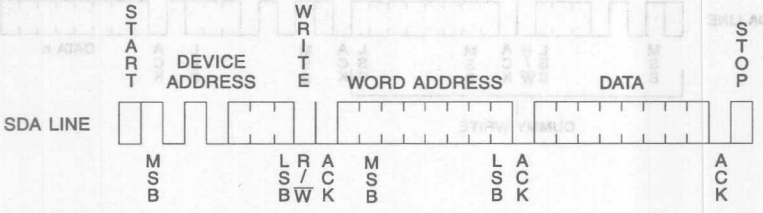


Figure 4. Page Write

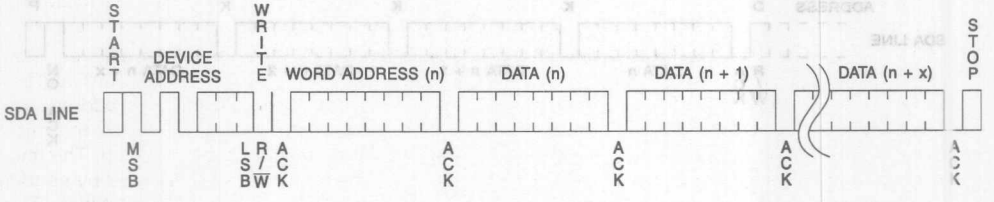


Figure 5. Current Address Read

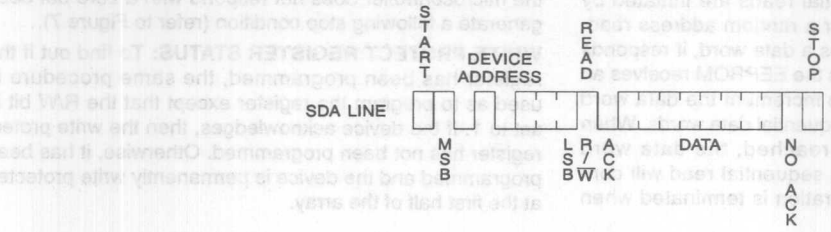


Figure 6. Random Read

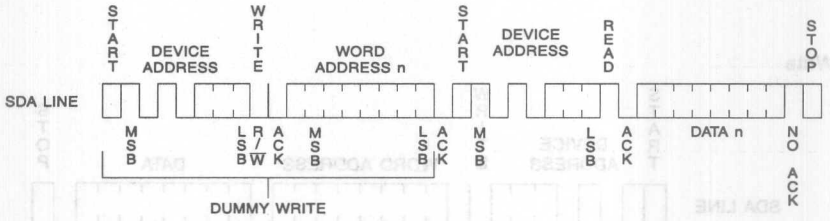
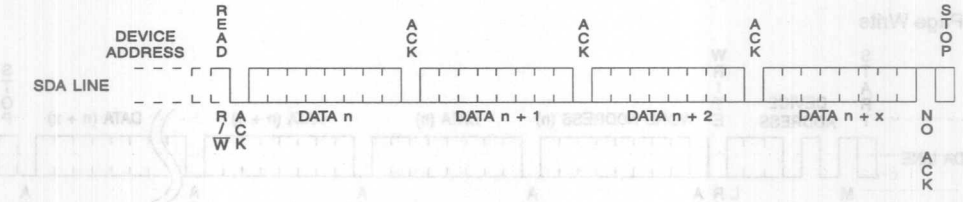


Figure 7. Sequential Read



Ordering Information

t_{WR} (max) (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	3000	18	400	AT34C02-10PC AT34C02N-10SC AT34C02-10TC	8P3 8S1 8T	Commercial (0°C to 70°C)
	3000	18	400	AT34C02-10PI AT34C02N-10SI AT34C02-10TI	8P3 8S1 8T	Industrial (-40°C to 85°C)
10	1500	4	100	AT34C02-10PC-2.7 AT34C02N-10SC-2.7 AT34C02-10TC-2.7	8P3 8S1 8T	Commercial (0°C to 70°C)
	1500	4	100	AT34C02-10PI-2.7 AT34C02N-10SI-2.7 AT34C02-10TI-2.7	8P3 8S1 8T	Industrial (-40°C to 85°C)
10	800	3	100	AT34C02-10PC-1.8 AT34C02N-10SC-1.8 AT34C02-10TC-1.8	8P3 8S1 8T	Commercial (0°C to 70°C)
	800	3	100	AT34C02-10PI-1.8 AT34C02N-10SI-1.8 AT34C02-10TI-1.8	8P3 8S1 8T	Industrial (-40°C to 85°C)

Package Type	
8P3	8-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8-Lead, 0.150" Wide, Plastic Gull Wing Small Outline Package(JEDEC SOIC)
8T	8-Lead, 0.170" Wide, Thin Shrink Small Outline Package (TSSOP)
Options	
Blank	Standard Operation (4.5V to 5.5V)
-2.7	Low Voltage (2.7V to 5.5V)
-1.8	Low Voltage (1.8V to 5.5V)

t_{WR} (max) (sec)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	3000	18	400	AT34C02-10PC AT34C02N-10SC AT34C02-10TC	8P3 8S1 8T	Commercial (0°C to 70°C)
	3000	18	400	AT34C02-10PI AT34C02N-10SI AT34C02-10TI	8P3 8S1 8T	Industrial (-40°C to 85°C)
10	1500	4	100	AT34C02-10PC-2.7 AT34C02N-10SC-2.7 AT34C02-10TC-2.7	8P3 8S1 8T	Commercial (0°C to 70°C)
	1500	4	100	AT34C02-10PI-2.7 AT34C02N-10SI-2.7 AT34C02-10TI-2.7	8P3 8S1 8T	Industrial (-40°C to 85°C)
10	800	3	100	AT34C02-10PC-1.8 AT34C02N-10SC-1.8 AT34C02-10TC-1.8	8P3 8S1 8T	Commercial (0°C to 70°C)
	800	3	100	AT34C02-10PI-1.8 AT34C02N-10SI-1.8 AT34C02-10TI-1.8	8P3 8S1 8T	Industrial (-40°C to 85°C)

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Blank	Standard Operation (4.5V to 5.5V)
-2.7	Low Voltage (2.7V to 5.5V)
-1.8	Low Voltage (1.8V to 5.5V)

Features

- Low-Voltage and Standard-Voltage Operation
  - 5.0 (V_{CC} = 4.5V to 5.5V)
  - 2.7 (V_{CC} = 2.7V to 5.5V)
  - 2.5 (V_{CC} = 2.5V to 5.5V)
  - 1.8 (V_{CC} = 1.8V to 5.5V)
- Internally Organized 128 x 8 (1K), 256 x 8 (2K), 512 x 8 (4K), 1024 x 8 (8K) or 2048 x 8 (16K)
- 2-Wire Serial Interface
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- Bidirectional Data Transfer Protocol
- 100 kHz (1.8V, 2.5V, 2.7V) and 400 kHz (5V) Compatibility
- Write Protect Pin for Hardware Data Protection
- 8-Byte Page (1K, 2K), 16-Byte Page (4K, 8K, 16K) Write Modes
- Partial Page Writes Are Allowed
- Self-Timed Write Cycle (10 ms max)
- High Reliability
  - Endurance: 1 Million Write Cycles
  - Data Retention: 100 Years
  - ESD Protection: >3000V
- Automotive Grade and Extended Temperature Devices Available
- 8-Pin and 14-Pin JEDEC SOIC, 8-Pin PDIP, 8-Pin MSOP, and 8-Pin TSSOP Packages

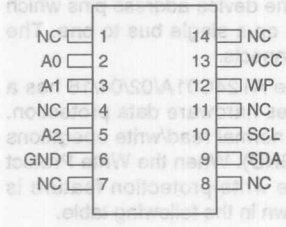
Description

The AT24C01A/02/04/08/16 provides 1024/2048/4096/8192/16384 bits of serial electrically erasable and programmable read only memory (EEPROM) organized as 128/256/512/1024/2048 words of 8 bits each. The device is optimized for use in many industrial and commercial applications where low power and low voltage operation are essential. The AT24C01A/02/04/08/16 is available in space saving 8-pin PDIP, (AT24C01A/02/04/08/16), 8-Pin MSOP (AT24C01A/02), 8-Pin TSSOP (AT24C01A/02/04/08/16), and 8-Pin and 14-Pin JEDEC SOIC (AT24C01A/02/04/08/16) packages and is accessed via a 2-wire serial interface. In addition, the entire family is available in 5.0V (4.5V to 5.5V), 2.7V (2.7V to 5.5V), 2.5V (2.5V to 5.5V) and 1.8V (1.8V to 5.5V) versions.

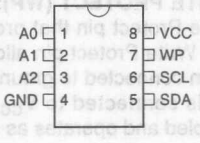
Pin Configurations

Pin Name	Function
A0 - A2	Address Inputs
SDA	Serial Data
SCL	Serial Clock Input
WP	Write Protect
NC	No Connect

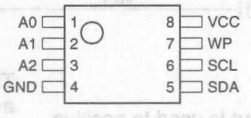
14-Pin SOIC



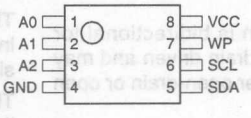
8-Pin PDIP



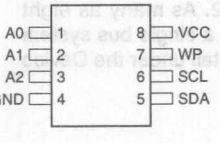
8-Pin TSSOP



8-Pin MSOP



8-Pin SOIC



2

2-Wire Serial EEPROM

1K (128 x 8)

2K (256 x 8)

4K (512 x 8)

8K (1024 x 8)

16K (2048 x 8)

AT24C01A
AT24C02
AT24C04
AT24C08
AT24C16

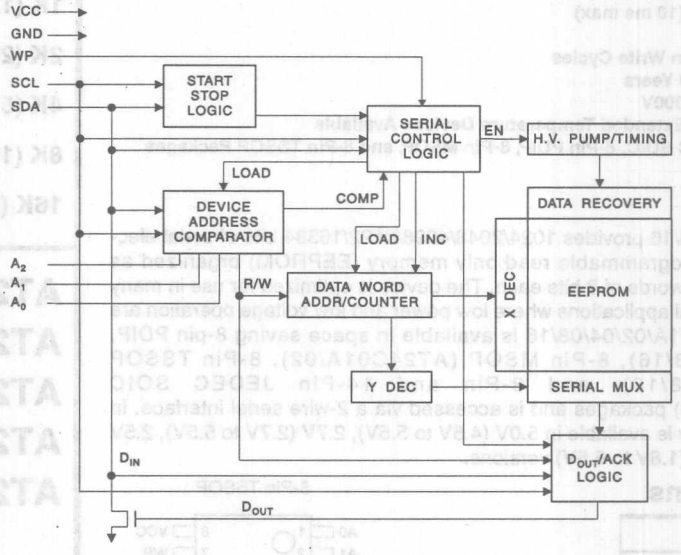
Rev. 0180D–10/98

Absolute Maximum Ratings

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Block Diagram



Pin Description

SERIAL CLOCK (SCL): The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

SERIAL DATA (SDA): The SDA pin is bidirectional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open collector devices.

DEVICE/PAGE ADDRESSES (A2, A1, A0): The A2, A1 and A0 pins are device address inputs that are hard wired for the AT24C01A and the AT24C02. As many as eight 1K/2K devices may be addressed on a single bus system (device addressing is discussed in detail under the Device Addressing section).

The AT24C04 uses the A2 and A1 inputs for hard wire addressing and a total of four 4K devices may be addressed on a single bus system. The A0 pin is a no connect.

The AT24C08 only uses the A2 input for hardwire addressing and a total of two 8K devices may be addressed on a single bus system. The A0 and A1 pins are no connects.

The AT24C16 does not use the device address pins which limits the number of devices on a single bus to one. The A0, A1 and A2 pins are no connects.

WRITE PROTECT (WP): The AT24C01A/02/04/16 has a Write Protect pin that provides hardware data protection. The Write Protect pin allows normal read/write operations when connected to ground (GND). When the Write Protect pin is connected to V_{CC}, the write protection feature is enabled and operates as shown in the following table.

WP Pin Status	Part of the Array Protected				
	24C01A	24C02	24C04	24C08	24C16
At V_{CC}	Full (1K) Array	Full (2K) Array	Full (4K) Array	Normal Read/ Write Operation	Upper Half (8K) Array
At GND	Normal Read/Write Operations				

Memory Organization

AT24C01A, 1K SERIAL EEPROM: Internally organized with 128 pages of 1-byte each, the 1K requires a 7-bit data word address for random word addressing.

AT24C02, 2K SERIAL EEPROM: Internally organized with 256 pages of 1-byte each, the 2K requires an 8-bit data word address for random word addressing.

AT24C04, 4K SERIAL EEPROM: The 4K is internally organized with 256 pages of 2 bytes each. Random word addressing Chip Number requires a 9-bit data word address.

AT24C08, 8K SERIAL EEPROM: The 8K is internally organized with 4 blocks of 256 pages of 4 bytes each. Random word addressing requires a 10-bit data word address.

AT24C16, 16K SERIAL EEPROM: The 16K is internally organized with 8 blocks of 256 pages of 8 bytes each. Random word addressing requires an 11-bit data word address.

2

Pin Capacitance[1]

Applicable over recommended operating range from T_A = 25°C, f = 1.0 MHz, V_{CC} = +1.8V.

Symbol	Test Condition	Max	Units	Conditions
$C_{I/O}$	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}	Input Capacitance (A_0, A_1, A_2, SCL)	6	pF	V_{IN} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

DC Characteristics

Applicable over recommended operating range from: T_{AI} = -40°C to +85°C, V_{CC} = +1.8V to +5.5V, T_{AC} = 0°C to +70°C, V_{CC} = +1.8V to +5.5V (unless otherwise noted).

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V_{CC1}	Supply Voltage		1.8		5.5	V
V_{CC2}	Supply Voltage		2.5		5.5	V
V_{CC3}	Supply Voltage		2.7		5.5	V
V_{CC4}	Supply Voltage		4.5		5.5	V
I_{CC}	Supply Current V_{CC} = 5.0V	READ at 100 kHz		0.4	1.0	mA
I_{CC}	Supply Current V_{CC} = 5.0V	WRITE at 100 kHz		2.0	3.0	mA
I_{SB1}	Standby Current V_{CC} = 1.8V	V_{IN} = V_{CC} or V_{SS}		0.6	3.0	µA
I_{SB2}	Standby Current V_{CC} = 2.5V	V_{IN} = V_{CC} or V_{SS}		1.4	4.0	µA
I_{SB3}	Standby Current V_{CC} = 2.7V	V_{IN} = V_{CC} or V_{SS}		1.6	4.0	µA
I_{SB4}	Standby Current V_{CC} = 5.0V	V_{IN} = V_{CC} or V_{SS}		8.0	18.0	µA
I_{LI}	Input Leakage Current	V_{IN} = V_{CC} or V_{SS}		0.10	3.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{CC} or V_{SS}		0.05	3.0	µA
V_{IL}	Input Low Level[1]		-0.6		V_{CC} x 0.3	V
V_{IH}	Input High Level[1]		V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL2}	Output Low Level V_{CC} = 3.0V	I_{OL} = 2.1 mA			0.4	V
V_{OL1}	Output Low Level V_{CC} = 1.8V	I_{OL} = 0.15 mA			0.2	V

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

AC Characteristics

Applicable over recommended operating range from T_A = -40°C to +85°C, V_{CC} = +1.8V to +5.5V, CL = 1 TTL Gate and 100pF (unless otherwise noted).

Symbol	Parameter	2.7-, 2.5-, 1.8-volt		5.0-volt		Units
		Min	Max	Min	Max	
f_{SCL}	Clock Frequency, SCL		100		400	kHz
t_{LOW}	Clock Pulse Width Low	4.7		1.2		µs
t_{HIGH}	Clock Pulse Width High	4.0		0.6		µs
t_I	Noise Suppression Time(1)		100		50	ns
t_{AA}	Clock Low to Data Out Valid	0.1	4.5	0.1	0.9	µs
t_{BUF}	Time the bus must be free before a new transmission can start(1)	4.7		1.2		µs
$t_{HD.STA}$	Start Hold Time	4.0		0.6		µs
$t_{SU.STA}$	Start Set-up Time	4.7		0.6		µs
$t_{HD.DAT}$	Data In Hold Time	0		0		µs
$t_{SU.DAT}$	Data In Set-up Time	200		100		ns
t_R	Inputs Rise Time(1)		1.0		0.3	µs
t_F	Inputs Fall Time(1)		300		300	ns
$t_{SU.STO}$	Stop Set-up Time	4.7		0.6		µs
t_{DH}	Data Out Hold Time	100		50		ns
t_{WR}	Write Cycle Time		10		10	ms
Endurance(1)	5.0V, 25°C, Page Mode	1M		1M		Write Cycles

Note: 1. This parameter is characterized and is not 100% tested.

Device Operation

CLOCK and DATA TRANSITIONS: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (refer to Data Validity timing diagram). Data changes during SCL high periods will indicate a start or stop condition as defined below.

START CONDITION: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (refer to Start and Stop Definition timing diagram).

STOP CONDITION: A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode (refer to Start and Stop Definition timing diagram).

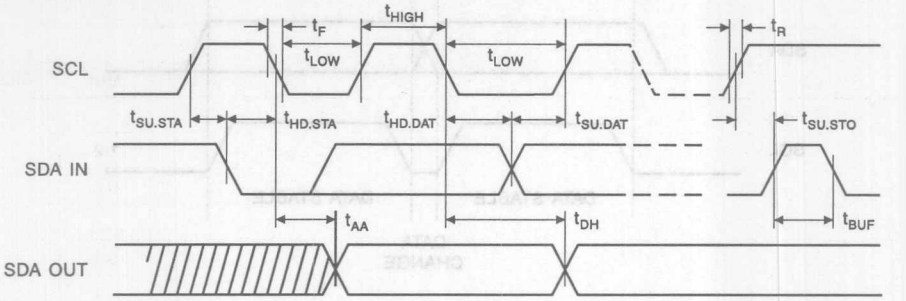
ACKNOWLEDGE: All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a zero to acknowledge that it has received each word. This happens during the ninth clock cycle.

STANDBY MODE: The AT24C01A/02/04/08/16 features a low power standby mode which is enabled: (a) upon power-up and (b) after the receipt of the STOP bit and the completion of any internal operations.

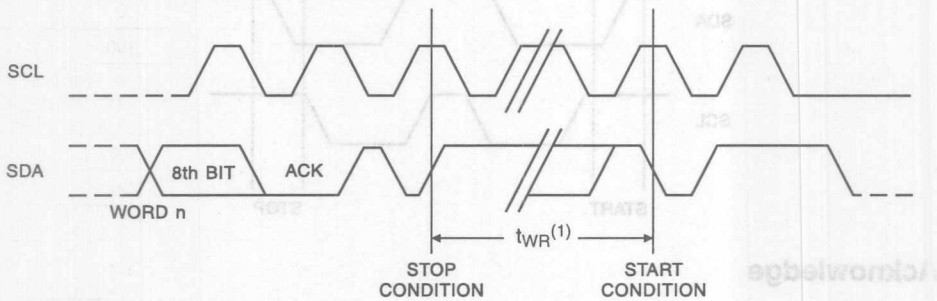
MEMORY RESET: After an interruption in protocol, power loss or system reset, any 2-wire part can be reset by following these steps:

1. Clock up to 9 cycles.
2. Look for SDA high in each cycle while SCL is high.
3. Create a start condition as SDA is high.

Bus Timing
SCL: Serial Clock, SDA: Serial Data I/O

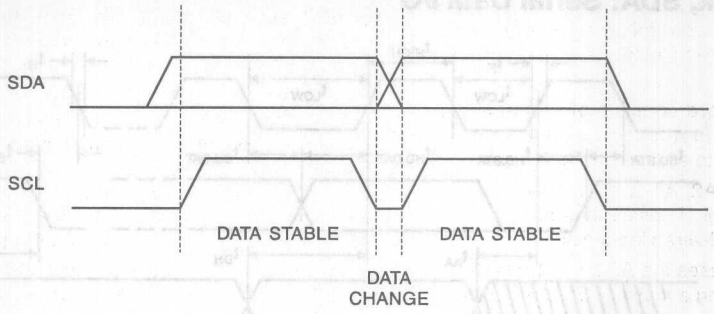


Write Cycle Timing
SCL: Serial Clock, SDA: Serial Data I/O

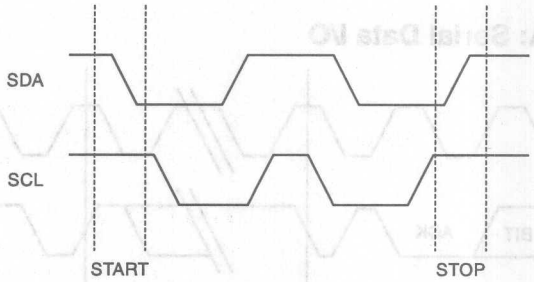


Note: 1. The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

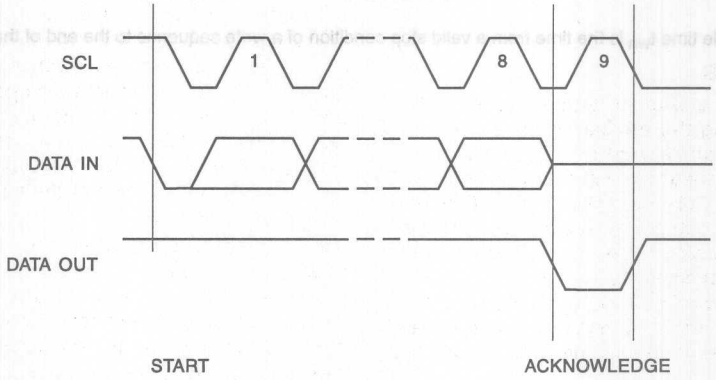
Data Validity



Start and Stop Definition



Output Acknowledge



Device Addressing

The 1K, 2K, 4K, 8K and 16K EEPROM devices all require an 8-bit device address word following a start condition to enable the chip for a read or write operation (refer to Figure 1).

The device address word consists of a mandatory one, zero sequence for the first four most significant bits as shown. This is common to all the EEPROM devices.

The next 3 bits are the A2, A1 and A0 device address bits for the 1K/2K EEPROM. These 3 bits must compare to their corresponding hard-wired input pins.

The 4K EEPROM only uses the A2 and A1 device address bits with the third bit being a memory page address bit. The two device address bits must compare to their corresponding hard-wired input pins. The A0 pin is no connect.

The 8K EEPROM only uses the A2 device address bit with the next 2 bits being for memory page addressing. The A2 bit must compare to its corresponding hard-wired input pin. The A1 and A0 pins are no connect.

The 16K does not use any device address bits but instead the 3 bits are used for memory page addressing. These page addressing bits on the 4K, 8K, and 16K devices should be considered the most significant bits of the data word address which follows. The A0, A1 and A2 pins are no connect.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

Upon a compare of the device address, the EEPROM will output a zero. If a compare is not made, the chip will return to a standby state.

Write Operations

BYTE WRITE: A write operation requires an 8-bit data word address following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a zero and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a zero and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally-timed write cycle, t_{WR}, to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (refer to Figure 2).

PAGE WRITE: The 1K/2K EEPROM is capable of an 8-byte page write, and the 4K, 8K and 16K devices are capable of 16-byte page writes.

A page write is initiated the same as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to seven (1K/2K) or fifteen (4K, 8K, 16K) more data words. The EEPROM will respond with a zero after each data word received. The microcontroller must terminate the page write sequence with a stop condition (refer to Figure 3).

The data word address lower three (1K/2K) or four (4K, 8K, 16K) bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than eight (1K/2K) or sixteen (4K, 8K, 16K) data words are transmitted to the EEPROM, the data word address will "roll over" and previous data will be overwritten.

ACKNOWLEDGE POLLING: Once the internally-timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a zero allowing the read or write sequence to continue.

Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to one. There are three read operations: current address read, random address read and sequential read.

CURRENT ADDRESS READ: The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address "roll over" during read is from the last byte of the last memory page to the first byte of the first page. The address "roll over" during write is from the last byte of the current page to the first byte of the same page.

Once the device address with the read/write select bit set to one is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input zero but does generate a following stop condition (refer to Figure 4).

RANDOM READ: A random read requires a "dummy" byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out

the data word. The microcontroller does not respond with a zero but does generate a following stop condition (refer to Figure 5).

SEQUENTIAL READ: Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will "roll over" and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a zero but does generate a following stop condition (refer to Figure 6).

Figure 1. Device Address

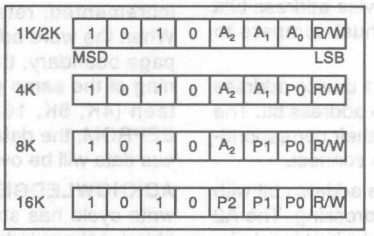


Figure 2. Byte Write

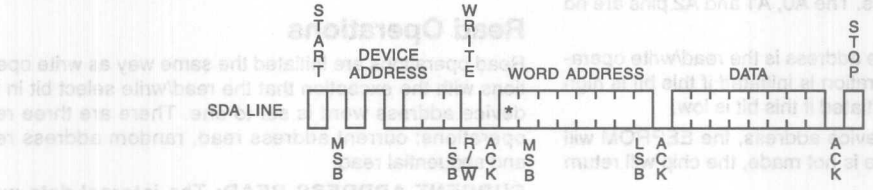
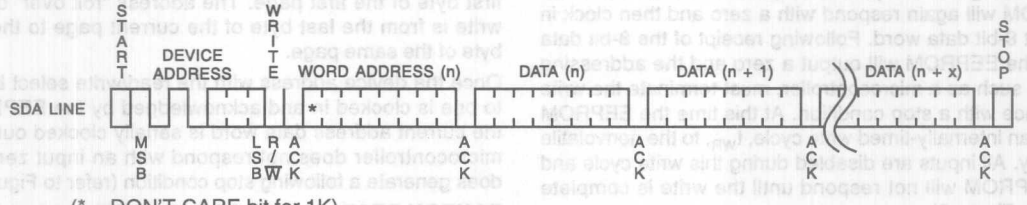


Figure 3. Page Write



(* = DON'T CARE bit for 1K)

Figure 4. Current Address Read

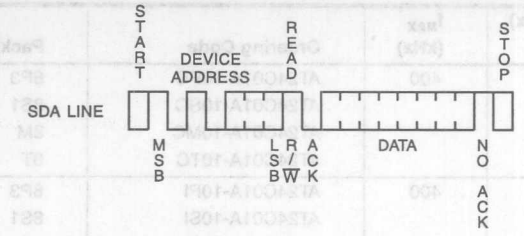
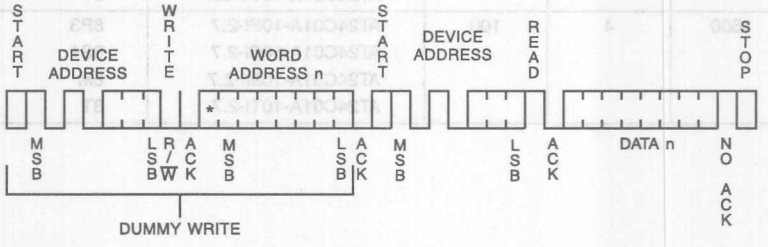
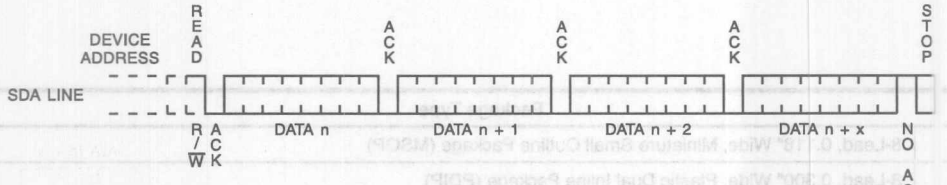


Figure 5. Random Read



(* = DON'T CARE bit for 1K)

Figure 6. Sequential Read



AT24C01A Ordering Information

t_{WR} (max) (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	3000	18	400	AT24C01A-10PC AT24C01A-10SC AT24C01A-10MC AT24C01A-10TC	8P3 8S1 8M 8T	Commercial (0°C to 70°C)
	3000	18	400	AT24C01A-10PI AT24C01A-10SI AT24C01A-10MI AT24C01A-10TI	8P3 8S1 8M 8T	Industrial (-40°C to 85°C)
10	1500	4	100	AT24C01A-10PC-2.7 AT24C01A-10SC-2.7 AT24C01A-10MC-2.7 AT24C01A-10TC-2.7	8P3 8S1 8M 8T	Commercial (0°C to 70°C)
	1500	4	100	AT24C01A-10PI-2.7 AT24C01A-10SI-2.7 AT24C01A-10MI-2.7 AT24C01A-10TI-2.7	8P3 8S1 8M 8T	Industrial (-40°C to 85°C)

Package Type	
8M	8-Lead, 0.118" Wide, Miniature Small Outline Package (MSOP)
8P3	8-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8T	8-Lead, 0.170" Wide, Thin Shrink Small Outline Package (TSSOP)
Options	
Blank	Standard Operation (4.5V to 5.5V)
-2.7	Low Voltage (2.7V to 5.5V)
-2.5	Low Voltage (2.5V to 5.5V)
-1.8	Low Voltage (1.8V to 5.5V)

AT24C01A Ordering Information (Continued)

t_{WR} (max) (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	1000	4	100	AT24C01A-10PC-2.5	8P3	Commercial
				AT24C01A-10SC-2.5	8S1	(0°C to 70°C)
				AT24C01A-10MC-2.5	8M	
				AT24C01A-10TC-2.5	8T	
	1000	4	100	AT24C01A-10PI-2.5	8P3	Industrial
				AT24C01A-10SI-2.5	8S1	(-40°C to 85°C)
				AT24C01A-10MI-2.5	8M	
				AT24C01A-10TI-2.5	8T	
10	800	3	100	AT24C01A-10PC-1.8	8P3	Commercial
				AT24C01A-10SC-1.8	8S1	(0°C to 70°C)
				AT24C01A-10MC-1.8	8M	
				AT24C01A-10TC-1.8	8T	
	800	3	100	AT24C01A-10PI-1.8	8P3	Industrial
				AT24C01A-10SI-1.8	8S1	(-40°C to 85°C)
				AT24C01A-10MI-1.8	8M	
				AT24C01A-10TI-1.8	8T	

Package Type	
8M	8-Lead, 0.118" Wide, Miniature Small Outline Package (MSOP)
8P3	8-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8T	8-Lead, 0.170" Wide, Thin Shrink Small Outline Package (TSSOP)
Options	
Blank	Standard Operation (4.5V to 5.5V)
-2.7	Low Voltage (2.7V to 5.5V)
-2.5	Low Voltage (2.5V to 5.5V)
-1.8	Low Voltage (1.8V to 5.5V)

AT24C02 Ordering Information

t_{WR} (max) (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	3000	18	400	AT24C02-10PC	8P3	Commercial (0°C to 70°C)
				AT24C02N-10SC	8S1	
				AT24C02-10SC	14S	
				AT24C02-10MC	8M	
				AT24C02-10TC	8T	
	3000	18	400	AT24C02-10PI	8P3	Industrial (-40°C to 85°C)
				AT24C02N-10SI	8S1	
				AT24C02-10SI	14S	
				AT24C02-10MI	8M	
				AT24C02-10TI	8T	
10	1500	4	100	AT24C02-10PC-2.7	8P3	Commercial (0°C to 70°C)
				AT24C02N-10SC-2.7	8S1	
				AT24C02-10SC-2.7	14S	
				AT24C02-10MC-2.7	8M	
				AT24C02-10TC-2.7	8T	
	1500	4	100	AT24C02-10PI-2.7	8P3	Industrial (-40°C to 85°C)
				AT24C02N-10SI-2.7	8S1	
				AT24C02-10SI-2.7	14S	
				AT24C02-10MI-2.7	8M	
				AT24C02-10TI-2.7	8T	

Package Type	
8M	8-Lead, 0.118" Wide, Miniature Small Outline Package (MSOP)
8P3	8-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8T	8-Lead, 0.170" Wide, Thin Shrink Small Outline Package (TSSOP)
14S	14-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
Options	
Blank	Standard Operation (4.5V to 5.5V)
-2.7	Low Voltage (2.7V to 5.5V)
-2.5	Low Voltage (2.5V to 5.5V)
-1.8	Low Voltage (1.8V to 5.5V)

AT24C02 Ordering Information (Continued)

t_{WR} (max) (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	1000	4	100	AT24C02-10PC-2.5	8P3	Commercial
				AT24C02N-10SC-2.5	8S1	(0°C to 70°C)
				AT24C02-10SC-2.5	14S	
				AT24C02-10MC-2.5	8M	
				AT24C02-10TC-2.5	8T	
	1000	4	100	AT24C02-10PI-2.5	8P3	Industrial
				AT24C02N-10SI-2.5	8S1	(-40°C to 85°C)
				AT24C02-10SI-2.5	14S	
				AT24C02-10MI-2.5	8M	
				AT24C02-10TI-2.5	8T	
10	800	3	100	AT24C02-10PC-1.8	8P3	Commercial
				AT24C02N-10SC-1.8	8S1	(0°C to 70°C)
				AT24C02-10SC-1.8	14S	
				AT24C02-10MC-1.8	8M	
				AT24C02-10TC-1.8	8T	
	800	3	100	AT24C02-10PI-1.8	8P3	Industrial
				AT24C02N-10SI-1.8	8S1	(-40°C to 85°C)
				AT24C02-10SI-1.8	14S	
				AT24C02-10MI-1.8	8M	
				AT24C02-10TI-1.8	8T	

Package Type	
8M	8-Lead, 0.118" Wide, Miniature Small Outline Package (MSOP)
8P3	8-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8T	8-Lead, 0.170" Wide, Thin Shrink Small Outline Package (TSSOP)
14S	14-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
Options	
Blank	Standard Operation (4.5V to 5.5V)
-2.7	Low Voltage (2.7V to 5.5V)
-2.5	Low Voltage (2.5V to 5.5V)
-1.8	Low Voltage (1.8V to 5.5V)

AT24C04 Ordering Information

t_{WR} (max) (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	3000	18	400	AT24C04-10PC AT24C04N-10SC AT24C04-10SC AT24C04-10TC	8P3 8S1 14S 8T	Commercial (0°C to 70°C)
	3000	18	400	AT24C04-10PI AT24C04N-10SI AT24C04-10SI AT24C04-10TI	8P3 8S1 14S 8T	Industrial (-40°C to 85°C)
10	1500	4	100	AT24C04-10PC-2.7 AT24C04N-10SC-2.7 AT24C04-10SC-2.7 AT24C04-10TC-2.7	8P3 8S1 14S 8T	Commercial (0°C to 70°C)
	1500	4	100	AT24C04-10PI-2.7 AT24C04N-10SI-2.7 AT24C04-10SI-2.7 AT24C04-10TI-2.7	8P3 8S1 14S 8T	Industrial (-40°C to 85°C)

Package Type	
8P3	8-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8T	8-Lead, 0.170" Wide, Thin Shrink Small Outline Package (TSSOP)
14S	14-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
Options	
Blank	Standard Operation (4.5V to 5.5V)
-2.7	Low Voltage (2.7V to 5.5V)
-2.5	Low Voltage (2.5V to 5.5V)
-1.8	Low Voltage (1.8V to 5.5V)

AT24C04 Ordering Information (Continued)

t_{WR} (max) (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	1000	4	100	AT24C04-10PC-2.5	8P3	Commercial (0°C to 70°C)
				AT24C04N-10SC-2.5	8S1	
				AT24C04-10SC-2.5	14S	
				AT24C04-10TC-2.5	8T	
	1000	4	100	AT24C04-10PI-2.5	8P3	Industrial (-40°C to 85°C)
				AT24C04N-10SI-2.5	8S1	
				AT24C04-10SI-2.5	14S	
				AT24C04-10TI-2.5	8T	
10	800	3	100	AT24C04-10PC-1.8	8P3	Commercial (0°C to 70°C)
				AT24C04N-10SC-1.8	8S1	
				AT24C04-10SC-1.8	14S	
				AT24C04-10TC-1.8	8T	
	800	3	100	AT24C04-10PI-1.8	8P3	Industrial (-40°C to 85°C)
				AT24C04N-10SI-1.8	8S1	
				AT24C04-10SI-1.8	14S	
				AT24C04-10TI-1.8	8T	

Package Type	
8P3	8-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8T	8-Lead, 0.170" Wide, Thin Shrink Small Outline Package (TSSOP)
14S	14-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
Options	
Blank	Standard Operation (4.5V to 5.5V)
-2.7	Low Voltage (2.7V to 5.5V)
-2.5	Low Voltage (2.5V to 5.5V)
-1.8	Low Voltage (1.8V to 5.5V)

AT24C08 Ordering Information

t_{WR} (max) (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	3000	18	400	AT24C08-10PC	8P3	Commercial (0°C to 70°C)
				AT24C08N-10SC	8S1	
				AT24C08-10SC	14S	
				AT24C08-10TC	8T	
	3000	18	400	AT24C08-10PI	8P3	Industrial (-40°C to 85°C)
				AT24C08N-10SI	8S1	
				AT24C08-10SI	14S	
				AT24C08-10TI	8T	
10	1500	4	100	AT24C08-10PC-2.7	8P3	Commercial (0°C to 70°C)
				AT24C08N-10SC-2.7	8S1	
				AT24C08-10SC-2.7	14S	
				AT24C08-10TC-2.7	8T	
	1500	4	100	AT24C08-10PI-2.7	8P3	Industrial (-40°C to 85°C)
				AT24C08N-10SI-2.7	8S1	
				AT24C08-10SI-2.7	14S	
				AT24C08-10TI-2.7	8T	

Package Type	
8P3	8-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8T	8-Lead, 0.170" Wide, Thin Shrink Small Outline Package (TSSOP)
14S	14-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
Options	
Blank	Standard Operation (4.5V to 5.5V)
-2.7	Low Voltage (2.7V to 5.5V)
-2.5	Low Voltage (2.5V to 5.5V)
-1.8	Low Voltage (1.8V to 5.5V)

AT24C08 Ordering Information (Continued)

t_{WR} (max) (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	1000	4	100	AT24C08-10PC-2.5 AT24C08N-10SC-2.5 AT24C08-10SC-2.5 AT24C08-10TC-2.5	8P3 8S1 14S 8T	Commercial (0°C to 70°C)
	1000	4	100	AT24C08-10PI-2.5 AT24C08N-10SI-2.5 AT24C08-10SI-2.5 AT24C08-10TI-2.5	8P3 8S1 14S 8T	Industrial (-40°C to 85°C)
10	800	3	100	AT24C08-10PC-1.8 AT24C08N-10SC-1.8 AT24C08-10SC-1.8 AT24C08-10TC-1.8	8P3 8S1 14S 8T	Commercial (0°C to 70°C)
	800	3	100	AT24C08-10PI-1.8 AT24C08N-10SI-1.8 AT24C08-10SI-1.8 AT24C08-10TI-1.8	8P3 8S1 14S 8T	Industrial (-40°C to 85°C)

Package Type	
8P3	8-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8T	8-Lead, 0.170" Wide, Thin Shrink Small Outline Package (TSSOP)
14S	14-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
Options	
Blank	Standard Operation (4.5V to 5.5V)
-2.7	Low Voltage (2.7V to 5.5V)
-2.5	Low Voltage (2.5V to 5.5V)
-1.8	Low Voltage (1.8V to 5.5V)

AT24C16 Ordering Information

t_{WR} (max) (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	3000	18	400	AT24C16-10PC AT24C16N-10SC AT24C16-10SC AT24C16-10TC	8P3 8S1 14S 8T	Commercial (0°C to 70°C)
	3000	18	400	AT24C16-10PI AT24C16N-10SI AT24C16-10SI AT24C16-10TI	8P3 8S1 14S 8T	Industrial (-40°C to 85°C)
10	1500	4	100	AT24C16-10PC-2.7 AT24C16N-10SC-2.7 AT24C16-10SC-2.7 AT24C16-10TC-2.7	8P3 8S1 14S 8T	Commercial (0°C to 70°C)
	1500	4	100	AT24C16-10PI-2.7 AT24C16N-10SI-2.7 AT24C16-10SI-2.7 AT24C16-10TI-2.7	8P3 8S1 14S 8T	Industrial (-40°C to 85°C)

Package Type	
8P3	8-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8T	8-Lead, 0.170" Wide, Thin Shrink Small Outline Package (TSSOP)
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Options	
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-2.5	Low Voltage (2.5V to 5.5V)
-1.8	Low Voltage (1.8V to 5.5V)

AT24C16 Ordering Information (Continued)

t_{WR} (max) (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	1000	4	100	AT24C16-10PC-2.5 AT24C16N-10SC-2.5 AT24C16-10SC-2.5 AT24C16-10TC-2.5	8P3 8S1 14S 8T	Commercial (0°C to 70°C)
	1000	4	100	AT24C16-10PI-2.5 AT24C16N-10SI-2.5 AT24C16-10SI-2.5 AT24C16-10TI-2.5	8P3 8S1 14S 8T	Industrial (-40°C to 85°C)
10	800	3	100	AT24C16-10PC-1.8 AT24C16N-10SC-1.8 AT24C16-10SC-1.8 AT24C16-10TC-1.8	8P3 8S1 14S 8T	Commercial (0°C to 70°C)
	800	3	100	AT24C16-10PI-1.8 AT24C16N-10SI-1.8 AT24C16-10SI-1.8 AT24C16-10TI-1.8	8P3 8S1 14S 8T	Industrial (-40°C to 85°C)

Package Type	
8P3	8-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8T	8-Lead, 0.170" Wide, Thin Shrink Small Outline Package (TSSOP)
14S	14-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
Options	
Blank	Standard Operation (4.5V to 5.5V)
-2.7	Low Voltage (2.7V to 5.5V)
-2.5	Low Voltage (2.5V to 5.5V)
-1.8	Low Voltage (1.8V to 5.5V)

Features

- Write Protect Pin for Hardware Data Protection
  - Utilizes Different Array Protection Compared to the AT24C02/04/08
- Low Voltage and Standard Voltage Operation
  - 5.0 (V_{CC} = 4.5V to 5.5V)
  - 2.7 (V_{CC} = 2.7V to 5.5V)
  - 2.5 (V_{CC} = 2.5V to 5.5V)
  - 1.8 (V_{CC} = 1.8V to 5.5V)
- Internally Organized 256 x 8 (2K), 512 x 8 (4K) or 1024 x 8 (8K)
- 2-Wire Serial Interface
- Schmitt Trigger, Filtered Inputs for Noise Supperssion
- Bidirectional Data Transfer Protocol
- 100 kHz (1.8V, 2.5V, 2.7V) and 400 kHz (5V) Compatibility
- 8-Byte Page (2K), 16-Byte Page (4K, 8K) Write Modes
- Partial Page Writes Are Allowed
- Self-Timed Write Cycle (10 ms max)
- High Reliability
  - Endurance: 1 Million Write Cycles
  - Data Retention: 100 Years
  - ESD Protection: >3000V
- Automotive Grade and Extended Temperature Devices Available
- 8-Pin and 14-Pin JEDEC SOIC, 8-Pin PDIP, and 8-Pin TSSOP Packages

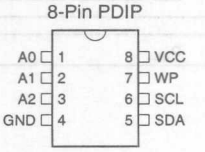
Description

The AT24C02A/04A/08A provides 2048/4096/8192 bits of serial electrically erasable and programmable read only memory (EEPROM) organized as 256/512/1024 words of 8 bits each. The device is optimized for use in many industrial and commercial applications where low power and low voltage operation are essential. The AT24C02A/04A/08A is available in space saving 8-pin PDIP, 8-pin and 14-pin JEDEC SOIC, and 8-pin TSSOP packages and is accessed via a 2-wire serial interface. In addition, the entire family is available in 5.0V (4.5V to 5.5V), 2.7V (2.7V to 5.5V), 2.5V (2.5V to 5.5V) and 1.8V (1.8V to 5.5V) versions.

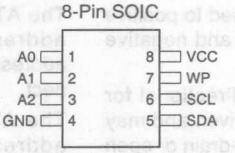
Pin Configurations

Pin Name	Function
A0 - A2	Address Inputs
SDA	Serial Data
SCL	Serial Clock Input
WP	Write Protect
NC	No Connect

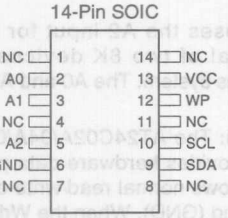
8-Pin PDIP



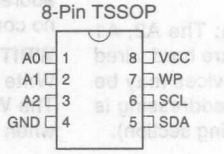
8-Pin SOIC



14-Pin SOIC



8-Pin TSSOP



2

2-Wire Serial EEPROM

2K (256 x 8)

4K (512 x 8)

8K (1024 x 8)

AT24C02A
AT24C04A
AT24C08A

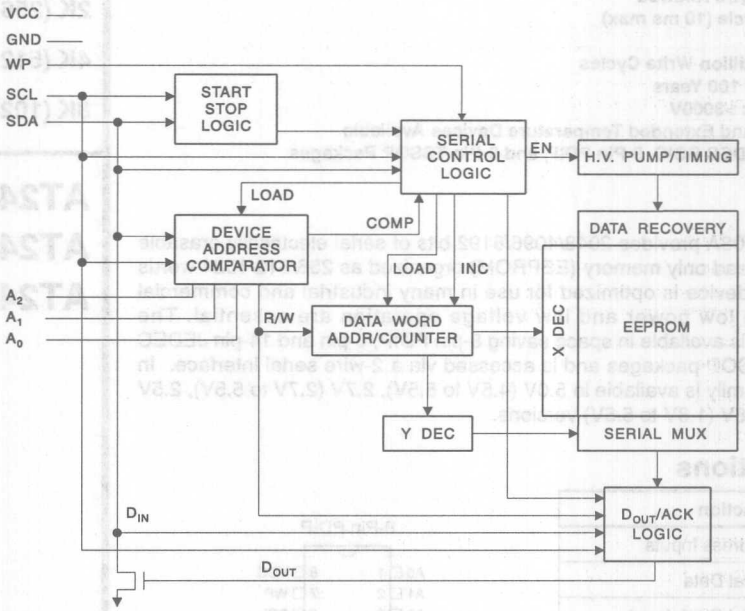
Rev. 0976B–07/98

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Block Diagram



Pin Description

SERIAL CLOCK (SCL): The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

SERIAL DATA (SDA): The SDA pin is bidirectional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open collector devices.

DEVICE/PAGE ADDRESSES (A2, A1, A0): The A2, A1 and A0 pins are device address inputs that are hard wired for the AT24C02A. As many as eight 2K devices may be addressed on a single bus system (device addressing is discussed in detail under the Device Addressing section).

The AT24C04A uses the A2 and A1 inputs for hard wire addressing and a total of four 4K devices may be addressed on a single bus system. The A0 pin is a no connect.

The AT24C08A only uses the A2 input for hardwire addressing and a total of two 8K devices may be addressed on a single bus system. The A0 and A1 pins are no connects.

WRITE PROTECT (WP): The AT24C02A/04A/08A has a Write Protect pin that provides hardware data protection. The Write Protect pin allows normal read/write operations when connected to ground (GND). When the Write Protect

pin is connected to V_{CC}, the write protection feature is enabled and operates as shown in the following table.

WP Pin Status	Part of the Array Protected		
	24C02A	24C04A	24C08A
At V_{CC}	Upper Half (1K) Array	Upper Half (2K) Array	Full (8K) Array
At GND	Normal Read/Write Operations		

Memory Organization

AT24C02A, 2K SERIAL EEPROM: Internally organized with 256 pages of 1-byte each, the 2K requires an 8 bit data word address for random word addressing.

AT24C04A, 4K SERIAL EEPROM: The 4K is internally organized with 256 pages of 2-bytes each. Random word addressing requires a 9 bit data word address.

AT24C08A, 8K SERIAL EEPROM: The 8K is internally organized with 4 blocks of 256 pages of 4-bytes each. Random word addressing requires a 10 bit data word address.

2

Pin Capacitance

Applicable over recommended operating range from T_A = 25°C, f = 1.0 MHz, V_{CC} = +1.8V.

Symbol	Test Condition	Max	Units	Conditions
$C_{I/O}$	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}	Input Capacitance (A_0, A_1, A_2, SCL)	6	pF	V_{IN} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

DC Characteristics

Applicable over recommended operating range from: T_{AI} = -40°C to +85°C, V_{CC} = +1.8V to +5.5V, T_{AC} = 0°C to +70°C, V_{CC} = +1.8V to +5.5V (unless otherwise noted).

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V_{CC1}	Supply Voltage		1.8		5.5	V
V_{CC2}	Supply Voltage		2.5		5.5	V
V_{CC3}	Supply Voltage		2.7		5.5	V
V_{CC4}	Supply Voltage		4.5		5.5	V
I_{CC}	Supply Current V_{CC} = 5.0V	READ at 100 kHz		0.4	1.0	mA
I_{CC}	Supply Current V_{CC} = 5.0V	WRITE at 100 kHz		2.0	3.0	mA
I_{SB1}	Standby Current V_{CC} = 1.8V	V_{IN} = V_{CC} or V_{SS}		0.6	3.0	µA
I_{SB2}	Standby Current V_{CC} = 2.5V	V_{IN} = V_{CC} or V_{SS}		1.4	4.0	µA
I_{SB3}	Standby Current V_{CC} = 2.7V	V_{IN} = V_{CC} or V_{SS}		1.6	4.0	µA
I_{SB4}	Standby Current V_{CC} = 5.0V	V_{IN} = V_{CC} or V_{SS}		8.0	18.0	µA
I_{LI}	Input Leakage Current	V_{IN} = V_{CC} or V_{SS}		0.10	3.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{CC} or V_{SS}		0.05	3.0	µA
V_{IL}	Input Low Level (1)		-0.6		V_{CC} x 0.3	V
V_{IH}	Input High Level (1)		V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL2}	Output Low Level V_{CC} = 3.0V	I_{OL} = 2.1 mA			0.4	V
V_{OL1}	Output Low Level V_{CC} = 1.8V	I_{OL} = 0.15 mA			0.2	V

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

AC Characteristics

Applicable over recommended operating range from T_A = -40°C to +85°C, V_{CC} = +1.8V to +5.5V, CL = 1 TTL Gate and 100 pF (unless otherwise noted).

Symbol	Parameter	2.7-, 2.5-, 1.8-volt		5.0-volt		Units
		Min	Max	Min	Max	
f_{SCL}	Clock Frequency, SCL		100		400	kHz
t_{LOW}	Clock Pulse Width Low	4.7		1.2		µs
t_{HIGH}	Clock Pulse Width High	4.0		0.6		µs
t_I	Noise Suppression Time(1)		100		50	ns
t_{AA}	Clock Low to Data Out Valid	0.1	4.5	0.1	0.9	µs
t_{BUF}	Time the bus must be free before a new transmission can start(1)	4.7		1.2		µs
$t_{HD.STA}$	Start Hold Time	4.0		0.6		µs
$t_{SU.STA}$	Start Set-up Time	4.7		0.6		µs
$t_{HD.DAT}$	Data In Hold Time	0		0		µs
$t_{SU.DAT}$	Data In Set-up Time	200		100		ns
t_R	Inputs Rise Time(1)		1.0		0.3	µs
t_F	Inputs Fall Time(1)		300		300	ns
$t_{SU.STO}$	Stop Set-up Time	4.7		0.6		µs
t_{DH}	Data Out Hold Time	100		50		ns
t_{WR}	Write Cycle Time		10		10	ms
Endurance(1)	5.0V, 25°C, Page Mode	1M		1M		Write Cycles

Note: 1. This parameter is characterized and is not 100% tested.

Device Operation

CLOCK and DATA TRANSITIONS: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (refer to Data Validity timing diagram). Data changes during SCL high periods will indicate a start or stop condition as defined below.

START CONDITION: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (refer to Start and Stop Definition timing diagram).

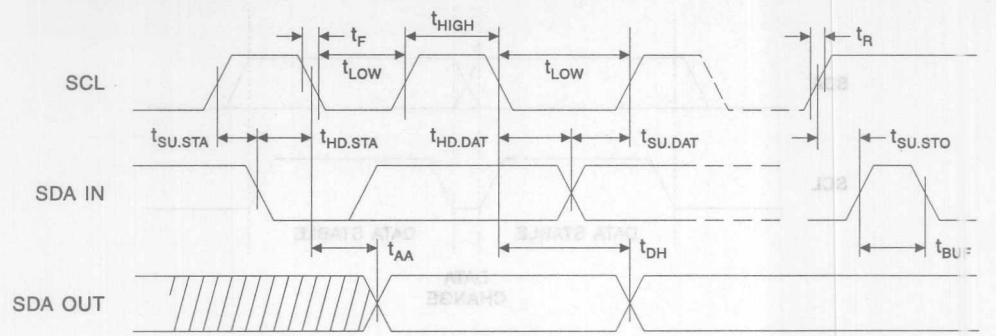
STOP CONDITION: A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode (refer to Start and Stop Definition timing diagram).

ACKNOWLEDGE: All addresses and data words are serially transmitted to and from the EEPROM in 8 bit words. The EEPROM sends a zero to acknowledge that it has received each word. This happens during the ninth clock cycle.

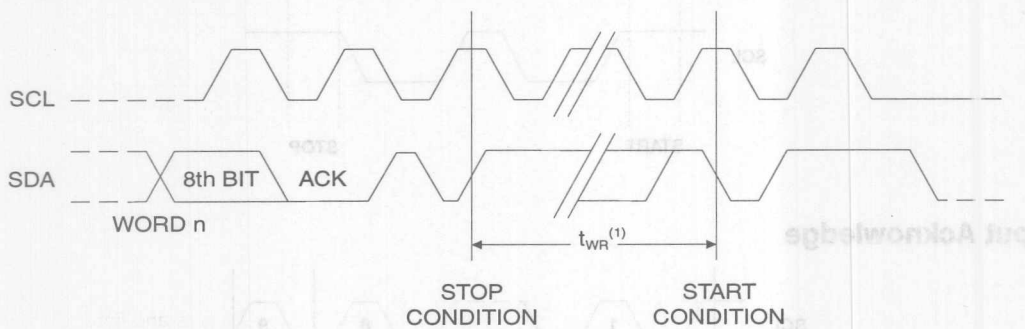
STANDBY MODE: The AT24C02A/04A/08A features a low power standby mode which is enabled: (a) upon power-up and (b) after the receipt of the STOP bit and the completion of any internal operations.

MEMORY RESET: After an interruption in protocol, power loss or system reset, any 2-wire part can be reset by following these steps:(a) Clock up to 9 cycles, (b) look for SDA high in each cycle while SCL is high and then (c) create a start condition as SDA is high.

Bus Timing (SCL: Serial Clock, SDA: Serial Data I/O)

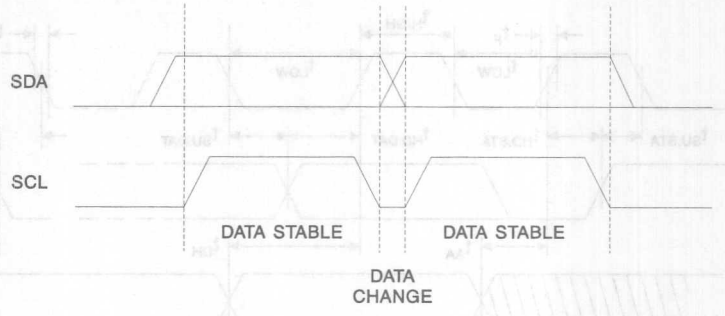


Write Cycle Timing (SCL: Serial Clock, SDA: Serial Data I/O)

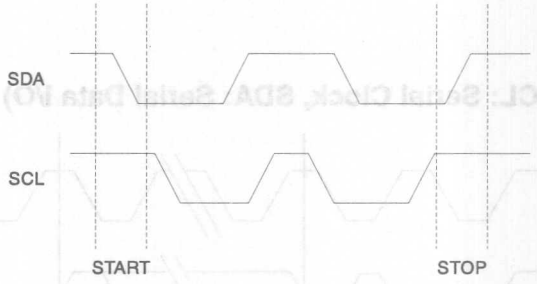


Note: 1. The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the interval clear/write cycle.

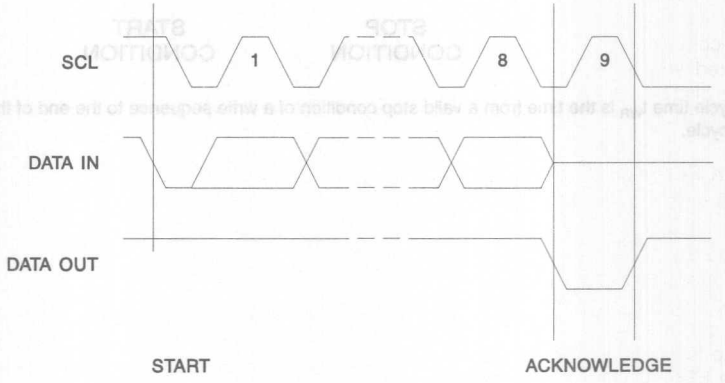
Data Validity



Start and Stop Definition



Output Acknowledge



Device Addressing

The 2K, 4K and 8K EEPROM devices all require an 8 bit device address word following a start condition to enable the chip for a read or write operation (refer to Figure 1).

The device address word consists of a mandatory one, zero sequence for the first four most significant bits as shown. This is common to all the EEPROM devices.

The next 3 bits are the A2, A1 and A0 device address bits for the 2K EEPROM. These 3 bits must compare to their corresponding hard-wired input pins.

The 4K EEPROM only uses the A2 and A1 device address bits with the third bit being a memory page address bit. The two device address bits must compare to their corresponding hard-wired input pins. The A0 pin is no connect.

The 8K EEPROM only uses the A2 device address bit with the next 2 bits being for memory page addressing. The A2 bit must compare to its corresponding hard-wired input pin. The A1 and A0 pins are no connect.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

Upon a compare of the device address, the EEPROM will output a zero. If a compare is not made, the chip will return to a standby state.

Write Operations

BYTE WRITE: A write operation requires an 8 bit data word address following the device address word and acknowledgement. Upon receipt of this address, the EEPROM will again respond with a zero and then clock in the first 8 bit data word. Following receipt of the 8 bit data word, the EEPROM will output a zero and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally-timed write cycle, t_{WR}, to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (refer to Figure 2).

PAGE WRITE: The 2K EEPROM is capable of an 8-byte page write, and the 4K and 8K devices are capable of 16-byte page writes.

A page write is initiated the same as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to seven (2K) or fifteen (4K, 8K) more data words. The EEPROM will respond with a zero after each data word received. The microcontroller must terminate the page write sequence with a stop condition (refer to Figure 3).

The data word address lower three (2K) or four (4K, 8K) bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than eight (2K) or sixteen (4K, 8K) data words are transmitted to the EEPROM, the data word address will "roll over" and previous data will be overwritten.

ACKNOWLEDGE POLLING: Once the internally-timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a zero allowing the read or write sequence to continue.

Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to one. There are three read operations: current address read, random address read and sequential read.

CURRENT ADDRESS READ: The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address "roll over" during read is from the last byte of the last memory page to the first byte of the first page. The address "roll over" during write is from the last byte of the current page to the first byte of the same page.

Once the device address with the read/write select bit set to one is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input zero but does generate a following stop condition (refer to Figure 4).

RANDOM READ: A random read requires a "dummy" byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a zero but does generate a following stop condition (refer to Figure 5).

SEQUENTIAL READ: Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds

with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will "roll over" and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a zero but does generate a following stop condition (refer to Figure 6).

Figure 1. Device Address

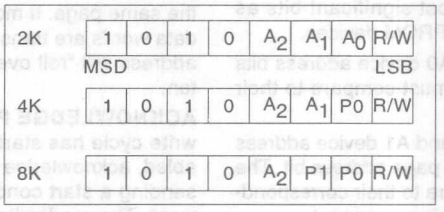


Figure 2. Byte Write

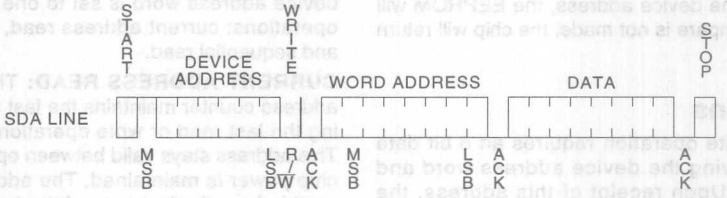


Figure 3. Page Write

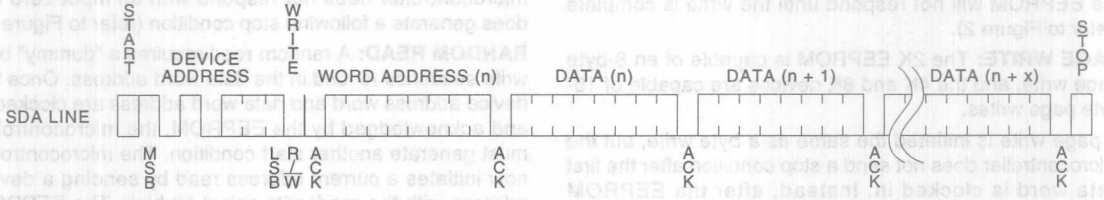


Figure 4. Current Address Read

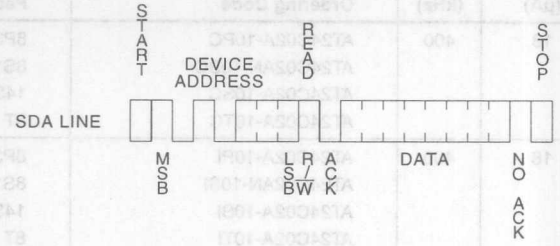


Figure 5. Random Read

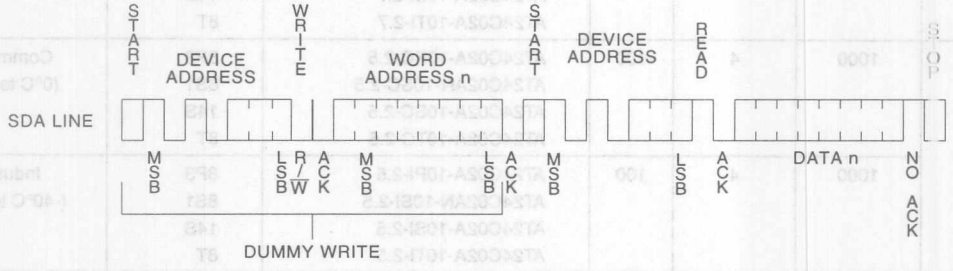
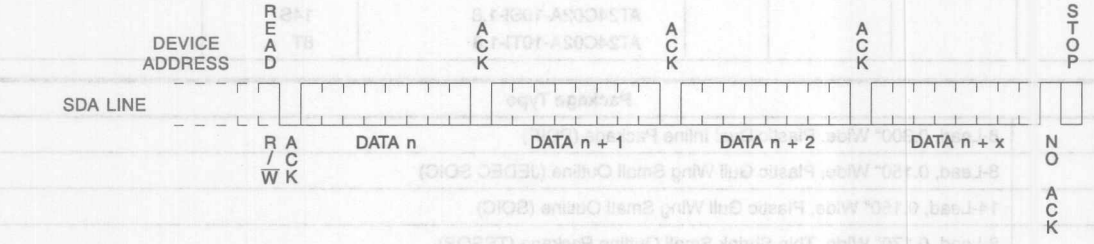


Figure 6. Sequential Read



AT24C02A Ordering Information

t_{WR} (max) (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	3000	18	400	AT24C02A-10PC AT24C02AN-10SC AT24C02A-10SC AT24C02A-10TC	8P3 8S1 14S 8T	Commercial (0°C to 70°C)
	3000	18	400	AT24C02A-10PI AT24C02AN-10SI AT24C02A-10SI AT24C02A-10TI	8P3 8S1 14S 8T	Industrial (-40°C to 85°C)
10	1500	4	100	AT24C02A-10PC-2.7 AT24C02AN-10SC-2.7 AT24C02A-10SC-2.7 AT24C02A-10TC-2.7	8P3 8S1 14S 8T	Commercial (0°C to 70°C)
	1500	4	100	AT24C02A-10PI-2.7 AT24C02AN-10SI-2.7 AT24C02A-10SI-2.7 AT24C02A-10TI-2.7	8P3 8S1 14S 8T	Industrial (-40°C to 85°C)
10	1000	4	100	AT24C02A-10PC-2.5 AT24C02AN-10SC-2.5 AT24C02A-10SC-2.5 AT24C02A-10TC-2.5	8P3 8S1 14S 8T	Commercial (0°C to 70°C)
	1000	4	100	AT24C02A-10PI-2.5 AT24C02AN-10SI-2.5 AT24C02A-10SI-2.5 AT24C02A-10TI-2.5	8P3 8S1 14S 8T	Industrial (-40°C to 85°C)
10	800	3	100	AT24C02A-10PC-1.8 AT24C02AN-10SC-1.8 AT24C02A-10SC-1.8 AT24C02A-10TC-1.8	8P3 8S1 14S 8T	Commercial (0°C to 70°C)
	800	3	100	AT24C02A-10PI-1.8 AT24C02AN-10SI-1.8 AT24C02A-10SI-1.8 AT24C02A-10TI-1.8	8P3 8S1 14S 8T	Industrial (-40°C to 85°C)

Package Type	
8P3	8-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
14S	14-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (SOIC)
8T	8-Lead, 0.170" Wide, Thin Shrink Small Outline Package (TSSOP)
Options	
Blank	Standard Operation (4.5V to 5.5V)
-2.7	Low-Voltage (2.7V to 5.5V)
-2.5	Low-Voltage (2.5V to 5.5V)
-1.8	Low-Voltage (1.8V to 5.5V)

AT24C04A Ordering Information

t_{WR} (max) (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	3000	18	400	AT24C04A-10PC AT24C04AN-10SC AT24C04A-10SC AT24C04A-10TC	8P3 8S1 14S 8T	Commercial (0°C to 70°C)
	3000	18	400	AT24C04A-10PI AT24C04AN-10SI AT24C04A-10SI AT24C04A-10TI	8P3 8S1 14S 8T	Industrial (-40°C to 85°C)
10	1500	4	100	AT24C04A-10PC-2.7 AT24C04AN-10SC-2.7 AT24C04A-10SC-2.7 AT24C04A-10TC	8P3 8S1 14S 8T	Commercial (0°C to 70°C)
	1500	4	100	AT24C04A-10PI-2.7 AT24C04AN-10SI-2.7 AT24C04A-10SI-2.7 AT24C04A-10TI-2.7	8P3 8S1 14S 8T	Industrial (-40°C to 85°C)
10	1000	4	100	AT24C04A-10PC-2.5 AT24C04AN-10SC-2.5 AT24C04A-10SC-2.5 AT24C04A-10TC-2.5	8P3 8S1 14S 8T	Commercial (0°C to 70°C)
	1000	4	100	AT24C04A-10PI-2.5 AT24C04AN-10SI-2.5 AT24C04A-10SI-2.5 AT24C04A-10TI-2.5	8P3 8S1 14S 8T	Industrial (-40°C to 85°C)
10	800	3	100	AT24C04A-10PC-1.8 AT24C04AN-10SC-1.8 AT24C04A-10SC-1.8 AT24C04A-10TC-1.8	8P3 8S1 14S 8T	Commercial (0°C to 70°C)
	800	3	100	AT24C04A-10PI-1.8 AT24C04AN-10SI-1.8 AT24C04A-10SI-1.8 AT24C04A-10TI-1.8	8P3 8S1 14S 8T	Industrial (-40°C to 85°C)

Package Type	
8P3	8-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
14S	14-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (SOIC)
8T	8-Lead, 0.170" Wide, Thin Shrink Small Outline Package (TSSOP)
Options	
Blank	Standard Operation (4.5V to 5.5V)
-2.7	Low-Voltage (2.7V to 5.5V)
-2.5	Low-Voltage (2.5V to 5.5V)
-1.8	Low-Voltage (1.8V to 5.5V)

AT24C08A Ordering Information

t_{WR} (max) (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	3000	18	400	AT24C08A-10PC AT24C08AN-10SC AT24C08A-10SC AT24C08A-10TC	8P3 8S1 14S 8T	Commercial (0°C to 70°C)
	3000	18	400	AT24C08A-10PI AT24C08AN-10SI AT24C08A-10SI AT24C08A-10TI	8P3 8S1 14S 8T	Industrial (-40°C to 85°C)
10	1500	4	100	AT24C08A-10PC-2.7 AT24C08AN-10SC-2.7 AT24C08A-10SC-2.7 AT24C08A-10TC-2.7	8P3 8S1 14S 8T	Commercial (0°C to 70°C)
	1500	4	100	AT24C08A-10PI-2.7 AT24C08AN-10SI-2.7 AT24C08A-10SI-2.7 AT24C08A-10TI-2.7	8P3 8S1 14S 8T	Industrial (-40°C to 85°C)
10	1000	4	100	AT24C08A-10PC-2.5 AT24C08AN-10SC-2.5 AT24C08A-10SC-2.5 AT24C08A-10TC-2.5	8P3 8S1 14S 8T	Commercial (0°C to 70°C)
	1000	4	100	AT24C08A-10PI-2.5 AT24C08AN-10SI-2.5 AT24C08A-10SI-2.5 AT24C08A-10TI-2.5	8P3 8S1 14S 8T	Industrial (-40°C to 85°C)
10	800	3	100	AT24C08A-10PC-1.8 AT24C08AN-10SC-1.8 AT24C08A-10SC-1.8 AT24C08A-10TC-1.8	8P3 8S1 14S 8T	Commercial (0°C to 70°C)
	800	3	100	AT24C08A-10PI-1.8 AT24C08AN-10SI-1.8 AT24C08A-10SI-1.8 AT24C08A-10TI-1.8	8P3 8S1 14S 8T	Industrial (-40°C to 85°C)

Package Type	
8P3	8-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
14S	14-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (SOIC)
8T	8-Lead, 0.170" Wide, Thin Shrink Small Outline Package (TSSOP)
Options	
Blank	Standard Operation (4.5V to 5.5V)
-2.7	Low-Voltage (2.7V to 5.5V)
-2.5	Low-Voltage (2.5V to 5.5V)
-1.8	Low-Voltage (1.8V to 5.5V)

2-Wire Serial EEPROM

16K (2048 x 8)

AT24C164

Features

- Low Voltage and Standard Voltage Operation
  - 5.0 (V_{CC} = 4.5V to 5.5V)
  - 2.7 (V_{CC} = 2.7V to 5.5V)
  - 2.5 (V_{CC} = 2.5V to 5.5V)
  - 1.8 (V_{CC} = 1.8V to 5.5V)
- Internally Organized 2048 x 8 (16K)
- 2-Wire Serial Interface
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- Bidirectional Data Transfer Protocol
- 100 kHz (1.8V, 2.5V, 2.7V) and 400 kHz (5V) Compatibility
- Write Protect Pin for Hardware Data Protection
- Cascadable Feature Allows for Extended Densities
- 16-Byte Page Write Mode
- Partial Page Writes Are Allowed
- Self-Timed Write Cycle (10 ms max)
- High Reliability
  - Endurance: 1 Million Write Cycles
  - Data Retention: 100 Years
  - ESD Protection: >3,000V
- Automotive Grade and Extended Temperature Devices Available
- 8-Pin JEDEC SOIC and 8-Pin PDIP Packages

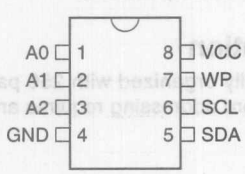
Description

The AT24C164 provides 16,384 bits of serial electrically erasable and programmable read only memory (EEPROM) organized as 2048 words of 8 bits each. The device's cascadable feature allows up to eight devices to share a common 2-wire bus. The device is optimized for use in many industrial and commercial applications where low power and low voltage operation are essential. The AT24C164 is available in space saving 8-pin PDIP and 8-pin SOIC packages and is accessed via a 2-wire serial interface. In addition, this device is available in 5.0V (4.5V to 5.5V), 2.7V (2.7V to 5.5V), 2.5V (2.5V to 5.5V) and 1.8V (1.8V to 5.5V) versions.

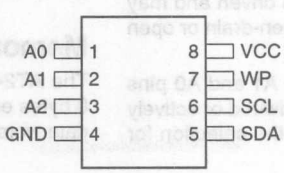
Pin Configurations

Pin Name	Function
A0 - A2	Address Inputs
SDA	Serial Data
SCL	Serial Clock Input
WP	Write Protect

8-Pin PDIP



8-Pin SOIC



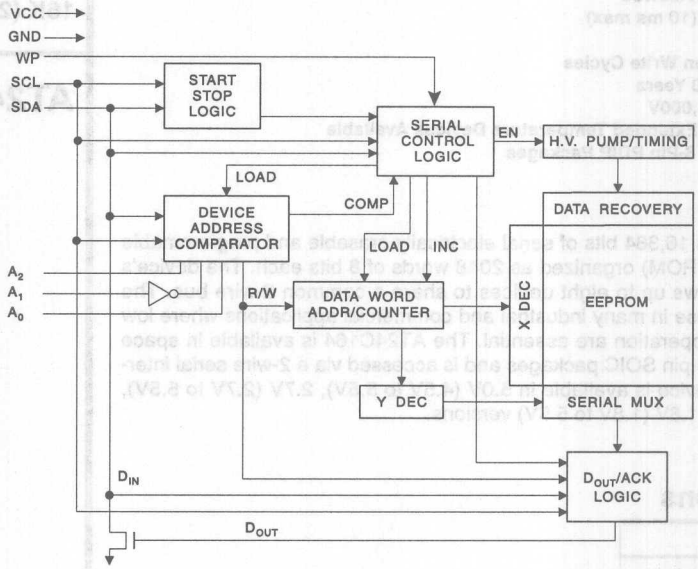
Rev. 0105D–07/98

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Block Diagram



Pin Description

SERIAL CLOCK (SCL): The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

SERIAL DATA (SDA): The SDA pin is bidirectional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open collector devices.

DEVICE SELECT (A2, A1, A0): The A2, A1 and A0 pins are device address inputs that may be hardwired or actively driven to V_{DD} or V_{SS}. These inputs allow the selection for one of eight possible devices sharing a common bus. The AT24C164 can be made compatible with the AT24C16 by tying A2, A1 and A0 to V_{SS}. Device addressing is discussed in detail in the device addressing section.

WRITE PROTECT (WP): The write protect input, when tied low to GND, allows normal write operations.

Memory Organization

The AT24C164 is internally organized with 256 pages of 8 bytes each. Random word addressing requires an 11 bit data word address.

Pin Capacitance[1]

Applicable over recommended operating range from T_A = 25°C, f = 1.0 MHz, V_{CC} = +1.8V.

Symbol	Test Condition	Max	Units	Conditions
$C_{I/O}$	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}	Input Capacitance (A_0, A_1, A_2, SCL)	6	pF	V_{IN} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

2

DC Characteristics

Applicable over recommended operating range from: T_{AI} = -40°C to +85°C, V_{CC} = +1.8V to +5.5V, T_{AC} = 0°C to +70°C, V_{CC} = +1.8V to +5.5V (unless otherwise noted).

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V_{CC1}	Supply Voltage		1.8		5.5	V
V_{CC2}	Supply Voltage		2.5		5.5	V
V_{CC3}	Supply Voltage		2.7		5.5	V
V_{CC4}	Supply Voltage		4.5		5.5	V
I_{CC}	Standby Current V_{CC} = 5.0V	READ at 100 kHz		0.4	1.0	mA
I_{CC}	Standby Current V_{CC} = 5.0V	WRITE at 100 kHz		2.0	3.0	mA
I_{SB1}	Standby Current V_{CC} = 1.8V	V_{IN} = V_{CC} or V_{SS}		0.6	3.0	µA
I_{SB2}	Standby Current V_{CC} = 2.5V	V_{IN} = V_{CC} or V_{SS}		1.4	4.0	µA
I_{SB3}	Standby Current V_{CC} = 2.7V	V_{IN} = V_{CC} or V_{SS}		1.6	4.0	µA
I_{SB4}	Standby Current V_{CC} = 5.0V	V_{IN} = V_{CC} or V_{SS}		8.0	18.0	µA
I_{LI}	Input Leakage Current	V_{IN} = V_{CC} or V_{SS}		0.10	3.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{CC} or V_{SS}		0.05	3.0	µA
V_{IL}	Input Low Level[1]		-0.6		V_{CC} x 0.3	V
V_{IH}	Input High Level[1]		V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL2}	Output Low Level V_{CC} = 3.0V	I_{OL} = 2.1 mA			0.4	V
V_{OL1}	Output Low Level V_{CC} = 1.8V	I_{OL} = 0.15 mA			0.2	V

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

AC Characteristics

Applicable over recommended operating range from T_A = -40°C to +85°C, V_{CC} = +1.8V to +5.5V, CL = 1 TTL Gate and 100 pF (unless otherwise noted).

Symbol	Parameter	2.7-, 2.5-, 1.8-volt		5.0-volt		Units
		Min	Max	Min	Max	
f_{SCL}	Clock Frequency, SCL		100		400	kHz
t_{LOW}	Clock Pulse Width Low	4.7		1.2		µs
t_{HIGH}	Clock Pulse Width High	4.0		0.6		µs
t_I	Noise Suppression Time(1)		100		50	ns
t_{AA}	Clock Low to Data Out Valid	0.1	4.5	0.1	0.9	µs
t_{BUF}	Time the bus must be free before a new transmission can start(1)	4.7		1.2		µs
$t_{HD.STA}$	Start Hold Time	4.0		0.6		µs
$t_{SU.STA}$	Start Set-up Time	4.7		0.6		µs
$t_{HD.DAT}$	Data In Hold Time	0		0		µs
$t_{SU.DAT}$	Data In Set-up Time	200		100		ns
t_R	Inputs Rise Time(1)		1.0		0.3	µs
t_F	Inputs Fall Time(1)		300		300	ns
$t_{SU.STO}$	Stop Set-up Time	4.7		0.6		µs
t_{DH}	Data Out Hold Time	100		50		ns
t_{WR}	Write Cycle Time		10		10	ms
Endurance(1)	5.0V, 25°C, Page Mode	1M		1M		Write cycles

Notes: 1. This parameter is characterized and is not 100% tested.

Device Operation

CLOCK and DATA TRANSITIONS: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (refer to Data Validity timing diagram). Data changes during SCL high periods will indicate a start or stop condition as defined below.

START CONDITION: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (refer to Start and Stop Definition timing diagram).

STOP CONDITION: A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode (refer to Start and Stop Definition timing diagram).

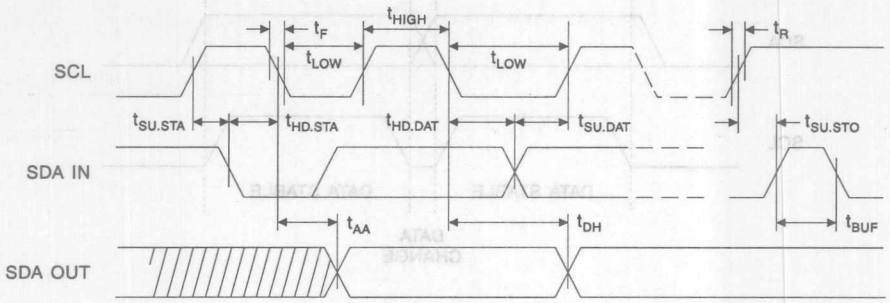
ACKNOWLEDGE: All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a zero to acknowledge that it has received each word. This happens during the ninth clock cycle.

STANDBY MODE: The AT24C164 features a low power standby mode which is enabled: a) upon power-up and b) after the receipt of the STOP bit and the completion of any internal operations.

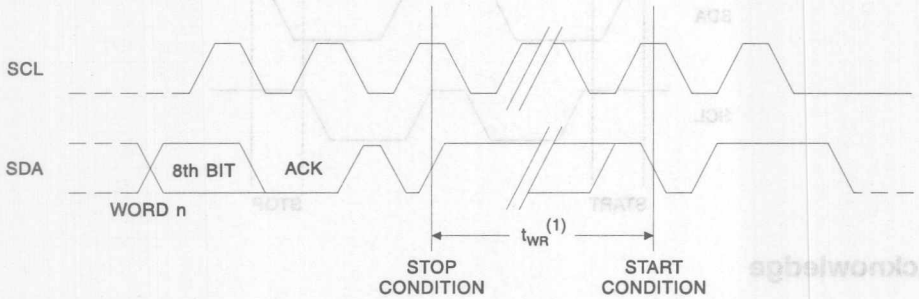
MEMORY RESET: After an interruption in protocol, power loss or system reset, the AT24C164 can be reset by following these steps:

(a) Clock up to 9 cycles, (b) look for SDA high in each cycle while SCL is high and then (c) create a start condition as SDA is high.

Bus Timing
SCL: Serial Clock, SDA: Serial Data I/O

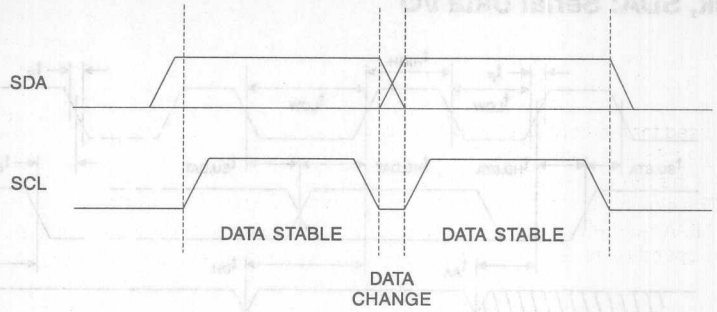


Write Cycle Timing
SCL: Serial Clock, SDA: Serial Data I/O

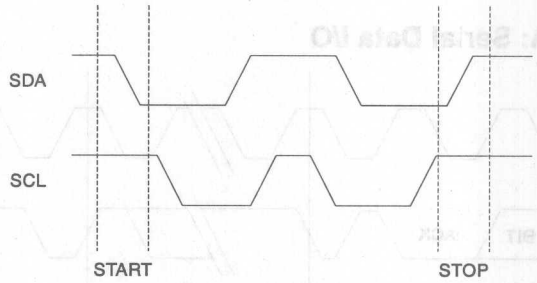


Note: 1. The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

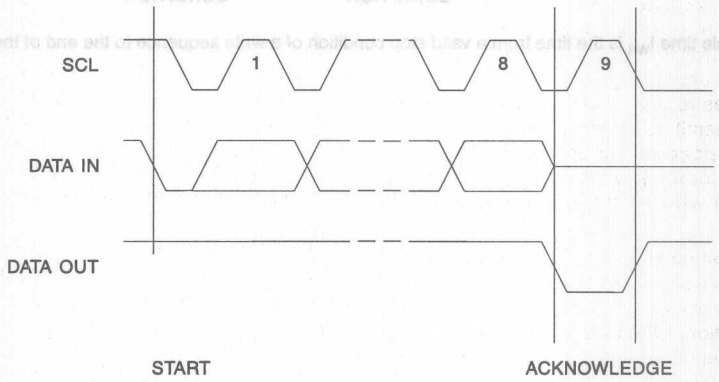
Data Validity



Start and Stop Definition



Output Acknowledge



Device Addressing

The AT24C164 requires an 8-bit device address word following a start condition to enable the chip for read or write operations (refer to Figure 1). The most significant bit must be a one followed by the A2, A1 and A0 device select bits (the A1 bit must be the compliment of the A1 input pin signal). The next 3 bits are used for memory block addressing and select one of the eight 256 x 8 memory blocks. These bits should be considered the three most significant bits of the data word address. The eighth bit of the device address is the read/write select bit. A read operation is selected if this bit is high or a write operation is selected if this bit is low.

Upon a compare of the device address, the EEPROM will output a zero. If a compare is not made, the chip will return to a standby state.

Write Operations

BYTE WRITE: A write operation requires an 8-bit data word address following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a zero and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a zero and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally-timed write cycle, t_{WR}, to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (refer to Figure 2).

PAGE WRITE: The AT24C164 is capable of a 16-byte page write. A page write is initiated the same as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to fifteen more data words. The EEPROM will respond with a zero after each data word received. The microcontroller must terminate the page write sequence with a stop condition (refer to Figure 3).

The data word address lower 4 bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than sixteen data words are transmitted to the EEPROM, the data word address will "roll over" and previous data will be overwritten.

ACKNOWLEDGE POLLING: Once the internally-timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a zero allowing the read or write sequence to continue.

2

Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to one. There are three read operations: current address read, random address read and sequential read.

CURRENT ADDRESS READ: The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address "roll over" during read is from the last byte of the last memory page to the first byte of the first page. The address "roll over" during write is from the last byte of the current page to first byte of the same page.

Once the device address with the read/write select bit set to one is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input zero but does generate a following stop condition (refer to Figure 4).

RANDOM READ: A random read requires a "dummy" byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a zero but does generate a following stop condition (refer to Figure 5).

SEQUENTIAL READ: Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will "roll over" and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a zero but does generate a following stop condition (refer to Figure 6).

Figure 1. Device Address

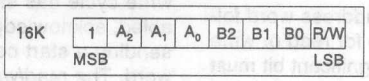


Figure 2. Byte Write

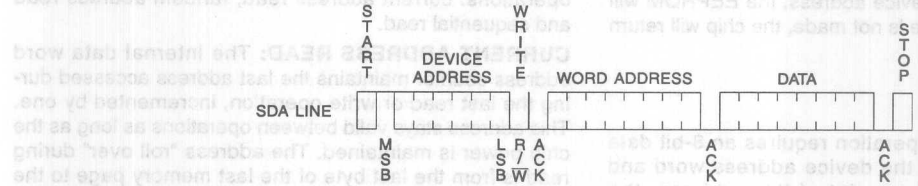


Figure 3. Page Write

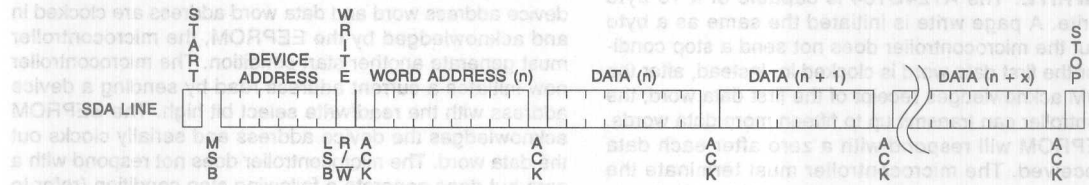


Figure 4. Current Address Read

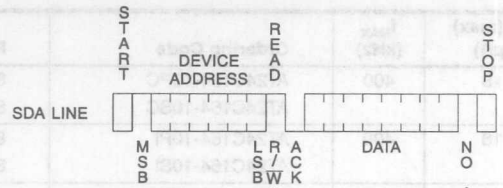


Figure 5. Random Read

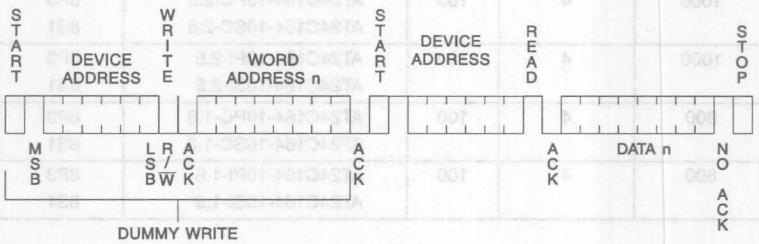
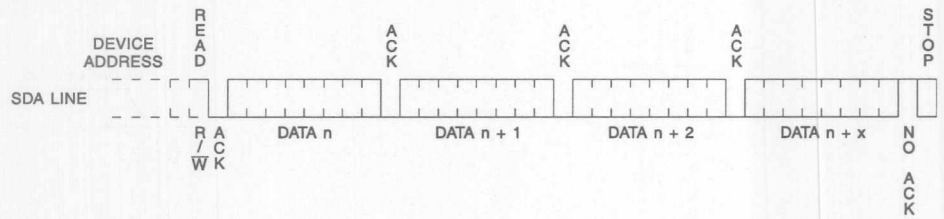


Figure 6. Sequential Read



Ordering Information

t_{WR} (max) (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	3000	18	400	AT24C164-10PC AT24C164-10SC	8P3 8S1	Commercial (0°C to 70°C)
	3000	18	400	AT24C164-10PI AT24C164-10SI	8P3 8S1	Industrial (-40°C to 85°C)
10	1500	4	100	AT24C164-10PC-2.7 AT24C164-10SC-2.7	8P3 8S1	Commercial (0°C to 70°C)
	1500	4	100	AT24C164-10PI-2.7 AT24C164-10SI-2.7	8P3 8S1	Industrial (-40°C to 85°C)
10	1000	4	100	AT24C164-10PC-2.5 AT24C164-10SC-2.5	8P3 8S1	Commercial (0°C to 70°C)
	1000	4	100	AT24C164-10PI-2.5 AT24C164-10SI-2.5	8P3 8S1	Industrial (-40°C to 85°C)
10	800	4	100	AT24C164-10PC-1.8 AT24C164-10SC-1.8	8P3 8S1	Commercial (0°C to 70°C)
	800	4	100	AT24C164-10PI-1.8 AT24C164-10SI-1.8	8P3 8S1	Industrial (-40°C to 85°C)

Package Type	
8P3	8 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8 Lead, 0.150" Wide, Plastic Gull Wing Small Outline Package (JEDEC SOIC)
Options	
Blank	Standard Operation (4.5V to 5.5V)
-2.7	Low-Voltage (2.7V to 5.5V)
-2.5	Low-Voltage (2.5V to 5.5V)
-1.8	Low-Voltage (1.8V to 5.5V)

Features

- Low-Voltage and Standard-Voltage Operation
  - 5.0 (V_{CC} = 4.5V to 5.5V)
  - 2.7 (V_{CC} = 2.7V to 5.5V)
  - 2.5 (V_{CC} = 2.5V to 5.5V)
  - 1.8 (V_{CC} = 1.8V to 5.5V)
- Low-Power Devices (I_{SB} = 2 µA @ 5.5V) Available
- Internally Organized 4096 x 8, 8192 x 8
- 2-Wire Serial Interface
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- Bidirectional Data Transfer Protocol
- 100 kHz (1.8V, 2.5V, 2.7V) and 400 kHz (5V) Compatibility
- Write Protect Pin for Hardware Data Protection
- 32-Byte Page Write Mode (Partial Page Writes Allowed)
- Self-Timed Write Cycle (10 ms max)
- High Reliability
  - Endurance: 1 Million Write Cycles
  - Data Retention: 100 Years
  - ESD Protection: >3,000V
- Automotive Grade and Extended Temperature Devices Available
- 8-Pin JEDEC PDIP, 8-Pin and 14-Pin JEDEC SOIC, 8-Pin EIAJ SOIC, and 8-pin TSSOP Packages

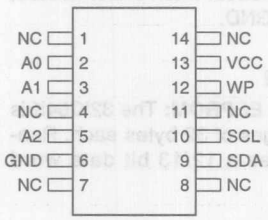
Description

The AT24C32/64 provides 32,768/65,536 bits of serial electrically erasable and programmable read only memory (EEPROM) organized as 4096/8192 words of 8 bits each. The device's cascadable feature allows up to 8 devices to share a common 2-wire bus. The device is optimized for use in many industrial and commercial applications where low power and low voltage operation are essential. The AT24C32/64 is available in space saving 8-pin JEDEC PDIP, 8-pin and 14-pin JEDEC SOIC, 8-pin EIAJ SOIC, and 8-pin TSSOP packages and is accessed via a 2-wire serial interface. In addition, the entire family is available in 5.0V (4.5V to 5.5V), 2.7V (2.7V to 5.5V), 2.5V (2.5V to 5.5V) and 1.8V (1.8V to 5.5V) versions.

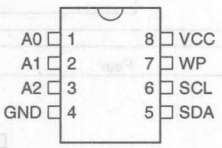
Pin Configurations

Pin Name	Function
A0 - A2	Address Inputs
SDA	Serial Data
SCL	Serial Clock Input
WP	Write Protect

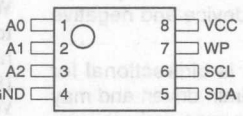
14-Pin SOIC



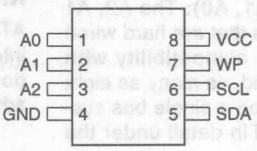
8-Pin PDIP



8-Pin TSSOP



8-Pin SOIC



ATMEL

2

2-Wire Serial EEPROM

32K (4096 x 8)

64K (8192 x 8)

AT24C32
AT24C64

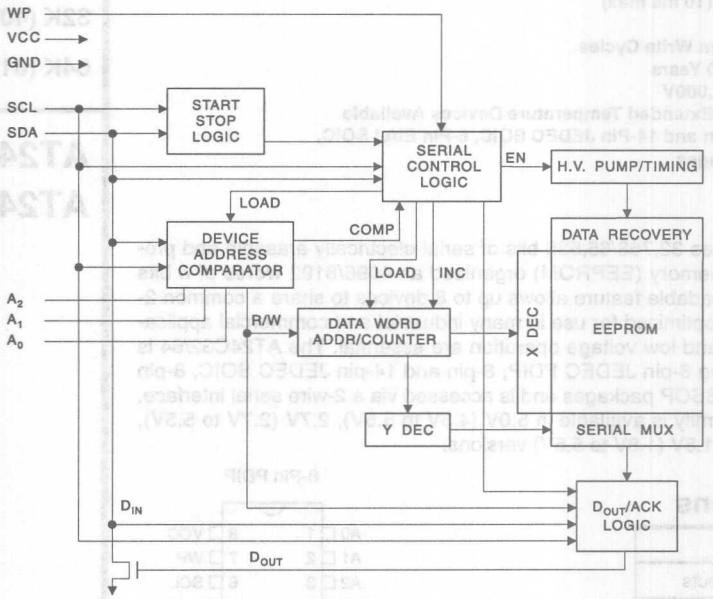
Rev. 0336F–08/98

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Block Diagram



Pin Description

SERIAL CLOCK (SCL): The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

SERIAL DATA (SDA): The SDA pin is bidirectional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open collector devices.

DEVICE/PAGE ADDRESSES (A2, A1, A0): The A2, A1 and A0 pins are device address inputs that are hard wired or left not connected for hardware compatibility with AT24C16. When the pins are hardwired, as many as eight 32K/64K devices may be addressed on a single bus system (device addressing is discussed in detail under the Device Addressing section). When the pins are not hardwired, the default A_2, A_1, and A_0 are zero.

WRITE PROTECT (WP): The write protect input, when tied to GND, allows normal write operations. When WP is tied high to V_{CC}, all write operations to the upper quandrant (8/16K bits) of memory are inhibited. If left unconnected, WP is internally pulled down to GND.

Memory Organization

AT24C32/64, 32K/64K SERIAL EEPROM: The 32K/64K is internally organized as 256 pages of 32 bytes each. Random word addressing requires a 12/13 bit data word address.

Pin Capacitance[1]

Applicable over recommended operating range from T_A = 25°C, f = 1.0 MHz, V_{CC} = +1.8V.

Symbol	Test Condition	Max	Units	Conditions
$C_{I/O}$	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}	Input Capacitance (A_0, A_1, A_2, SCL)	6	pF	V_{IN} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

DC Characteristics

Applicable over recommended operating range from: T_{AI} = -40°C to +85°C, V_{CC} = +1.8V to +5.5V, T_{AC} = 0°C to +70°C, V_{CC} = +1.8V to +5.5V (unless otherwise noted).

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
V_{CC1}	Supply Voltage			1.8		5.5	V
V_{CC2}	Supply Voltage			2.5		5.5	V
V_{CC3}	Supply Voltage			2.7		5.5	V
V_{CC4}	Supply Voltage			4.5		5.5	V
I_{CC1}	Supply Current	V_{CC} = 5.0V	READ at 100 kHz		0.4	1.0	mA
I_{CC2}	Supply Current	V_{CC} = 5.0V	WRITE at 100 kHz		2.0	3.0	mA
I_{SB1}	Standby Current (1.8V option)	V_{CC} = 1.8V	V_{IN} = V_{CC} or V_{SS}			0.1	µA
		V_{CC} = 5.5V				2.0	
I_{SB2}	Standby Current (2.5V option)	V_{CC} = 2.5V	V_{IN} = V_{CC} or V_{SS}			0.5	µA
		V_{CC} = 5.5V				2.0	
I_{SB3}	Standby Current (2.7V option)	V_{CC} = 2.7V	V_{IN} = V_{CC} or V_{SS}			0.5	µA
		V_{CC} = 5.5V				2.0	
I_{SB4}	Standby Current (5V option)	V_{CC} = 4.5 - 5.5V	V_{IN} = V_{CC} or V_{SS}		20	35	µA
I_{LI}	Input Leakage Current	V_{IN} = V_{CC} or V_{SS}			0.10	3.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{CC} or V_{SS}			0.05	3.0	µA
V_{IL}	Input Low Level[1]			-0.6		V_{CC} x 0.3	V
V_{IH}	Input High Level[1]			V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL2}	Output Low Level	V_{CC} = 3.0V	I_{OL} = 2.1 mA			0.4	V
V_{OL1}	Output Low Level	V_{CC} = 1.8V	I_{OL} = 0.15 mA			0.2	V

Notes: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

AC Characteristics

Applicable over recommended operating range from T_A = -40°C to +85°C, V_{CC} = +1.8V to +5.5V, CL = 1 TTL Gate and 100 pF (unless otherwise noted).

Symbol	Parameter	1.8-volt		2.7-, 2.5-volt		5.0-volt		Units
		Min	Max	Min	Max	Min	Max	
f_{SCL}	Clock Frequency, SCL		100		100		400	kHz
t_{LOW}	Clock Pulse Width Low	4.7		4.7		1.2		µs
t_{HIGH}	Clock Pulse Width High	4.0		4.0		0.6		µs
t_I	Noise Suppression Time(1)		100		100		50	ns
t_{AA}	Clock Low to Data Out Valid	0.1	4.5	0.1	4.5	0.1	0.9	µs
t_{BUF}	Time the bus must be free before a new transmission can start(1)	4.7		4.7		1.2		µs
$t_{HD.STA}$	Start Hold Time	4.0		4.0		0.6		µs
$t_{SU.STA}$	Start Set-up Time	4.7		4.7		0.6		µs
$t_{HD.DAT}$	Data In Hold Time	0		0		0		µs
$t_{SU.DAT}$	Data In Set-up Time	200		200		100		ns
t_R	Inputs Rise Time(1)		1.0		1.0		0.3	µs
t_F	Inputs Fall Time(1)		300		300		300	ns
$t_{SU.STO}$	Stop Set-up Time	4.7		4.7		0.6		µs
t_{DH}	Data Out Hold Time	100		100		50		ns
t_{WR}	Write Cycle Time		20		10		10	ms
Endurance(1)	5.0V, 25°C, Page Mode	1M		1M		1M		Write Cycles

Note: 1. This parameter is characterized and is not 100% tested.

Device Operation

CLOCK and DATA TRANSITIONS: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (refer to Data Validity timing diagram). Data changes during SCL high periods will indicate a start or stop condition as defined below.

START CONDITION: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (refer to Start and Stop Definition timing diagram).

STOP CONDITION: A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode (refer to Start and Stop Definition timing diagram).

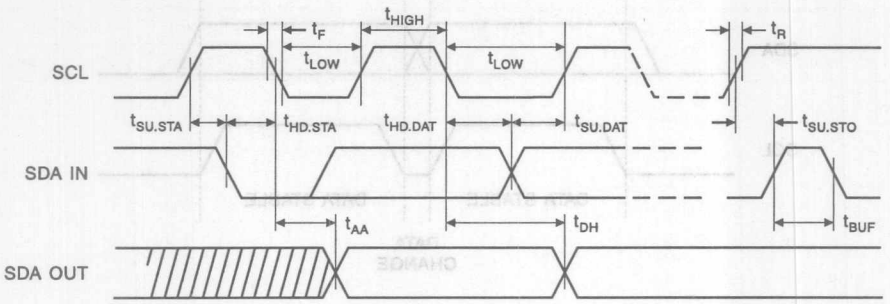
ACKNOWLEDGE: All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a zero during the ninth clock cycle to acknowledge that it has received each word.

STANDBY MODE: The AT24C32/64 features a low power standby mode which is enabled: a) upon power-up and b) after the receipt of the STOP bit and the completion of any internal operations.

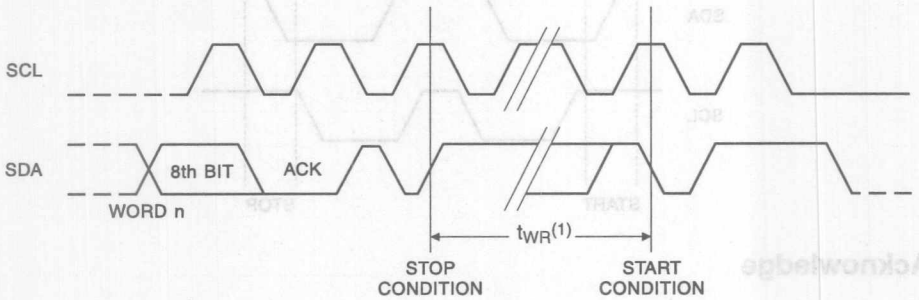
MEMORY RESET: After an interruption in protocol, power loss or system reset, any 2-wire part can be reset by following these steps:

(a) Clock up to 9 cycles, (b) look for SDA high in each cycle while SCL is high and then (c) create a start condition as SDA is high.

Bus Timing
SCL: Serial Clock, SDA: Serial Data I/O

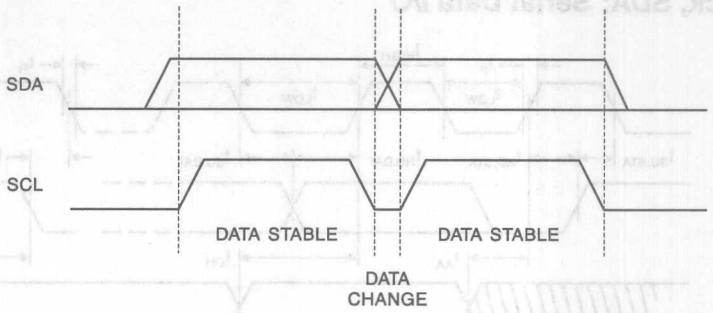


Write Cycle Timing
SCL: Serial Clock, SDA: Serial Data I/O

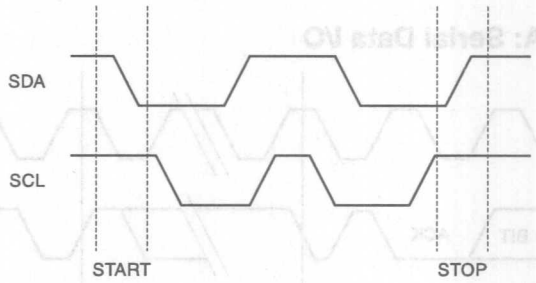


Note: 1. The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the internal clea /write cycle.

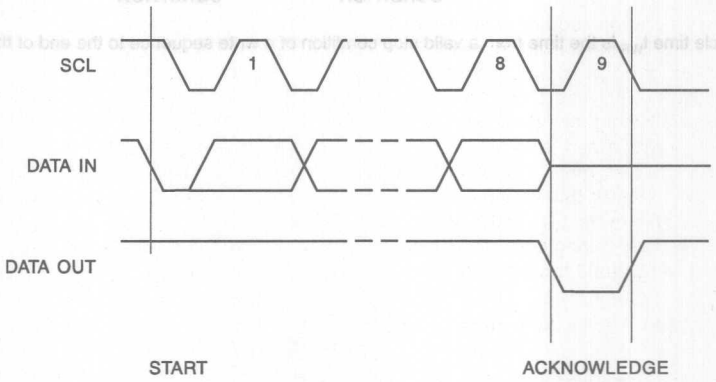
Data Validity



Start and Stop Definition



Output Acknowledge



Device Addressing

The 32K/64K EEPROM requires an 8-bit device address word following a start condition to enable the chip for a read or write operation (refer to Figure 1). The device address word consists of a mandatory one, zero sequence for the first four most significant bits as shown. This is common to all 2-wire EEPROM devices.

The 32K/64K uses the three device address bits A2, A1, A0 to allow as many as eight devices on the same bus. These bits must compare to their corresponding hardwired input pins. The A2, A1, and A0 pins use an internal proprietary circuit that biases them to a logic low condition if the pins are allowed to float.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

Upon a compare of the device address, the EEPROM will output a zero. If a compare is not made, the device will return to standby state.

NOISE PROTECTION: Special internal circuitry placed on the SDA and SCL pins prevent small noise spikes from activating the device. A low-V_{CC} detector (5-volt option) resets the device to prevent data corruption in a noisy environment.

DATA SECURITY: The AT24C32/64 has a hardware data protection scheme that allows the user to write protect the upper quadrant (8/16K bits) of memory when the WP pin is at V_{CC}.

Write Operations

BYTE WRITE: A write operation requires two 8-bit data word addresses following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a zero and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a zero and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally-timed write cycle, t_{WR}, to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (refer to Figure 2).

PAGE WRITE: The 32K/64K EEPROM is capable of 32-byte page writes.

A page write is initiated the same way as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to 31 more data words. The EEPROM will respond with a zero after each data word received. The microcontroller must terminate the page write sequence with a stop condition (refer to Figure 3).

The data word address lower 5 bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than 32 data words are transmitted to the EEPROM, the data word address will "roll over" and previous data will be overwritten.

ACKNOWLEDGE POLLING: Once the internally-timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a zero, allowing the read or write sequence to continue.

Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to one. There are three read operations: current address read, random address read and sequential read.

CURRENT ADDRESS READ: The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address "roll over" during read is from the last byte of the last memory page, to the first byte of the first page. The address "roll over" during write is from the last byte of the current page to the first byte of the same page.

Once the device address with the read/write select bit set to one is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input zero but does generate a following stop condition (refer to Figure 4).

RANDOM READ: A random read requires a "dummy" byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a zero but does generate a following stop condition (refer to Figure 5).

SEQUENTIAL READ: Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an

acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will "roll over" and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a zero but does generate a following stop condition (refer to Figure 6).

Figure 1. Device Address

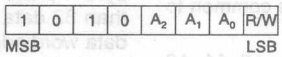


Figure 2. Byte Write

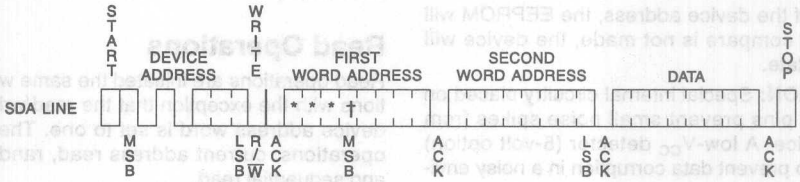
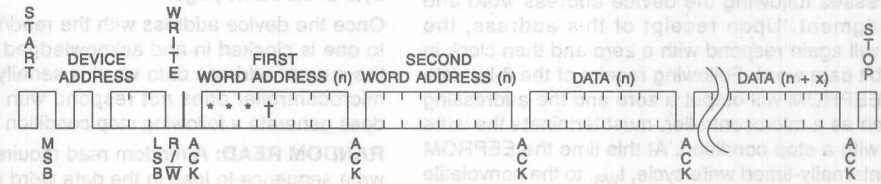


Figure 3. Page Write



Notes: 1. * = DON'T CARE bits

2. † = DON'T CARE bits for the 32K

Figure 4. Current Address Read

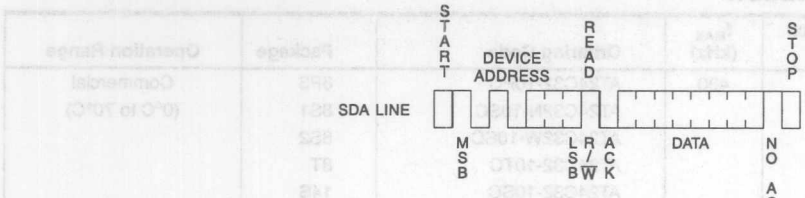
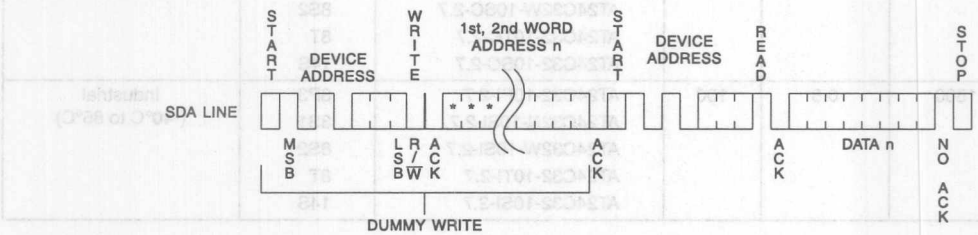
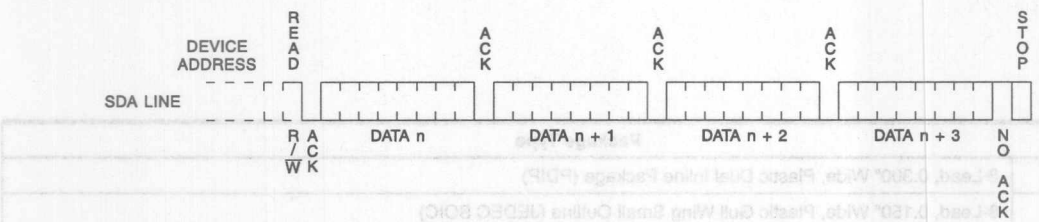


Figure 5. Random Read



Note: 1. * = DON'T CARE bits

Figure 6. Sequential Read



AT24C32 Ordering Information

t_{WR} (max) (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	3000	35	400	AT24C32-10PC	8P3	Commercial (0°C to 70°C)
				AT24C32N-10SC	8S1	
				AT24C32W-10SC	8S2	
				AT24C32-10TC	8T	
				AT24C32-10SC	14S	
	3000	35	400	AT24C32-10PI	8P3	Industrial (-40°C to 85°C)
				AT24C32N-10SI	8S1	
				AT24C32W-10SI	8S2	
				AT24C32-10TI	8T	
				AT24C32-10SI	14S	
10	1500	0.5	100	AT24C32-10PC-2.7	8P3	Commercial (0°C to 70°C)
				AT24C32N-10SC-2.7	8S1	
				AT24C32W-10SC-2.7	8S2	
				AT24C32-10TC-2.7	8T	
				AT24C32-10SC-2.7	14S	
	1500	0.5	100	AT24C32-10PI-2.7	8P3	Industrial (-40°C to 85°C)
				AT24C32N-10SI-2.7	8S1	
				AT24C32W-10SI-2.7	8S2	
				AT24C32-10TI-2.7	8T	
				AT24C32-10SI-2.7	14S	

Package Type	
8P3	8-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8S2	8-Lead, 0.200" Wide, Plastic Gull Wing Small Outline (EIAJ SOIC)
8T	8-Lead, 0.170" Wide, Plastic Gull Wing Small Outline (TSSOP)
14S	14-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
Options	
Blank	Standard Operation (4.5V to 5.5V)
-2.7	Low Voltage (2.7V to 5.5V)
-2.5	Low Voltage (2.5V to 5.5V)
-1.8	Low Voltage (1.8V to 5.5V)

AT24C32 Ordering Information (Continued)

t_{WR} (max) (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	1000	0.5	100	AT24C32-10PC-2.5 AT24C32N-10SC-2.5 AT24C32W-10SC-2.5 AT24C32-10TC-2.5 AT24C32-10SC-2.5	8P3 8S1 8S2 8T 14S	Commercial (0°C to 70°C)
	1000	0.5	100	AT24C32-10PI-2.5 AT24C32N-10SI-2.5 AT24C32W-10SI-2.5 AT24C32-10TI-2.5 AT24C32-10SI-2.5	8P3 8S1 8S2 8T 14S	Industrial (-40°C to 85°C)
10	800	0.1	100	AT24C32-10PC-1.8 AT24C32N-10SC-1.8 AT24C32W-10SC-1.8 AT24C32-10TC-1.8 AT24C32-10SC-1.8	8P3 8S1 8S2 8T 14S	Commercial (0°C to 70°C)
	800	0.1	100	AT24C32-10PI-1.8 AT24C32N-10SI-1.8 AT24C32W-10SI-1.8 AT24C32-10TI-1.8 AT24C32-10SI-1.8	8P3 8S1 8S2 8T 14S	Industrial (-40°C to 85°C)

Package Type	
8P3	8-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8S2	8-Lead, 0.200" Wide, Plastic Gull Wing Small Outline (EIAJ SOIC)
8T	8-Lead, 0.170" Wide, Plastic Gull Wing Small Outline (TSSOP)
14S	14-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
Options	
Blank	Standard Operation (4.5V to 5.5V)
-2.7	Low Voltage (2.7V to 5.5V)
-2.5	Low Voltage (2.5V to 5.5V)
-1.8	Low Voltage (1.8V to 5.5V)

AT24C64 Ordering Information

t_{WR} (max) (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	3000	35	400	AT24C64-10PC AT24C64N-10SC AT24C64W-10SC AT24C64-10TC AT24C64-10SC	8P3 8S1 8S2 8T 14S	Commercial (0°C to 70°C)
	3000	35	400	AT24C64-10PI AT24C64N-10SI AT24C64W-10SI AT24C64-10TI AT24C64-10SI	8P3 8S1 8S2 8T 14S	Industrial (-40°C to 85°C)
10	1500	0.5	100	AT24C64-10PC-2.7 AT24C64N-10SC-2.7 AT24C64W-10SC-2.7 AT24C64-10TC-2.7 AT24C64-10SC-2.7	8P3 8S1 8S2 8T 14S	Commercial (0°C to 70°C)
	1500	0.5	100	AT24C64-10PI-2.7 AT24C64N-10SI-2.7 AT24C64W-10SI-2.7 AT24C64-10TI-2.7 AT24C64-10SI-2.7	8P3 8S1 8S2 8T 14S	Industrial (-40°C to 85°C)

Package Type	
8P3	8-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8S2	8-Lead, 0.200" Wide, Plastic Gull Wing Small Outline (EIAJ SOIC)
8T	8-Lead, 0.170" Wide, Plastic Gull Wing Small Outline (TSSOP)
14S	14-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
Options	
Blank	Standard Operation (4.5V to 5.5V)
-2.7	Low Voltage (2.7V to 5.5V)
-2.5	Low Voltage (2.5V to 5.5V)
-1.8	Low Voltage (1.8V to 5.5V)

AT24C64 Ordering Information (Continued)

t_{WR} (max) (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	1000	0.5	100	AT24C64-10PC-2.5 AT24C64N-10SC-2.5 AT24C64W-10SC-2.5 AT24C64-10TC-2.5 AT24C64-10SC-2.5	8P3 8S1 8S2 8T 14S	Commercial (0°C to 70°C)
	1000	0.5	100	AT24C64-10PI-2.5 AT24C64N-10SI-2.5 AT24C64W-10SI-2.5 AT24C64-10TI-2.5 AT24C64-10SI-2.5	8P3 8S1 8S2 8T 14S	Industrial (-40°C to 85°C)
10	800	0.1	100	AT24C64-10PC-1.8 AT24C64N-10SC-1.8 AT24C64W-10SC-1.8 AT24C64-10TC-1.8 AT24C64-10SC-1.8	8P3 8S1 8S2 8T 14S	Commercial (0°C to 70°C)
	800	0.1	100	AT24C64-10PI-1.8 AT24C64N-10SI-1.8 AT24C64W-10SI-1.8 AT24C64-10TI-1.8 AT24C64-10SI-1.8	8P3 8S1 8S2 8T 14S	Industrial (-40°C to 85°C)

Package Type	
8P3	8-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8S2	8-Lead, 0.200" Wide, Plastic Gull Wing Small Outline (EIAJ SOIC)
8T	8-Lead, 0.170" Wide, Plastic Gull Wing Small Outline (TSSOP)
14S	14-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
Options	
Blank	Standard Operation (4.5V to 5.5V)
-2.7	Low Voltage (2.7V to 5.5V)
-2.5	Low Voltage (2.5V to 5.5V)
-1.8	Low Voltage (1.8V to 5.5V)

Features

- Low Voltage and Standard Voltage Operation
  - 5.0 (V_{CC} = 4.5V to 5.5V)
  - 2.7 (V_{CC} = 2.7V to 5.5V)
  - 1.8 (V_{CC} = 1.8V to 3.6V)
- Internally Organized 16,384 x 8 and 32,768 x 8
- 2-Wire Serial Interface
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- Bidirectional Data Transfer Protocol
- 1 MHz (5V), 400 kHz (2.7V) and 100 kHz (1.8V) Compatibility
- Write Protect Pin for Hardware and Software Data Protection
- 64-Byte Page Write Mode (Partial Page Writes Allowed)
- Self-Timed Write Cycle (5 ms typical)
- High Reliability
  - Endurance: 100,000 Write Cycles
  - Data Retention: 40 Years
  - ESD Protection: > 4000V
- Automotive Grade and Extended Temperature Devices Available
- 8-Pin JEDEC PDIP, 8-Pin JEDEC and EIAJ SOIC, 14-Pin TSSOP, and 8-Pin Leadless Array Packages

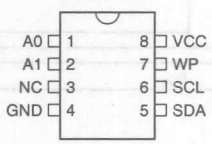
Description

The AT24C128/256 provides 131,072/262,144 bits of serial electrically erasable and programmable read only memory (EEPROM) organized as 16,384/32,768 words of 8 bits each. The device's cascadable feature allows up to 4 devices to share a common 2-wire bus. The device is optimized for use in many industrial and commercial applications where low power and low voltage operation are essential. The devices are available in space-saving 8-pin JEDEC PDIP, 8-pin EIAJ, 8-pin JEDEC SOIC, 14-pin TSSOP, and 8-pin LAP packages. In addition, the entire family is available in 5.0V (4.5V to 5.5V), 2.7V (2.7V to 5.5V) and 1.8V (1.8V to 3.6V) versions.

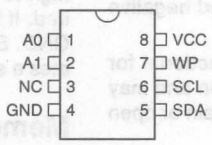
Pin Configurations

Pin Name	Function
A0 - A1	Address Inputs
SDA	Serial Data
SCL	Serial Clock Input
WP	Write Protect
NC	No Connect

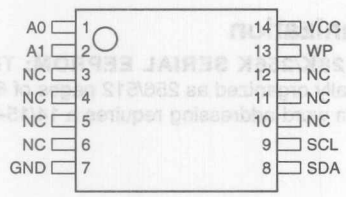
8-Pin PDIP



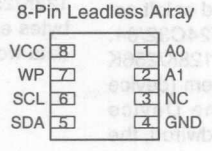
8-Pin SOIC



14-Pin TSSOP



8-Pin Leadless Array



Bottom View

2

2-Wire Serial EEPROMs

128K (16,384 x 8)

256K (32,768 x 8)

AT24C128
AT24C256

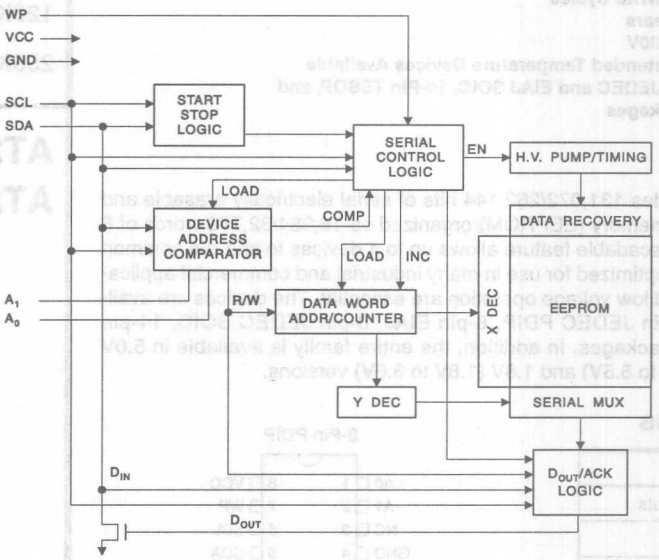
Rev. 0170C–08/98

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Block Diagram



Pin Description

SERIAL CLOCK (SCL): The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

SERIAL DATA (SDA): The SDA pin is bidirectional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open collector devices.

DEVICE/PAGE ADDRESSES (A1, A0): The A1 and A0 pins are device address inputs that are hardwired or left not connected for hardware compatibility with AT24C32/64. When the pins are hardwired, as many as four 128K/256K devices may be addressed on a single bus system (device addressing is discussed in detail under the Device Addressing section). When the pins are not hardwired, the default A_1 and A_0 are zero.

WRITE PROTECT (WP): The write protect input, when tied to GND, allows normal write operations. When WP is tied high to V_{CC}, all write operations to the memory are inhibited. If left unconnected, WP is internally pulled down to GND. Switching WP to V_{CC} prior to a write operation creates a software write protect function.

Memory Organization

AT24C128/256, 128K/256K SERIAL EEPROM: The 128K/256K is internally organized as 256/512 pages of 64-bytes each. Random word addressing requires a 14/15-bit data word address.

Pin Capacitance[1]

Applicable over recommended operating range from T_A = 25°C, f = 1.0 MHz, V_{CC} = +1.8V.

Symbol	Test Condition	Max	Units	Conditions
$C_{I/O}$	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}	Input Capacitance (A_0, A_1, SCL)	6	pF	V_{IN} = 0V

Note: This parameter is characterized and is not 100% tested.

DC Characteristics

Applicable over recommended operating range from: T_{AI} = -40°C to +85°C, V_{CC} = +1.8V to +5.5V, T_{AC} = 0°C to +70°C, V_{CC} = +1.8V to +5.5V (unless otherwise noted).

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
V_{CC1}	Supply Voltage			1.8		3.6	V
V_{CC2}	Supply Voltage			2.7		5.5	V
V_{CC3}	Supply Voltage			4.5		5.5	V
I_{CC1}	Supply Current	V_{CC} = 5.0V	READ at 400 kHz		1.0	2.0	mA
I_{CC2}	Supply Current	V_{CC} = 5.0V	WRITE at 400 kHz		2.0	3.0	mA
I_{SB1}	Standby Current (1.8V option)	V_{CC} = 1.8V	V_{IN} = V_{CC} or V_{SS}			0.2	µA
		V_{CC} = 3.6V				2.0	
I_{SB2}	Standby Current (2.7V option)	V_{CC} = 2.7V	V_{IN} = V_{CC} or V_{SS}			0.5	µA
		V_{CC} = 5.5V				6.0	
I_{SB3}	Standby Current (5.0V option)	V_{CC} = 4.5 - 5.5V	V_{IN} = V_{CC} or V_{SS}			6.0	µA
I_{LI}	Input Leakage Current	V_{IN} = V_{CC} or V_{SS}			0.10	3.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{CC} or V_{SS}			0.05	3.0	µA
V_{IL}	Input Low Level[1]			-0.6		V_{CC} x 0.3	V
V_{IH}	Input High Level[1]			V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL2}	Output Low Level	V_{CC} = 3.0V	I_{OL} = 2.1 mA			0.4	V
V_{OL1}	Output Low Level	V_{CC} = 1.8V	I_{OL} = 0.15 mA			0.2	V

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested

AC Characteristics

Applicable over recommended operating range from T_A = -40°C to +85°C, V_{CC} = +1.8V to +5.5V, CL = 100 pF (unless otherwise noted). Test conditions are listed in Note 2.

Symbol	Parameter	1.8-volt		2.7-volt		5.0-volt		Units
		Min	Max	Min	Max	Min	Max	
f_{SCL}	Clock Frequency, SCL		100		400		1000	kHz
t_{LOW}	Clock Pulse Width Low	4.7		1.3		0.6		µs
t_{HIGH}	Clock Pulse Width High	4.0		1.0		0.4		µs
t_{AA}	Clock Low to Data Out Valid	0.1	4.5	0.05	0.9	0.05	0.55	µs
t_{BUF}	Time the bus must be free before a new transmission can start(1)	4.7		1.3		0.5		µs
$t_{HD.STA}$	Start Hold Time	4.0		0.6		0.25		µs
$t_{SU.STA}$	Start Set-up Time	4.7		0.6		0.25		µs
$t_{HD.DAT}$	Data In Hold Time	0		0		0		µs
$t_{SU.DAT}$	Data In Set-up Time	200		100		100		ns
t_R	Inputs Rise Time(1)		1.0		0.3		0.3	µs
t_F	Inputs Fall Time(1)		300		300		100	ns
$t_{SU.STO}$	Stop Set-up Time	4.7		0.6		0.25		µs
t_{DH}	Data Out Hold Time	100		50		50		ns
t_{WR}	Write Cycle Time		20		10		10	ms
Endurance(1)	5.0V, 25°C, Page Mode	100K		100K		100K		Write Cycles

Notes: 1. This parameter is characterized and is not 100% tested.

2. AC measurement conditions:
   R_L (connects to V_{CC}): 1.3KΩ (2.7V, 5V), 10KΩ (1.8V)
   Input pulse voltages: $0.3V_{CC}$ to $0.7V_{CC}$
   Input rise and fall times: ≤50ns
   Input and output timing reference voltages: $0.5V_{CC}$

Device Operation

CLOCK and DATA TRANSITIONS: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (refer to Data Validity timing diagram). Data changes during SCL high periods will indicate a start or stop condition as defined below.

START CONDITION: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (refer to Start and Stop Definition timing diagram).

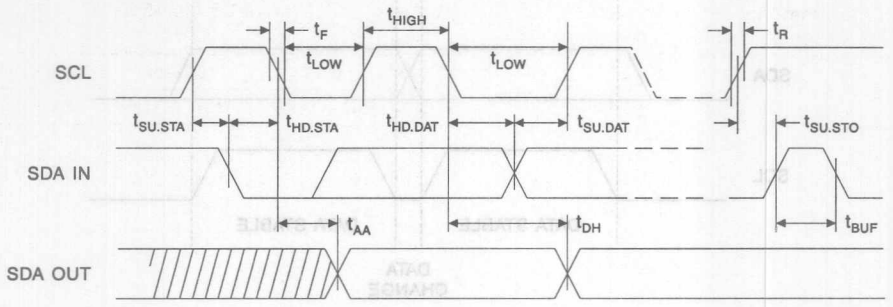
STOP CONDITION: A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode (refer to Start and Stop Definition timing diagram).

ACKNOWLEDGE: All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a zero during the ninth clock cycle to acknowledge that it has received each word.

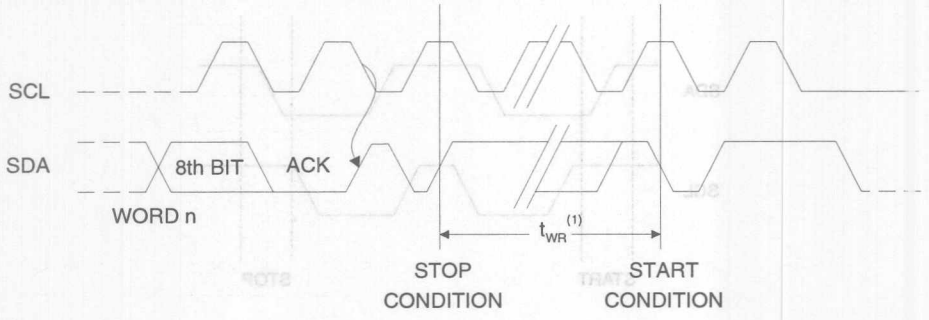
STANDBY MODE: The AT24C128/256 features a low power standby mode which is enabled: a) upon power-up and b) after the receipt of the STOP bit and the completion of any internal operations.

MEMORY RESET: After an interruption in protocol, power loss or system reset, any 2-wire part can be reset by following these steps: (a) Clock up to 9 cycles, (b) look for SDA high in each cycle while SCL is high and then (c) create a start condition as SDA is high.

Bus Timing (SCL: Serial Clock, SDA: Serial Data I/O)

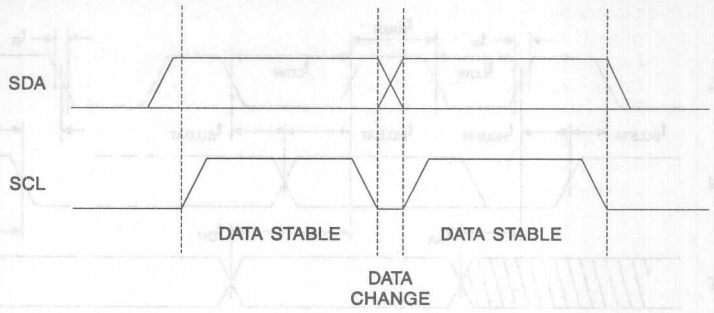


Write Cycle Timing (SCL: Serial Clock, SDA: Serial Data I/O)

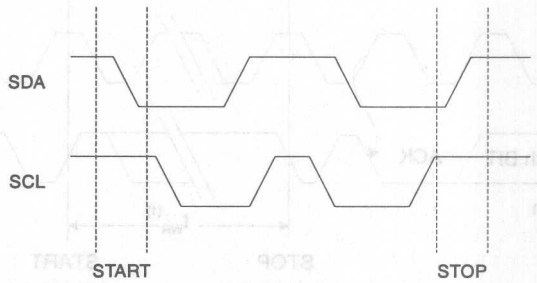


Note: 1. The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

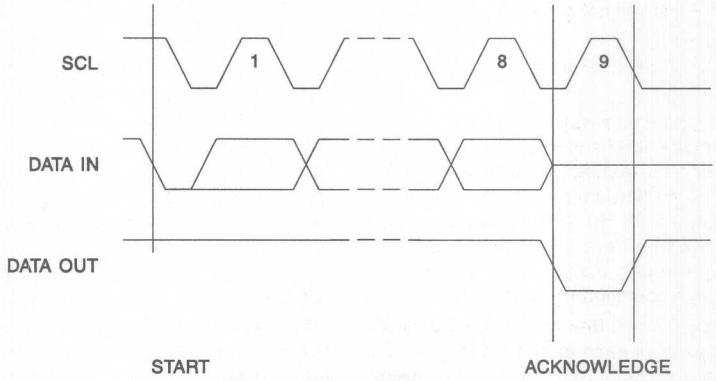
Data Validity



Start and Stop Definition



Output Acknowledge



Device Addressing

The 128K/256K EEPROM requires an 8-bit device address word following a start condition to enable the chip for a read or write operation (refer to Figure 1). The device address word consists of a mandatory one, zero sequence for the first five most significant bits as shown. This is common to all 2-wire EEPROM devices.

The 128K/256K uses the two device address bits A1, A0 to allow as many as four devices on the same bus. These bits must compare to their corresponding hardwired input pins. The A1 and A0 pins use an internal proprietary circuit that biases them to a logic low condition if the pins are allowed to float.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

Upon a compare of the device address, the EEPROM will output a zero. If a compare is not made, the device will return to a standby state.

DATA SECURITY: The AT24C128/256 has a hardware data protection scheme that allows the user to write protect the whole memory when the WP pin is at V_{CC}.

Write Operations

BYTE WRITE: A write operation requires two 8-bit data word addresses following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a zero and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a zero. The addressing device, such as a microcontroller, then must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally-timed write cycle, t_{WR}, to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (refer to Figure 2).

PAGE WRITE: The 128K/256K EEPROM is capable of 64-byte page writes.

A page write is initiated the same way as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to 63 more data words. The EEPROM will respond with a zero after each data word received. The microcontroller must terminate the page write sequence with a stop condition (refer to Figure 3).

The data word address lower 6 bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than 64 data words are transmitted to the EEPROM, the data word address will "roll over" and previous data will be overwritten. The address "roll over" during write is from the last byte of the current page to the first byte of the same page.

ACKNOWLEDGE POLLING: Once the internally-timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a zero, allowing the read or write sequence to continue.

Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to one. There are three read operations: current address read, random address read and sequential read.

CURRENT ADDRESS READ: The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address "roll over" during read is from the last byte of the last memory page, to the first byte of the first page.

Once the device address with the read/write select bit set to one is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input zero but does generate a following stop condition (refer to Figure 4).

RANDOM READ: A random read requires a "dummy" byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a zero but does generate a following stop condition (refer to Figure 5).

SEQUENTIAL READ: Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will "roll over" and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a zero but does generate a following stop condition (refer to Figure 6).

Figure 1. Device Address

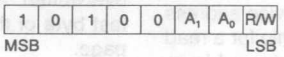


Figure 2. Byte Write

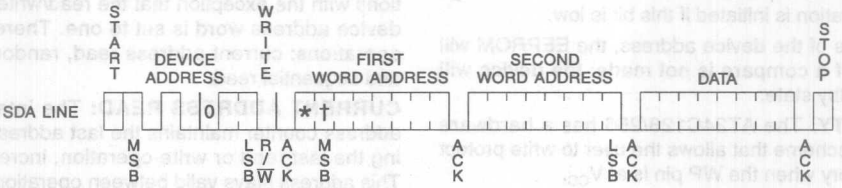
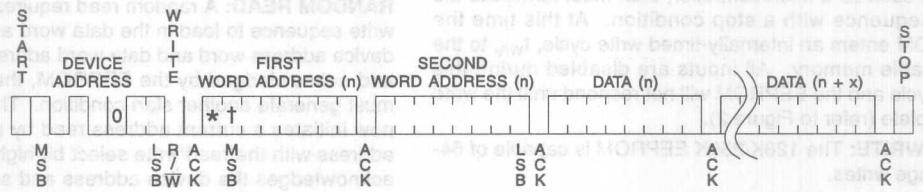


Figure 3. Page Write



(* = DON'T CARE bit)

(† = DON'T CARE bit for the 128K)

Figure 4. Current Address Read

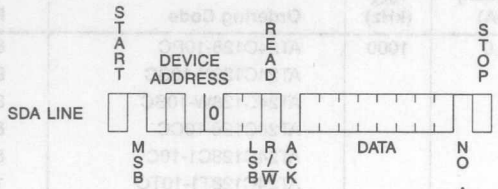
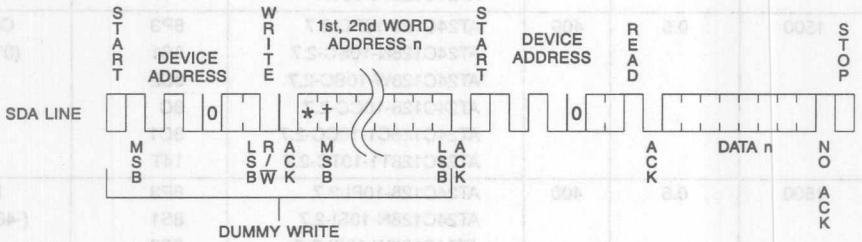


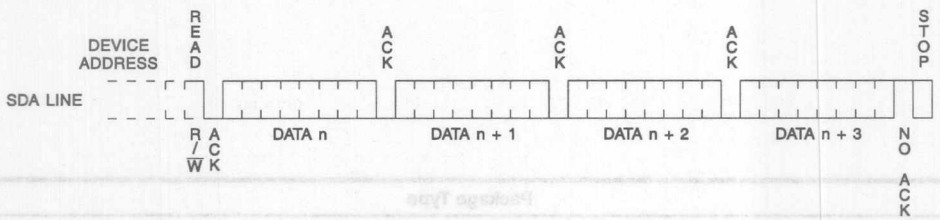
Figure 5. Random Read



(* = DON'T CARE bit)

(† = DON'T CARE bit for the 128K)

Figure 6. Sequential Read



AT24C128 Ordering Information

t_{WR} (max) (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	3000	6.0	1000	AT24C128-10PC AT24C128N-10SC AT24C128W-10SC AT24C128-10CC AT24C128C1-10CC AT24C128T1-10TC	8P3 8S1 8S2 8C 8C1 14T	Commercial (0°C to 70°C)
	3000	6.0	1000	AT24C128-10PI AT24C128N-10SI AT24C128W-10SI AT24C128-10CI AT24C128C1-10CI AT24C128T1-10TI	8P3 8S1 8S2 8C 8C1 14T	Industrial (-40°C to 85°C)
10	1500	0.5	400	AT24C128-10PC-2.7 AT24C128N-10SC-2.7 AT24C128W-10SC-2.7 AT24C128-10CC-2.7 AT24C128C1-10CC-2.7 AT24C128T1-10TC-2.7	8P3 8S1 8S2 8C 8C1 14T	Commercial (0°C to 70°C)
	1500	0.5	400	AT24C128-10PI-2.7 AT24C128N-10SI-2.7 AT24C128W-10SI-2.7 AT24C128-10CI-2.7 AT24C128C1-10CI-2.7 AT24C128T1-10TI-2.7	8P3 8S1 8S2 8C 8C1 14T	Industrial (-40°C to 85°C)

Package Type	
8C	8-Lead, 0.230" Wide, Leadless Array Package (LAP)
8C1	8-Lead, 0.300" Wide, Leadless Array Package (LAP)
8P3	8-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8-Lead, 0.150" Wide, Plastic Gull Wing Small Outline Package (JEDEC SOIC)
8S2	8-Lead, 0.200" Wide, Plastic Gull Wing Small Outline Package (EIAJ SOIC)
14T	14-Lead, 0.170" Wide, Thin Shrink Small Outline Package (TSSOP)
Options	
Blank	Standard Operation (4.5V to 5.5V)
-2.7	Low-Voltage (2.7V to 5.5V)
-1.8	Low-Voltage (1.8V to 3.6V)

AT24C128 Ordering Information (Continued)

t_{WR} (max) (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
20	800	0.2	100	AT24C128-10PC-1.8	8P3	Commercial
				AT24C128N-10SC-1.8	8S1	(0°C to 70°C)
				AT24C128W-10SC-1.8	8S2	
				AT24C128-10CC-1.8	8C	
				AT24C128C1-10CC-1.8	8C1	
				AT24C128T1-10TC-1.8	14T	
	800	0.2	100	AT24C128-10PI-1.8	8P3	Industrial
				AT24C128N-10SI-1.8	8S1	(-40°C to 85°C)
				AT24C128W-10SI-1.8	8S2	
				AT24C128-10CI-1.8	8C	
				AT24C128C1-10CI-1.8	8C1	
				AT24C128T1-10TI-1.8	14T	

Package Type	
8C	8-Lead, 0.230" Wide, Leadless Array Package (LAP)
8C1	8-Lead, 0.300" Wide, Leadless Array Package (LAP)
8P3	8-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
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14T	14-Lead, 0.170" Wide, Thin Shrink Small Outline Package (TSSOP)
Options	
Blank	Standard Operation (4.5V to 5.5V)
-2.7	Low-Voltage (2.7V to 5.5V)
-1.8	Low-Voltage (1.8V to 3.6V)

AT24C256 Ordering Information

t_{WR} (max) (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	3000	6.0	1000	AT24C256-10PC	8P3	Commercial
				AT24C256N-10SC	8S1	(0°C to 70°C)
				AT24C256W-10SC	8S2	
				AT24C256-10CC	8C	
				AT24C256C1-10CC	8C1	
				AT24C256T1-10TC	14T	
	3000	6.0	1000	AT24C256-10PI	8P3	Industrial
				AT24C256N-10SI	8S1	(-40°C to 85°C)
				AT24C256W-10SI	8S2	
				AT24C256-10CI	8C	
				AT24C256C1-10CI	8C1	
				AT24C256T1-10TI	14T	
10	1500	0.5	400	AT24C256-10PC-2.7	8P3	Commercial
				AT24C256N-10SC-2.7	8S1	(0°C to 70°C)
				AT24C256W-10SC-2.7	8S2	
				AT24C256-10CC-2.7	8C	
				AT24C256C1-10CC-2.7	8C1	
				AT24C256T1-10TC-2.7	14T	
	1500	0.5	400	AT24C256-10PI-2.7	8P3	Industrial
				AT24C256N-10SI-2.7	8S1	(-40°C to 85°C)
				AT24C256W-10SI-2.7	8S2	
				AT24C256-10CI-2.7	8C	
				AT24C256C1-10CI-2.7	8C1	
				AT24C256T1-10TI-2.7	14T	

Package Type	
8C	8-Lead, 0.230" Wide, Leadless Array Package (LAP)
8C1	8-Lead, 0.300" Wide, Leadless Array Package (LAP)
8P3	8-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
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14T	14-Lead, 0.170" Wide, Thin Shrink Small Outline Package (TSSOP)
Options	
Blank	Standard Operation (4.5V to 5.5V)
-2.7	Low-Voltage (2.7V to 5.5V)
-1.8	Low-Voltage (1.8V to 3.6V)

AT24C256 Ordering Information (Continued)

t_{WR} (max) (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
20	800	0.2	100	AT24C256-10PC-1.8	8P3	Commercial (0°C to 70°C)
				AT24C256N-10SC-1.8	8S1	
				AT24C256W-10SC-1.8	8S2	
				AT24C256-10CC-1.8	8C	
				AT24C256C1-10CC-1.8	8C1	
				AT24C256T1-10TC-1.8	14T	
	800	0.2	100	AT24C256-10PI-1.8	8P3	Industrial (-40°C to 85°C)
				AT24C256N-10SI-1.8	8S1	
				AT24C256W-10SI-1.8	8S2	
				AT24C256-10CI-1.8	8C	
				AT24C256C1-10CI-1.8	8C1	
				AT24C256T1-10TI-1.8	14T	

Package Type	
8C	8-Lead, 0.230" Wide, Leadless Array Package (LAP)
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Blank	Standard Operation (4.5V to 5.5V)
-2.7	Low-Voltage (2.7V to 5.5V)
-1.8	Low-Voltage (1.8V to 3.6V)

2-Wire Serial EEPROMs with Permanent Software Write Protect

128K (16,384 x 8)

256K (32,768 x 8)

AT24CS128
AT24CS256
Advance Information

Features

- One-Time Programmable (OTP) Feature
- Low-Voltage and Standard-Voltage Operation
  - 5.0 (V_{CC} = 4.5V to 5.5V)
  - 2.7 (V_{CC} = 2.7V to 5.5V)
  - 1.8 (V_{CC} = 1.8V to 3.6V)
- Internally Organized 16,384 x 8 and 32,768 x 8
- 2-Wire Serial Interface
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- Bidirectional Data Transfer Protocol
- 1 MHz (5V), 400 kHz (2.7V) and 100 kHz (1.8V) Compatibility
- Write Protect Pin for Hardware and Software Data Protection
- 64-Byte Page Write Mode (Partial Page Writes Allowed)
- Self-Timed Write Cycle (5 ms typical)
- High Reliability
  - Endurance: 100,000 Write Cycles
  - Data Retention: 40 Years
  - ESD Protection: >4000V
- Automotive Grade and Extended Temperature Devices Available
- 8-Pin JEDEC PDIP and 8-Pin JEDEC and EIAJ SOIC Packages

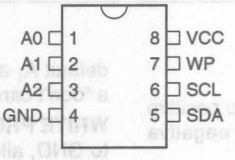
Description

The AT24CS128/256 provides 131,072/262,144 bits of serial electrically erasable and programmable read only memory (EEPROM) organized as 16,384/32,768 words of 8 bits each. The device's cascadable feature allows up to 4 devices to share a common 2-wire bus. The device also features a one-time programmable 2048 bit array, which once enabled, becomes read-only and cannot be overwritten. If not enabled, the OTP section will function as part of the normal memory array. The device is optimized for use in many industrial and commercial applications where low power and low voltage operation are essential. The devices are available in space-saving 8-pin JEDEC PDIP (AT24CS128/256), 8-pin EIAJ (AT24CS128/256), 8-pin JEDEC SOIC (AT24CS128) packages. In addition, the entire family is available in 5.0V (4.5V to 5.5V), 2.7V (2.7V to 5.5V) and 1.8V (1.8V to 3.6V) versions.

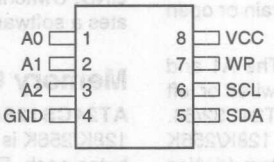
Pin Configurations

Pin Name	Function
A0 - A2	Address Inputs
SDA	Serial Data
SCL	Serial Clock Input
WP	Write Protect

8-Pin PDIP



8-Pin SOIC



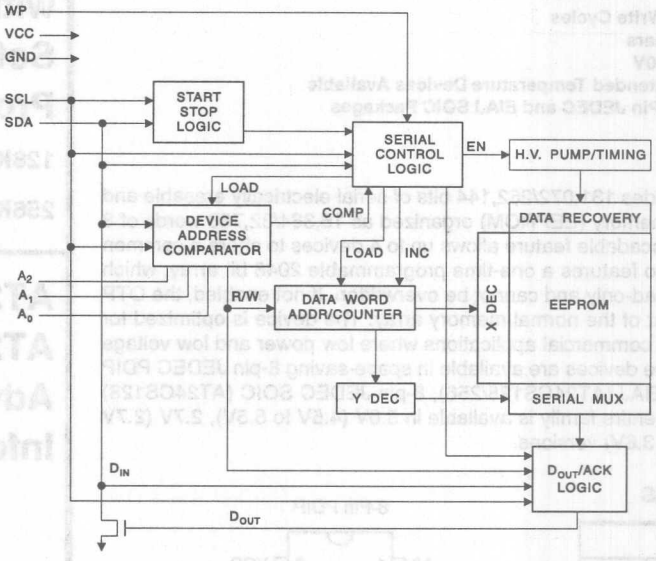
Rev. 1152A–09/98

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Block Diagram



Pin Description

SERIAL CLOCK (SCL): The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

SERIAL DATA (SDA): The SDA pin is bidirectional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open collector devices.

DEVICE/PAGE ADDRESSES (A2, A1, A0): The A1 and A0 pins are device address inputs that are hardwired or left not connected for hardware compatibility with AT24C32/64. When the pins are hardwired, as many as four 128K/256K devices may be addressed on a single bus system (device addressing is discussed in detail under the Device Addressing section). When the pins are not hardwired, the default A_1 and A_0 are zero. The A2 device address input is a "don't care" input.

WRITE PROTECT (WP): The write protect input, when tied to GND, allows normal write operations. When WP is tied high to V_{CC}, all write operations to the memory are inhibited. If left unconnected, WP is internally pulled down to GND. Switching WP to V_{CC} prior to a write operation creates a software write protect function.

Memory Organization

AT24CS128/256, 128K/256K SERIAL EEPROM: The 128K/256K is internally organized as 256/512 pages of 64-bytes each. Random word addressing requires a 14/15-bit data word address.

Pin Capacitance[1]

Applicable over recommended operating range from T_A = 25°C, f = 1.0 MHz, V_{CC} = +1.8V.

Symbol	Test Condition	Max	Units	Conditions
$C_{I/O}$	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}	Input Capacitance (A_0, A_1, SCL)	6	pF	V_{IN} = 0V

Note: This parameter is characterized and is not 100% tested.

DC Characteristics

Applicable over recommended operating range from: T_{AI} = -40°C to +85°C, V_{CC} = +1.8V to +5.5V, T_{AC} = 0°C to +70°C, V_{CC} = +1.8V to +5.5V (unless otherwise noted).

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
V_{CC1}	Supply Voltage			1.8		3.6	V
V_{CC2}	Supply Voltage			2.7		5.5	V
V_{CC3}	Supply Voltage			4.5		5.5	V
I_{CC1}	Supply Current	V_{CC} = 5.0V	READ at 400 kHz		1.0	2.0	mA
I_{CC2}	Supply Current	V_{CC} = 5.0V	WRITE at 400 kHz		2.0	3.0	mA
I_{SB1}	Standby Current (1.8V option)	V_{CC} = 1.8V	V_{IN} = V_{CC} or V_{SS}			0.2	µA
		V_{CC} = 3.6V				2.0	
I_{SB2}	Standby Current (2.7V option)	V_{CC} = 2.7V	V_{IN} = V_{CC} or V_{SS}			0.5	µA
		V_{CC} = 5.5V				5.0	
I_{SB3}	Standby Current (5.0V option)	V_{CC} = 4.5 - 5.5V	V_{IN} = V_{CC} or V_{SS}			5.0	µA
I_{LI}	Input Leakage Current	V_{IN} = V_{CC} or V_{SS}			0.10	3.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{CC} or V_{SS}			0.05	3.0	µA
V_{IL}	Input Low Level[1]			-0.6		V_{CC} x 0.3	V
V_{IH}	Input High Level[1]			V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL2}	Output Low Level	V_{CC3} = 3.0V	I_{OL} = 2.1 mA			0.4	V
V_{OL1}	Output Low Level	V_{CC} = 1.8V	I_{OL} = 0.15 mA			0.2	V

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested

AC Characteristics

Applicable over recommended operating range from T_A = -40°C to +85°C, V_{CC} = +1.8V to +5.5V, CL = 100 pF (unless otherwise noted). Test conditions are listed in Note 2.

Symbol	Parameter	1.8-volt		2.7-volt		5.0-volt		Units
		Min	Max	Min	Max	Min	Max	
f_{SCL}	Clock Frequency, SCL		400		1000		1000	kHz
t_{LOW}	Clock Pulse Width Low	1.3		0.6		0.6		µs
t_{HIGH}	Clock Pulse Width High	1.0		0.4		0.4		µs
t_{AA}	Clock Low to Data Out Valid	0.1	0.9	0.05	0.55	0.05	0.55	µs
t_{BUF}	Time the bus must be free before a new transmission can start(1)	1.2		0.5		0.5		µs
$t_{HD.STA}$	Start Hold Time	0.6		0.25		0.25		µs
$t_{SU.STA}$	Start Set-up Time	0.6		0.25		0.25		µs
$t_{HD.DAT}$	Data In Hold Time	0		0		0		µs
$t_{SU.DAT}$	Data In Set-up Time	100		100		100		ns
t_R	Inputs Rise Time(1)		0.3		0.3		0.3	µs
t_F	Inputs Fall Time(1)		300		100		100	ns
$t_{SU.STO}$	Stop Set-up Time	0.6		0.25		0.25		µs
t_{DH}	Data Out Hold Time	50		50		50		ns
t_{WR}	Write Cycle Time		20		10		10	ms
Endurance(1)	5.0V, 25°C, Page Mode	100K		100K		100K		Write Cycles

Notes: 1. This parameter is characterized and is not 100% tested.

2. AC measurement conditions:
   R_L (connects to V_{CC}): 1.3KΩ (2.7V, 5V), 10KΩ (1.8V)
   Input pulse voltages: $0.3V_{CC}$ to $0.7V_{CC}$
   Input rise and fall times: ≤50ns
   Input and output timing reference voltages: $0.5V_{CC}$

Device Operation

CLOCK and DATA TRANSITIONS: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (refer to Data Validity timing diagram). Data changes during SCL high periods will indicate a start or stop condition as defined below.

START CONDITION: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (refer to Start and Stop Definition timing diagram).

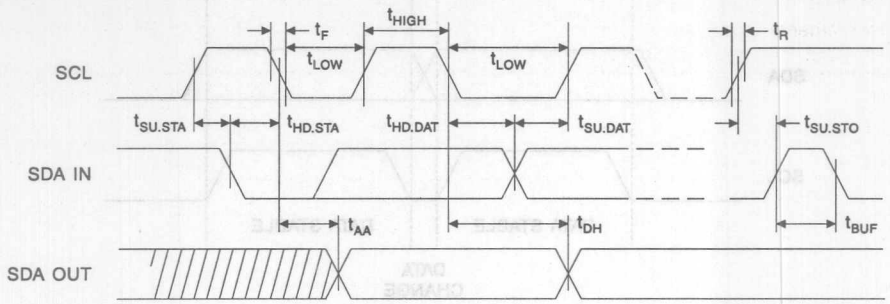
STOP CONDITION: A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode (refer to Start and Stop Definition timing diagram).

ACKNOWLEDGE: All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a zero during the ninth clock cycle to acknowledge that it has received each word.

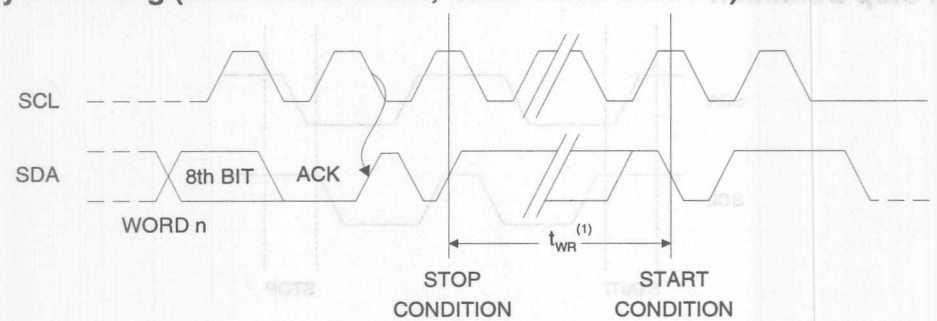
STANDBY MODE: The AT24CS128/256 features a low power standby mode which is enabled: a) upon power-up and b) after the receipt of the STOP bit and the completion of any internal operations.

MEMORY RESET: After an interruption in protocol, power loss or system reset, any 2-wire part can be reset by following these steps: (a) Clock up to 9 cycles, (b) look for SDA high in each cycle while SCL is high and then (c) create a start condition as SDA is high.

Bus Timing (SCL: Serial Clock, SDA: Serial Data I/O)

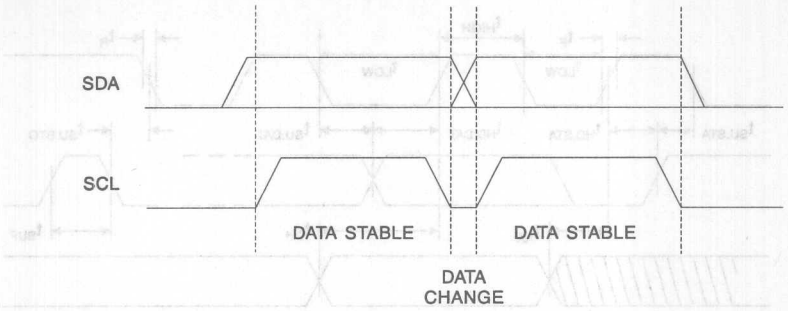


Write Cycle Timing (SCL: Serial Clock, SDA: Serial Data I/O)

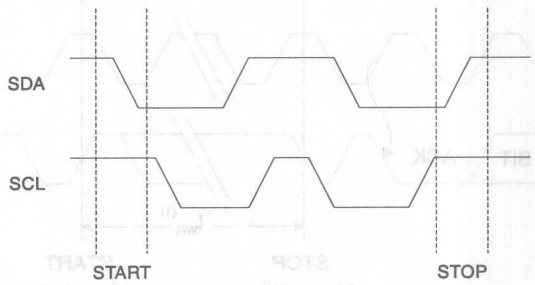


Note: 1. The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

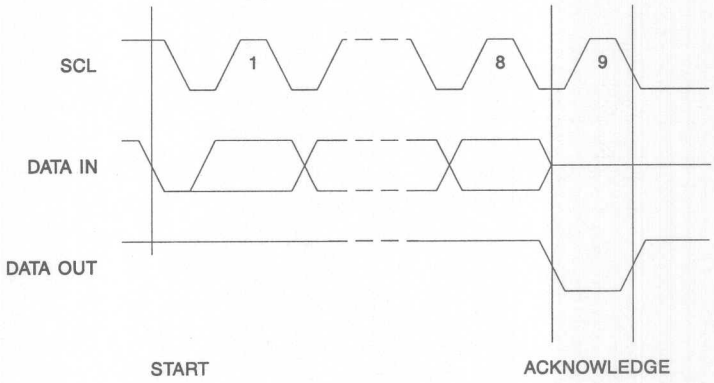
Data Validity



Start and Stop Definition



Output Acknowledge



Device Addressing

The 128K/256K EEPROM requires an 8-bit device address word following a start condition to enable the chip for a read or write operation (refer to Figure 1). The device address word consists of a mandatory one, zero sequence for the first five most significant bits as shown. This is common to all 2-wire EEPROM devices.

The 128K/256K uses the two device address bits A1, A0 to allow as many as four devices on the same bus. These bits must compare to their corresponding hardwired input pins. The A1 and A0 pins use an internal proprietary circuit that biases them to a logic low condition if the pins are allowed to float.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

Upon a compare of the device address, the EEPROM will output a zero. If a compare is not made, the device will return to a standby state.

DATA SECURITY: The AT24CS128/256 has a hardware data protection scheme that allows the user to write protect the whole memory when the WP pin is at V_{CC}.

Write Operations

BYTE WRITE: A write operation requires two 8-bit data word addresses following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a zero and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a zero. The addressing device, such as a microcontroller, then must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally-timed write cycle, t_{WR}, to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (refer to Figure 2).

PAGE WRITE: The 128K/256K EEPROM is capable of 64-byte page writes.

A page write is initiated the same way as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to 63 more data words. The EEPROM will respond with a zero after each data word received. The microcontroller must terminate the page write sequence with a stop condition (refer to Figure 3).

The data word address lower 6 bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than 64 data words are transmitted to the EEPROM, the data word address will "roll over" and previous data will be overwritten. The address "roll over" during write is from the last byte of the current page to the first byte of the same page.

ACKNOWLEDGE POLLING: Once the internally-timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a zero, allowing the read or write sequence to continue.

OTP Description/Operation

The OTP feature provides the user with a 2048-bit (256 x 8) security section, which once programmed and enabled, becomes read-only and data cannot be changed or overwritten. The OTP section is located in the upper 2K section of the memory array in the AT24CS128/256. If not enabled, the OTP section will function as part of the normal memory array.

To enable the OTP section:

1. Inputs must be connected:
   A2 = Don't Care, A1 and A0 = V_{CC} or GND
2. Initiate the programming sequence:

```
START 1010 1100 11xx xxxx xxxx xxxx xxxx xxxx STOP
```

Once enabled, previously written data cannot be changed. The status of the OTP section can only be confirmed by initiating a programming sequence to the OTP section and verifying by a read command. The use of the write protect (WP) feature can be utilized with or without enabling the OTP function.

Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to one. There are three read operations: current address read, random address read and sequential read.

CURRENT ADDRESS READ: The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address "roll over" during read is from the last byte of the last memory page, to the first byte of the first page.

Once the device address with the read/write select bit set to one is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input zero but does generate a following stop condition (refer to Figure 4).

RANDOM READ: A random read requires a "dummy" byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a zero but does generate a following stop condition (refer to Figure 5).

SEQUENTIAL READ: Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will "roll over" and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a zero but does generate a following stop condition (refer to Figure 6).

Figure 1. Device Address

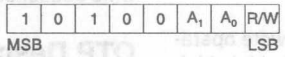


Figure 2. Byte Write

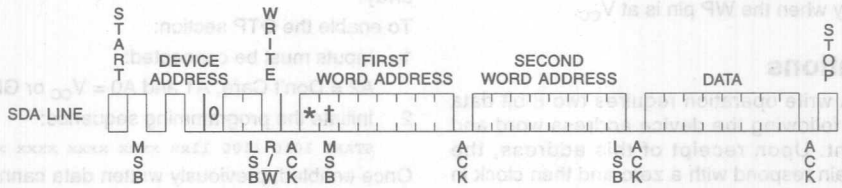
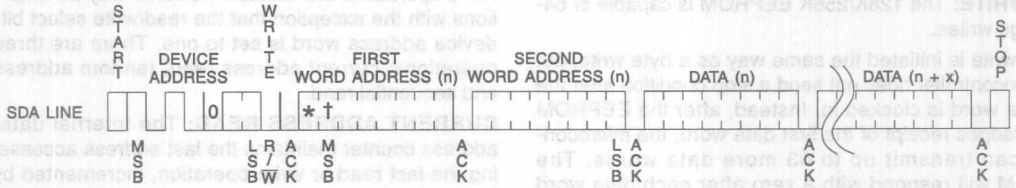


Figure 3. Page Write



(* = DON'T CARE bit)

(† = DON'T CARE bit for the 128K)

Figure 4. Current Address Read

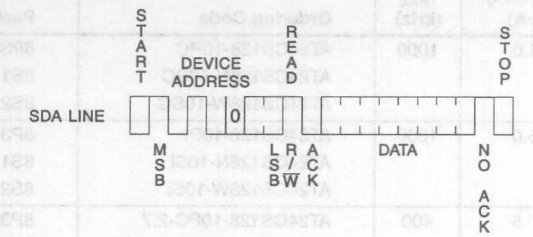
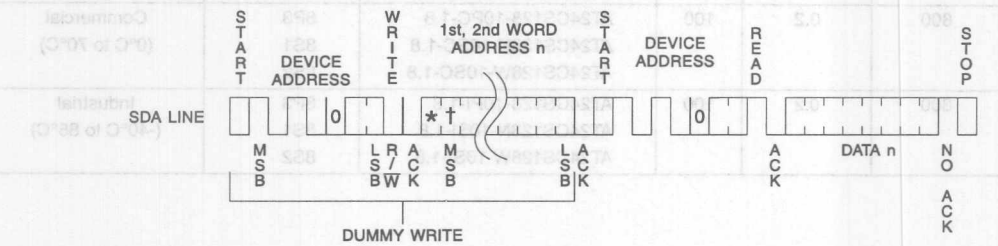


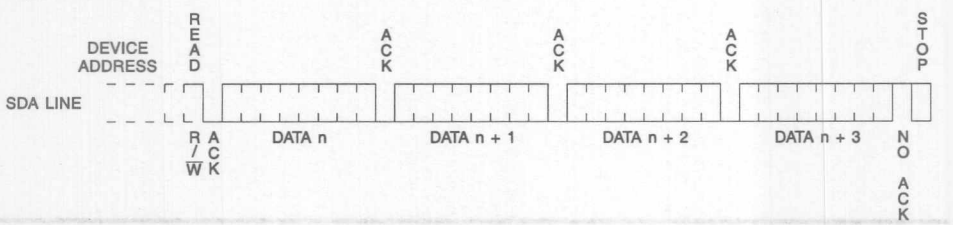
Figure 5. Random Read



(* = DON'T CARE bit)

(† = DON'T CARE bit for the 128K)

Figure 6. Sequential Read



AT24CS128 Ordering Information

t_{WR} (max) (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	3000	5.0	1000	AT24CS128-10PC AT24CS128N-10SC AT24CS128W-10SC	8P3 8S1 8S2	Commercial (0°C to 70°C)
	3000	5.0	1000	AT24CS128-10PI AT24CS128N-10SI AT24CS128W-10SI	8P3 8S1 8S2	Industrial (-40°C to 85°C)
10	1500	0.5	400	AT24CS128-10PC-2.7 AT24CS128N-10SC-2.7 AT24CS128W-10SC-2.7	8P3 8S1 8S2	Commercial (0°C to 70°C)
	1500	0.5	400	AT24CS128-10PI-2.7 AT24CS128N-10SI-2.7 AT24CS128W-10SI-2.7	8P3 8S1 8S2	Industrial (-40°C to 85°C)
20	800	0.2	100	AT24CS128-10PC-1.8 AT24CS128N-10SC-1.8 AT24CS128W-10SC-1.8	8P3 8S1 8S2	Commercial (0°C to 70°C)
	800	0.2	100	AT24CS128-10PI-1.8 AT24CS128N-10SI-1.8 AT24CS128W-10SI-1.8	8P3 8S1 8S2	Industrial (-40°C to 85°C)

Package Type	
8P3	8-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8S2	8-Lead, 0.200" Wide, Plastic Gull Wing Small Outline (EIAJ SOIC)
Options	
Blank	Standard Operation (4.5V to 5.5V)
-2.7	Low-Voltage (2.7V to 5.5V)
-1.8	Low-Voltage (1.8V to 3.6V)

AT24CS256 Ordering Information

t_{WR} (max) (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	3000	5.0	1000	AT24CS256-10PC AT24CS256W-10SC	8P3 8S2	Commercial (0°C to 70°C)
	3000	5.0	1000	AT24CS256-10PI AT24CS256W-10SI	8P3 8S2	Industrial (-40°C to 85°C)
10	1500	0.5	400	AT24CS256-10PC-2.7 AT24CS256W-10SC-2.7	8P3 8S2	Commercial (0°C to 70°C)
	1500	0.5	400	AT24CS256-10PI-2.7 AT24CS256W-10SI-2.7	8P3 8S2	Industrial (-40°C to 85°C)
20	800	0.2	100	AT24CS256-10PC-1.8 AT24CS256W-10SC-1.8	8P3 8S2	Commercial (0°C to 70°C)
	800	0.2	100	AT24CS256-10PI-1.8 AT24CS256W-10SI-1.8	8P3 8S2	Industrial (-40°C to 85°C)

Package Type	
8P3	8-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S2	8-Lead, 0.200" Wide, Plastic Gull Wing Small Outline (EIAJ SOIC)
Options	
Blank	Standard Operation (4.5V to 5.5V)
-2.7	Low-Voltage (2.7V to 5.5V)
-1.8	Low-Voltage (1.8V to 3.6V)

Features

- Low Voltage and Standard Voltage Operation
  - 5.0 (V_{CC} = 4.5V to 5.5V)
  - 2.7 (V_{CC} = 2.7V to 5.5V)
  - 1.8 (V_{CC} = 1.8V to 3.6V)
- Internally Organized 65,536 x 8
- 2-Wire Serial Interface
- Schmitt Triggers, Filtered Inputs for Noise Suppression
- Bidirectional Data Transfer Protocol
- 1 MHz (5V), 400 kHz (2.7V) and 100 kHz (1.8V) Compatibility
- Write Protect Pin for Hardware and Software Data Protection
- 128-Byte Page Write Mode (Partial Page Writes Allowed)
- Self-Timed Write Cycle (5 ms typical)
- High Reliability
  - Endurance: 100,000 Write Cycles
  - Data Retention: 40 Years
  - ESD Protection: >4000V
- Automotive Grade and Extended Temperature Devices Available
- 8-Pin PDIP and 20-Pin JEDEC SOIC and 8-Pin LAP Packages

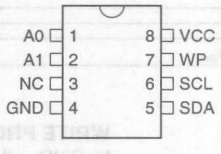
Description

The AT24C512 provides 524,288 bits of serial electrically erasable and programmable read only memory (EEPROM) organized as 65,536 words of 8 bits each. The device's cascadable feature allows up to 4 devices to share a common 2-wire bus. The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operation are essential. The devices are available in space-saving 8-pin PDIP, 20-pin JEDEC SOIC, and 8-pin Leadless Array (LAP) packages. In addition, the entire family is available in 5.0V (4.5V to 5.5V), 2.7V (2.7V to 5.5V) and 1.8V (1.8V to 3.6V) versions.

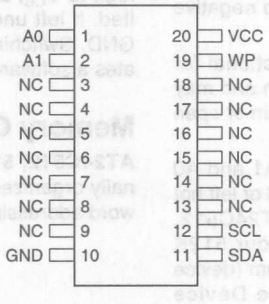
Pin Configurations

Pin Name	Function
A0 - A1	Address Inputs
SDA	Serial Data
SCL	Serial Clock Input
WP	Write Protect
NC	No Connect

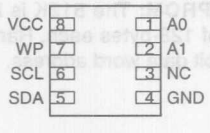
8-Pin PDIP



20-Pin SOIC



8-Pin Leadless Array



Bottom View

2

2-Wire Serial EEPROM

512K (65,536 x 8)

AT24C512

Preliminary

Rev. 116A–07/98

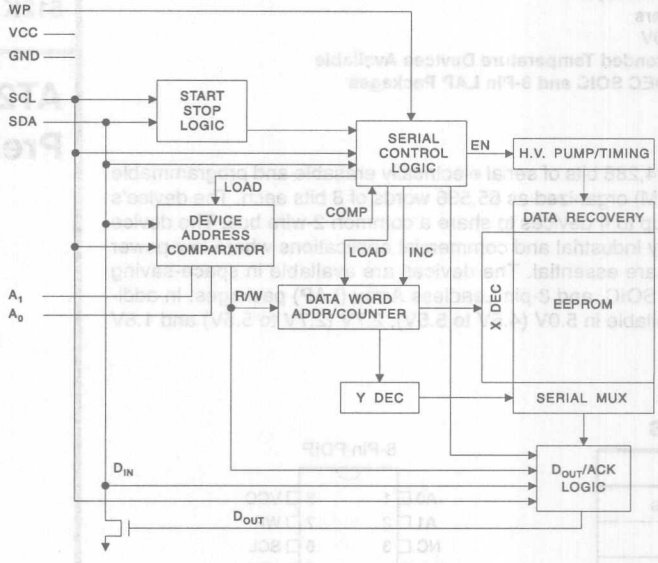
Note: Please contact Atmel Corporation for more information on this product.

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Block Diagram



Pin Description

SERIAL CLOCK (SCL): The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

SERIAL DATA (SDA): The SDA pin is bidirectional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open collector devices.

DEVICE/PAGE ADDRESSES (A1, A0): The A1 and A0 pins are device address inputs that are hardwired or left not connected for hardware compatibility with AT24C512. When the pins are hardwired, as many as four 512K devices may be addressed on a single bus system (device addressing is discussed in detail under the Device Addressing section). When the pins are not hardwired, the default A_1 and A_0 are zero.

WRITE PROTECT (WP): The write protect input, when tied to GND, allows normal write operations. When WP is tied high to V_{CC}, all write operations to the memory are inhibited. If left unconnected, WP is internally pulled down to GND. Switching WP to V_{CC} prior to a write operation creates a software write protect function.

Memory Organization

AT24C512, 512K SERIAL EEPROM: The 512K is internally organized as 512 pages of 128-bytes each. Random word addressing requires a 16-bit data word address.

Features

- Low Voltage and Standard Voltage Operation
  - 5.0 (V_{CC} = 4.5V to 5.5V)
  - 2.7 (V_{CC} = 2.7V to 5.5V)
  - 2.5 (V_{CC} = 2.5V to 5.5V)
  - 1.8 (V_{CC} = 1.8V to 5.5V)
- User Selectable Internal Organization
  - 1K: 128 x 8 or 64 x 16
  - 2K: 256 x 8 or 128 x 16
  - 4K: 512 x 8 or 256 x 16
- 3-Wire Serial Interface
- 2 MHz Clock Rate (5V) Compatibility
- Self-Timed Write Cycle (10 ms max)
- High Reliability
  - Endurance: 1 Million Write Cycles
  - Data Retention: 100 Years
  - ESD Protection: >4000V
- Automotive Grade and Extended Temperature Devices Available
- 8-Pin PDIP, 8-Pin JEDEC and EIAJ SOIC, and 8-Pin TSSOP Packages

Description

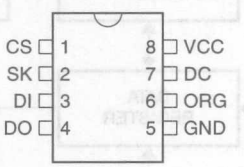
The AT93C46/56/57/66 provides 1024/2048/4096 bits of serial electrically erasable programmable read only memory (EEPROM) organized as 64/128/256 words of 16 bits each, when the ORG Pin is connected to V_{CC} and 128/256/512 words of 8 bits each when it is tied to ground. The device is optimized for use in many industrial and commercial applications where low power and low voltage operations are essential. The AT93C46/56/57/66 is available in space saving 8-pin PDIP and 8-pin JEDEC and EIAJ SOIC packages.

(continued)

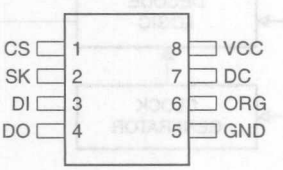
Pin Configurations

Pin Name	Function
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
VCC	Power Supply
ORG	Internal Organization
DC	Don't Connect

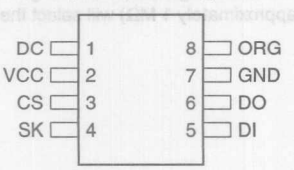
8-Pin PDIP



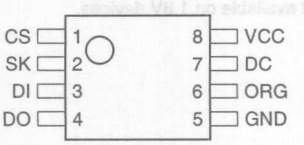
8-Pin SOIC



8-Pin SOIC
Rotated (R)
(1K JEDEC Only)



8-Pin TSSOP



ATMEL

2

3-Wire Serial EEPROMs

1K (128 x 8 or 64 x 16)

2K (256 x 8 or 128 x 16)

4K (512 x 8 or 256 x 16)

AT93C46
AT93C56
AT93C57
AT93C66

Rev. 0172K–07/98

The AT93C46/56/57/66 is enabled through the Chip Select pin (CS), and accessed via a 3-wire serial interface consisting of Data Input (DI), Data Output (DO), and Shift Clock (SK). Upon receiving a READ instruction at DI, the address is decoded and the data is clocked out serially on the data output pin DO. The WRITE cycle is completely self-timed and no separate ERASE cycle is required before WRITE. The WRITE cycle is only enabled when the part is in the ERASE/WRITE ENABLE state. When CS is brought "high" following the initiation of a WRITE cycle, the DO pin outputs the READY/BUSY status of the part.

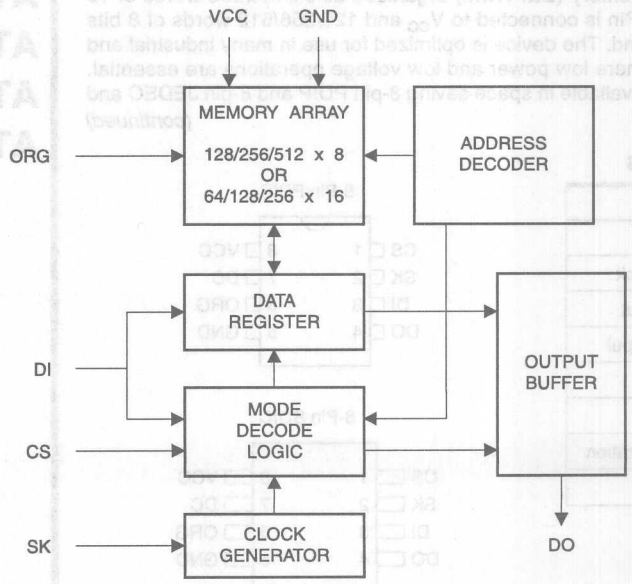
The AT93C46 is available in 4.5V to 5.5V, 2.7V to 5.5V, 2.5V to 5.5V, and 1.8V to 5.5V versions. The AT93C56/57/66 is available in 4.5V to 5.5V, 2.7V to 5.5V, and 2.5V to 5.5V versions.

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Block Diagram



Note: 1. When the ORG pin is connected to V_{CC}, the x 16 organization is selected. When it is connected to ground, the x 8 organization is selected. If the ORG pin is left unconnected, then an internal pullup device (of approximately 1 MΩ) will select the x 16 organization. This feature is not available on 1.8V devices.

Pin Capacitance[1]

Applicable over recommended operating range from T_A = 25°C, f = 1.0 MHz, V_{CC} = +5.0V (unless otherwise noted).

Symbol	Test Conditions	Max	Units	Conditions
C_{OUT}	Output Capacitance (DO)	5	pF	V_{OUT} = 0V
C_{IN}	Input Capacitance (CS, SK, DI)	5	pF	V_{IN} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

2

DC Characteristics

Applicable over recommended operating range from: T_{AI} = -40°C to +85°C, V_{CC} = +1.8V to +5.5V, T_{AC} = 0°C to +70°C, V_{CC} = +1.8V to +5.5V (unless otherwise noted).

Symbol	Parameter	Test Condition		Min	Typ	Max	Unit
V_{CC1}	Supply Voltage			1.8		5.5	V
V_{CC2}	Supply Voltage			2.5		5.5	V
V_{CC3}	Supply Voltage			2.7		5.5	V
V_{CC4}	Supply Voltage			4.5		5.5	V
I_{CC}	Supply Current	V_{CC} = 5.0V	READ at 1.0 MHz		0.5	2.0	mA
			WRITE at 1.0 MHz		0.5	2.0	mA
I_{SB1}	Standby Current	V_{CC} = 1.8V	CS = 0V		0	0.1	µA
I_{SB2}	Standby Current	V_{CC} = 2.5V	CS = 0V		6.0	10.0	µA
I_{SB3}	Standby Current	V_{CC} = 2.7V	CS = 0V		6.0	10.0	µA
I_{SB4}	Standby Current	V_{CC} = 5.0V	CS = 0V		17	30	µA
I_{IL}	Input Leakage	V_{IN} = 0V to V_{CC}			0.1	1.0	µA
I_{OL}	Output Leakage	V_{IN} = 0V to V_{CC}			0.1	1.0	µA
V_{IL1}[1] V_{IH1}[1]	Input Low Voltage Input High Voltage	4.5V ≤ V_{CC} ≤ 5.5V		-0.6 2.0		0.8 V_{CC} + 1	V
V_{IL2}[1] V_{IH2}[1]	Input Low Voltage Input High Voltage	1.8V ≤ V_{CC} ≤ 2.7V		-0.6 V_{CC} x 0.7		V_{CC} x 0.3 V_{CC} + 1	V
V_{OL1} V_{OH1}	Output Low Voltage Output High Voltage	4.5V ≤ V_{CC} ≤ 5.5V	I_{OL} = 2.1 mA			0.4	V
			I_{OH} = -0.4 mA	2.4			V
V_{OL2} V_{OH2}	Output Low Voltage Output High Voltage	1.8V ≤ V_{CC} ≤ 2.7V	I_{OL} = 0.15 mA			0.2	V
			I_{OH} = -100 µA	V_{CC} - 0.2			V

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

AC Characteristics

Applicable over recommended operating range from T_A = -40°C to + 85°C, V_{CC} = As Specified, CL = 1 TTL Gate and 100 pF (unless otherwise noted).

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
f_{SK}	SK Clock Frequency	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$		0 0 0 0		2 1 0.5 0.25	MHz
t_{SKH}	SK High Time	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$		250 250 500 1000			ns
t_{SKL}	SK Low Time	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$		250 250 500 1000			ns
t_{CS}	Minimum CS Low Time	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$		250 250 500 1000			ns
t_{CSS}	CS Setup Time	Relative to SK	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$	50 50 100 200			ns
t_{DIS}	DI Setup Time	Relative to SK	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$	100 100 200 400			ns
t_{CSH}	CS Hold Time	Relative to SK		0			ns
t_{DIH}	DI Hold Time	Relative to SK	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$	100 100 200 400			ns
t_{PD1}	Output Delay to '1'	AC Test	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$			250 250 500 1000	ns
t_{PD0}	Output Delay to '0'	AC Test	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$			250 250 500 1000	ns
t_{SV}	CS to Status Valid	AC Test	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$			250 250 500 1000	ns
t_{DF}	CS to DO in High Impedance	AC Test CS = V_{IL}	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$			100 100 200 400	ns
t_{WP}	Write Cycle Time			0.1		10	ms
			$4.5V \le V_{CC} \le 5.5V$		1		ms
Endurance[1]	5.0V, 25°C, Page Mode			1M			Write Cycles

Note: 1. This parameter is characterized and is not 100% tested.

Instruction Set for the AT93C46

Instruction	SB	Op Code	Address		Data		Comments
			x 8	x 16	x 8	x 16	
READ	1	10	A_6 - A_0	A_5 - A_0			Reads data stored in memory, at specified address.
EWEN	1	00	11XXXXX	11XXXX			Write enable must precede all programming modes.
ERASE	1	11	A_6 - A_0	A_5 - A_0			Erase memory location A_n - A_0.
WRITE	1	01	A_6 - A_0	A_5 - A_0	D_7 - D_0	D_{15} - D_0	Writes memory location A_n - A_0.
ERAL	1	00	10XXXXX	10XXXX			Erases all memory locations. Valid only at V_{CC} = 4.5V to 5.5V.
WRAL	1	00	01XXXXX	01XXXX	D_7 - D_0	D_{15} - D_0	Writes all memory locations. Valid only at V_{CC} = 4.5V to 5.5V.
EWDS	1	00	00XXXXX	00XXXX			Disables all programming instructions.

Instruction Set for the AT93C57

Instruction	SB	Op Code	Address		Data		Comments
			x 8	x 16	x 8	x 16	
READ	1	10	A_7 - A_0	A_6 - A_0			Reads data stored in memory, at specified address.
EWEN	1	00	11XXXXXX	11XXXXX			Write enable must precede all programming modes.
ERASE	1	11	A_7 - A_0	A_6 - A_0			Erase memory location A_n - A_0.
WRITE	1	01	A_7 - A_0	A_6 - A_0	D_7 - D_0	D_{15} - D_0	Writes memory location A_n - A_0.
ERAL	1	00	10XXXXXX	10XXXXX			Erases all memory locations. Valid only at V_{CC} = 4.5V to 5.5V.
WRAL	1	00	01XXXXXX	01XXXXX	D_7 - D_0	D_{15} - D_0	Writes all memory locations. Valid only at V_{CC} = 4.5V to 5.5V.
EWDS	1	00	00XXXXXX	00XXXXX			Disables all programming instructions.

Instruction Set for the AT93C56 and AT93C66

Instruction	SB	Op Code	Address		Data		Comments
			x 8	x 16	x 8	x 16	
READ	1	10	A_8 - A_0	A_7 - A_0			Reads data stored in memory, at specified address.
EWEN	1	00	11XXXXXXX	11XXXXXX			Write enable must precede all programming modes.
ERASE	1	11	A_8 - A_0	A_7 - A_0			Erases memory location A_n - A_0.
WRITE	1	01	A_8 - A_0	A_7 - A_0	D_7 - D_0	D_{15} - D_0	Writes memory location A_n - A_0.
ERAL	1	00	10XXXXXXX	10XXXXXX			Erases all memory locations. Valid only at V_{CC} = 4.5V to 5.5V.
WRAL	1	00	01XXXXXXX	01XXXXXX	D_7 - D_0	D_{15} - D_0	Writes all memory locations. Valid when V_{CC} = 5.0V ± 10% and Disable Register cleared.
EWDS	1	00	00XXXXXXX	00XXXXXX			Disables all programming instructions.

Functional Description

The AT93C46/56/57/66 is accessed via a simple and versatile 3-wire serial communication interface. Device operation is controlled by seven instructions issued by the host processor. **A valid instruction starts with a rising edge of CS** and consists of a Start Bit (logic "1") followed by the appropriate Op Code and the desired memory Address location.

READ (READ): The Read (READ) instruction contains the Address code for the memory location to be read. After the instruction and address are decoded, data from the selected memory location is available at the serial output pin DO. Output data changes are synchronized with the rising edges of serial clock SK. It should be noted that a dummy bit (logic "0") precedes the 8- or 16-bit data output string.

ERASE/WRITE (EWEN): To assure data integrity, the part automatically goes into the Erase/Write Disable (EWDS) state when power is first applied. An Erase/Write Enable (EWEN) instruction must be executed first before any programming instructions can be carried out. Please note that once in the Erase/Write Enable state, programming remains enabled until an Erase/Write Disable (EWDS) instruction is executed or V_{CC} power is removed from the part.

ERASE (ERASE): The Erase (ERASE) instruction programs all bits in the specified memory location to the logical "1" state. The self-timed erase cycle starts once the ERASE instruction and address are decoded. The DO pin outputs the READY/BUSY status of the part if CS is brought high after being kept low for a minimum of 250 ns (t_{CS}). A logic "1" at pin DO indicates that the selected memory location has been erased, and the part is ready for another instruction.

WRITE (WRITE): The Write (WRITE) instruction contains the 8 or 16 bits of data to be written into the specified memory location. The self-timed programming cycle, t_{WP}, starts after the last bit of data is received at serial data input pin DI. The DO pin outputs the READY/BUSY status of the part if CS is brought high after being kept low for a minimum of 250 ns (t_{CS}). A logic "0" at DO indicates that programming is still in progress. A logic "1" indicates that the memory location at the specified address has been written with the data pattern contained in the instruction and the part is ready for further instructions. **A READY/BUSY status cannot be obtained if the CS is brought high after the end of the self-timed programming cycle, t_{WP}.**

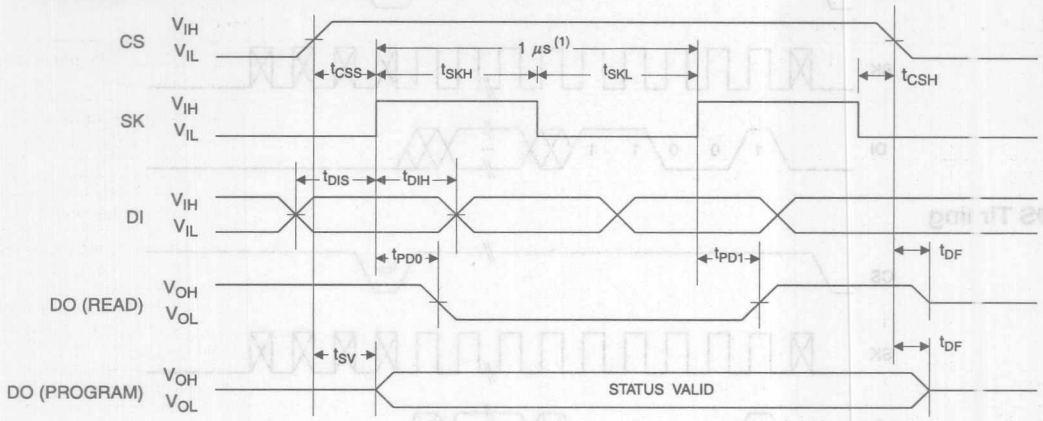
ERASE ALL (ERAL): The Erase All (ERAL) instruction programs every bit in the memory array to the logic "1" state and is primarily used for testing purposes. The DO pin outputs the READY/BUSY status of the part if CS is brought high after being kept low for a minimum of 250 ns (t_{CS}). The ERAL instruction is valid only at V_{CC} = 5.0V ± 10%.

WRITE ALL (WRAL): The Write All (WRAL) instruction programs all memory locations with the data patterns specified in the instruction. The DO pin outputs the READY/BUSY status of the part if CS is brought high after being kept low for a minimum of 250 ns (t_{CS}). The WRAL instruction is valid only at V_{CC} = 5.0V ± 10%.

ERASE/WRITE DISABLE (EWDS): To protect against accidental data disturb, the Erase/Write Disable (EWDS) instruction disables all programming modes and should be executed after all programming operations. The operation of the READ instruction is independent of both the EWEN and EWDS instructions and can be executed at any time.

Timing Diagrams

Synchronous Data Timing



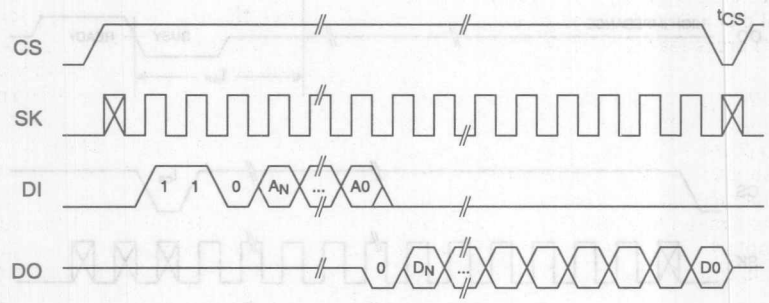
Note: 1. This is the minimum SK period.

Organization Key for Timing Diagrams

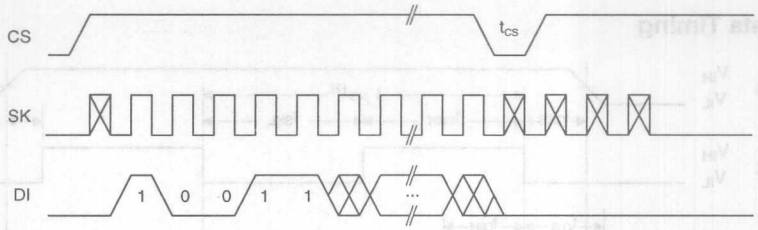
	AT93C46 (1K)		AT93C56 (2K)		AT93C57 (2K)		AT93C66 (4K)	
I/O	x 8	x 16	x 8	x 16	x 8	x 16	x 8	x 16
A_N	A_6	A_5	A_8 (1)	A_7	A_7	A_6	A_8	A_7
D_N	D_7	D_{15}	D_7	D_{15}	D_7	D_{15}	D_7	D_{15}

Note: 1. A_8 is a DON'T CARE value, but the extra clock is required.

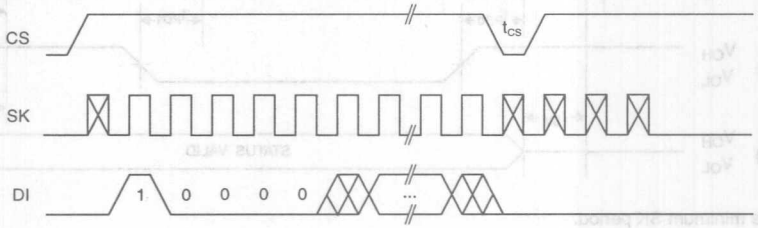
READ Timing



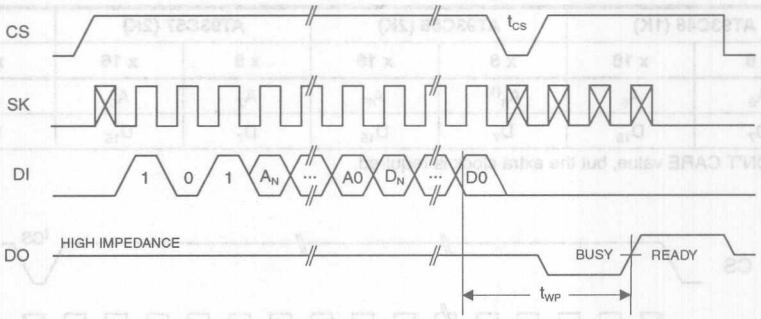
EWEN Timing



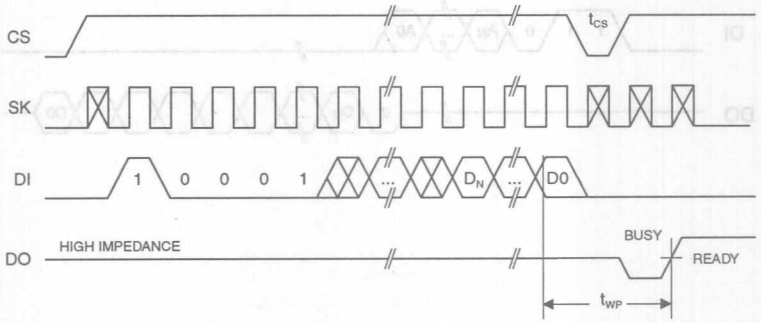
EWDS Timing



WRITE Timing

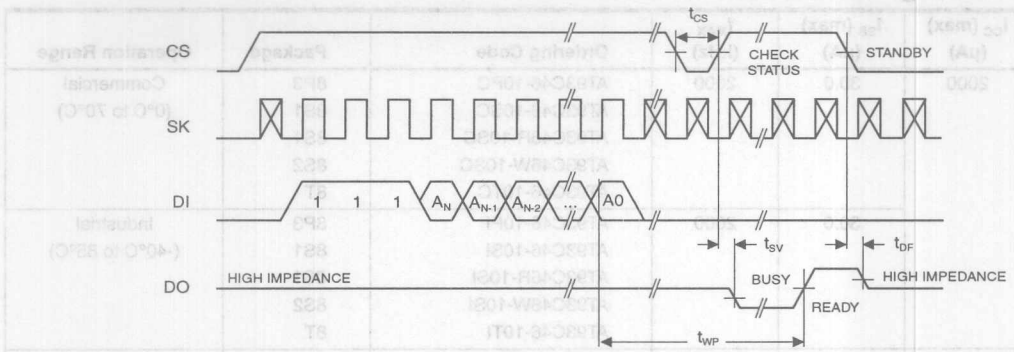


WRAL Timing[1]

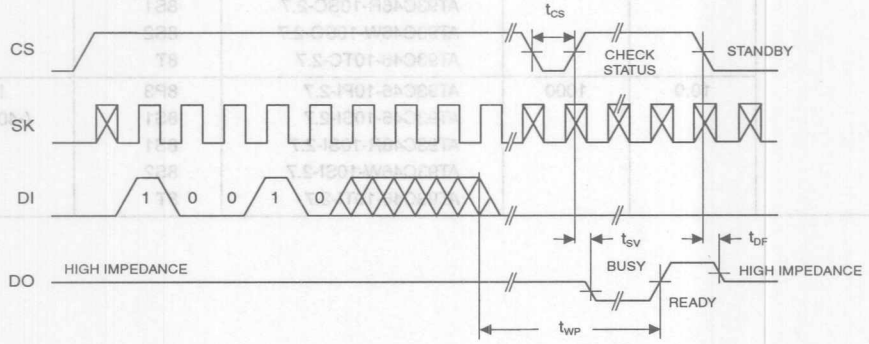


Note: 1. Valid only at V_{CC} = 4.5V to 5.5V.

ERASE Timing



TERAL Timing[1]



Note: 1. Valid only at V_{CC} = 4.5V to 5.5V.

AT93C46 Ordering Information

t_{WP} (max) (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	2000	30.0	2000	AT93C46-10PC	8P3	Commercial (0°C to 70°C)
				AT93C46-10SC	8S1	
				AT93C46R-10SC	8S1	
				AT93C46W-10SC	8S2	
				AT93C46-10TC	8T	
		30.0	2000	AT93C46-10PI	8P3	Industrial (-40°C to 85°C)
				AT93C46-10SI	8S1	
				AT93C46R-10SI	8S1	
				AT93C46W-10SI	8S2	
				AT93C46-10TI	8T	
10	800	10.0	1000	AT93C46-10PC-2.7	8P3	Commercial (0°C to 70°C)
				AT93C46-10SC-2.7	8S1	
				AT93C46R-10SC-2.7	8S1	
				AT93C46W-10SC-2.7	8S2	
				AT93C46-10TC-2.7	8T	
		10.0	1000	AT93C46-10PI-2.7	8P3	Industrial (-40°C to 85°C)
				AT93C46-10SI-2.7	8S1	
				AT93C46R-10SI-2.7	8S1	
				AT93C46W-10SI-2.7	8S2	
				AT93C46-10TI-2.7	8T	

Package Type	
8P3	8-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8S2	8-Lead, 0.200" Wide, Plastic Gull Wing Small Outline (EIAJ SOIC)
8T	8-Lead, 0.170" Wide, Thin Shrink Small Outline Package (TSSOP)
Options	
Blank	Standard Operation (4.5V to 5.5V)
-2.7	Low Voltage (2.7V to 5.5V)
-2.5	Low Voltage (2.5V to 5.5V)
R	Rotated Pinout

AT93C46 Ordering Information (Continued)

t_{WP} (max) (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	600	10.0	500	AT93C46-10PC-2.5	8P3	Commercial
				AT93C46-10SC-2.5	8S1	(0°C to 70°C)
				AT93C46R-10SC-2.5	8S1	
				AT93C46W-10SC-2.5	8S2	
				AT93C46-10TC-2.5	8T	
		10.0	500	AT93C46-10PI-2.5	8P3	Industrial
				AT93C46-10SI-2.5	8S1	(-40°C to 85°C)
				AT93C46R-10SI-2.5	8S1	
				AT93C46W-10SI-2.5	8S2	
				AT93C46-10TI-2.5	8T	
10	80	0.1	250	AT93C46-10PC-1.8	8P3	Commercial
				AT93C46-10SC-1.8	8S1	(0°C to 70°C)
				AT93C46R-10SC-1.8	8S1	
				AT93C46W-10SC-1.8	8S2	
				AT93C46-10TC-1.8	8T	
		0.1	250	AT93C46-10PI-1.8	8P3	Industrial
				AT93C46-10SI-1.8	8S1	(-40°C to 85°C)
				AT93C46R-10SI-1.8	8S1	
				AT93C46W-10SI-1.8	8S2	
				AT93C46-10TI-1.8	8T	

Package Type	
8P3	8-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8S2	8-Lead, 0.200" Wide, Plastic Gull Wing Small Outline (EIAJ SOIC)
8T	8-Lead, 0.170" Wide, Thin Shrink Small Outline Package (TSSOP)
Options	
Blank	Standard Operation (4.5V to 5.5V)
-2.7	Low Voltage (2.7V to 5.5V)
-2.5	Low Voltage (2.5V to 5.5V)
R	Rotated Pinout

AT93C56 Ordering Information

t_{WP} (max) (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	2000	30.0	2000	AT93C56-10PC AT93C56-10SC AT93C56W-10SC	8P3 8S1 8S2	Commercial (0°C to 70°C)
		30.0	2000	AT93C56-10PI AT93C56-10SI AT93C56W-10SI	8P3 8S1 8S2	Industrial (-40°C to 85°C)
10	800	10.0	1000	AT93C56-10PC-2.7 AT93C56-10SC-2.7 AT93C56W-10SC-2.7	8P3 8S1 8S2	Commercial (0°C to 70°C)
		10.0	1000	AT93C56-10PI-2.7 AT93C56-10SI-2.7 AT93C56W-10SI-2.7	8P3 8S1 8S2	Industrial (-40°C to 85°C)
10	600	10.0	500	AT93C56-10PC-2.5 AT93C56-10SC-2.5 AT93C56W-10SC-2.5	8P3 8S1 8S2	Commercial (0°C to 70°C)
		10.0	500	AT93C56-10PI-2.5 AT93C56-10SI-2.5 AT93C56W-10SI-2.5	8P3 8S1 8S2	Industrial (-40°C to 85°C)

Package Type	
8P3	8-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8S2	8-Lead, 0.200" Wide, Plastic Gull Wing Small Outline (EIAJ SOIC)
Options	
Blank	Standard Operation (4.5V to 5.5V)
-2.7	Low Voltage (2.7V to 5.5V)
-2.5	Low Voltage (2.5V to 5.5V)
R	Rotated Pinout

AT93C57 Ordering Information

t_{WP} (max) (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	2000	30.0	2000	AT93C57-10PC AT93C57-10SC AT93C57W-10SC	8P3 8S1 8S2	Commercial (0°C to 70°C)
		30.0	2000	AT93C57-10PI AT93C57-10SI AT93C57W-10SI	8P3 8S1 8S2	Industrial (-40°C to 85°C)
10	800	10.0	1000	AT93C57-10PC-2.7 AT93C57-10SC-2.7 AT93C57W-10SC-2.7	8P3 8S1 8S2	Commercial (0°C to 70°C)
		10.0	1000	AT93C57-10PI-2.7 AT93C57-10SI-2.7 AT93C57W-10SI-2.7	8P3 8S1 8S2	Industrial (-40°C to 85°C)

Package Type	
8P3	8-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8S2	8-Lead, 0.200" Wide, Plastic Gull Wing Small Outline (EIAJ SOIC)
Options	
Blank	Standard Operation (4.5V to 5.5V)
-2.7	Low Voltage (2.7V to 5.5V)
-2.5	Low Voltage (2.5V to 5.5V)
R	Rotated Pinout

AT93C66 Ordering Information

t_{WP} (max) (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	2000	30.0	2000	AT93C66-10PC AT93C66-10SC AT93C66W-10SC	8P3 8S1 8S2	Commercial (0°C to 70°C)
		30.0	2000	AT93C66-10PI AT93C66-10SI AT93C66W-10SI	8P3 8S1 8S2	Industrial (-40°C to 85°C)
10	800	10.0	1000	AT93C66-10PC-2.7 AT93C66-10SC-2.7 AT93C66W-10SC-2.7	8P3 8S1 8S2	Commercial (0°C to 70°C)
		10.0	1000	AT93C66-10PI-2.7 AT93C66-10SI-2.7 AT93C66W-10SI-2.7	8P3 8S1 8S2	Industrial (-40°C to 85°C)
10	600	10.0	500	AT93C66-10PC-2.5 AT93C66-10SC-2.5 AT93C66W-10SC-2.5	8P3 8S1 8S2	Commercial (0°C to 70°C)
		10.0	500	AT93C66-10PI-2.5 AT93C66-10SI-2.5 AT93C66W-10SI-2.5	8P3 8S1 8S2	Industrial (-40°C to 85°C)

Package Type	
8P3	8-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8S2	8-Lead, 0.200" Wide, Plastic Gull Wing Small Outline (EIAJ SOIC)
Options	
Blank	Standard Operation (4.5V to 5.5V)
-2.7	Low Voltage (2.7V to 5.5V)
-2.5	Low Voltage (2.5V to 5.5V)
R	Rotated Pinout

Features

- **Low-Voltage and Standard-Voltage Operation**
  - **5.0 (V_{CC} = 4.5V to 5.5V)**
  - **2.7 (V_{CC} = 2.7V to 5.5V)**
  - **2.5 (V_{CC} = 2.5V to 5.5V)**
- **3-Wire Serial Interface**
- **2 MHz Clock Rate (5V) Compatibility**
- **Self-Timed Write Cycle (10 ms max)**
- **High Reliability**
  - **Endurance: 1 Million Write Cycles**
  - **Data Retention: 100 Years**
  - **ESD Protection: >4,000V**
- **Automotive Grade and Extended Temperature Devices Available**
- **8-Pin PDIP, 8-Pin JEDEC SOIC, and 8-Pin TSSOP Packages**

Description

The AT93C46A provides 1024 bits of serial electrically erasable programmable read only memory (EEPROM) organized as 64 words of 16 bits each. The device is optimized for use in many industrial and commercial applications where low power and low voltage operation are essential. The AT93C46A is available in space saving 8-pin PDIP, 8-pin JEDEC, and 8-Pin TSSOP packages.

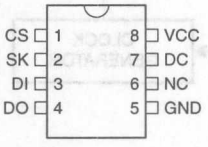
The AT93C46A is enabled through the Chip Select pin (CS), and accessed via a 3-wire serial interface consisting of Data Input (DI), Data Output (DO), and Shift Clock (SK). Upon receiving a READ instruction at DI, the address is decoded and the data is clocked out serially on the data output pin DO. The WRITE cycle is completely self-timed and no separate ERASE cycle is required before WRITE. The WRITE cycle is only enabled when the part is in the ERASE/WRITE ENABLE state. When CS is brought "high" following the initiation of a WRITE cycle, the DO pin outputs the READY/BUSY status of the part.

The AT93C46A is available in 4.5V to 5.5V, 2.7V to 5.5V, and 2.5V to 5.5V versions.

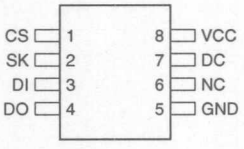
Pin Configurations

Pin Name	Function
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
VCC	Power Supply
NC	No Connect
DC	Don't Connect

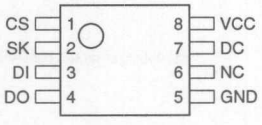
8-Pin PDIP



8-Pin SOIC



8-Pin TSSOP



3-Wire Serial EEPROM

1K (64 x 16)

AT93C46A

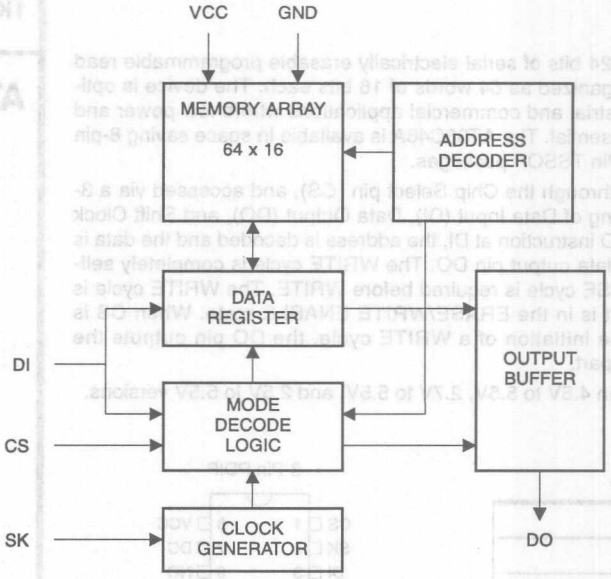
Rev. 0539C–10/98

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Block Diagram



Pin Capacitance[1]

Applicable over recommended operating range from T_A = 25°C, f = 1.0 MHz, V_{CC} = +5.0V (unless otherwise noted).

Symbol	Test Conditions	Max	Units	Conditions
C_{OUT}	Output Capacitance (DO)	5	pF	V_{OUT} = 0V
C_{IN}	Input Capacitance (CS, SK, DI)	5	pF	V_{IN} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

2

DC Characteristics

Applicable over recommended operating range from: T_{AI} = -40°C to +85°C, V_{CC} = +2.5V to +5.5V, T_{AC} = 0°C to +70°C, V_{CC} = +2.5V to +5.5V (unless otherwise noted).

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
V_{CC1}	Supply Voltage			1.8		5.5	V
V_{CC2}	Supply Voltage			2.5		5.5	V
V_{CC3}	Supply Voltage			2.7		5.5	V
V_{CC4}	Supply Voltage			4.5		5.5	V
I_{CC}	Supply Current	V_{CC} = 5.0V	READ at 1.0 MHz		0.5	2.0	mA
			WRITE at 1.0 MHz		0.5	2.0	mA
I_{SB1}	Standby Current	V_{CC} = 2.5V	CS = 0V		14.0	20.0	µA
I_{SB2}	Standby Current	V_{CC} = 2.7V	CS = 0V		14.0	20.0	µA
I_{SB3}	Standby Current	V_{CC} = 5.0V	CS = 0V		35.0	50.0	µA
I_{IL}	Input Leakage	V_{IN} = 0V to V_{CC}			0.1	1.0	µA
I_{OL}	Output Leakage	V_{IN} = 0V to V_{CC}			0.1	1.0	µA
V_{IL1}[1] V_{IH1}[1]	Input Low Voltage Input High Voltage	4.5V ≤ V_{CC} ≤ 5.5V		-0.6 2.0		0.8 V_{CC} + 1	V
V_{IL2}[1] V_{IH2}[1]	Input Low Voltage Input High Voltage	1.8V ≤ V_{CC} ≤ 2.7V		-0.6 V_{CC} x 0.7		V_{CC} x 0.3 V_{CC} + 1	V
V_{OL1}	Output Low Voltage	4.5V ≤ V_{CC} ≤ 5.5V	I_{OL} = 2.1 mA			0.4	V
V_{OH1}	Output High Voltage		I_{OH} = -0.4 mA	2.4			V
V_{OL2}	Output Low Voltage	1.8V ≤ V_{CC} ≤ 2.7V	I_{OL} = 0.15 mA			0.2	V
V_{OH2}	Output High Voltage		I_{OH} = -100 µA	V_{CC} - 0.2			V

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

AC Characteristics

Applicable over recommended operating range from T_A = -40°C to + 85°C, V_{CC} = +2.5V to + 5.5V, CL = 1 TTL Gate and 100 pF (unless otherwise noted).

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
f_{SK}	SK Clock Frequency	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$		0 0 0 0		2 1 0.5 0.25	MHz
t_{SKH}	SK High Time	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$		250 250 500 1000			ns
t_{SKL}	SK Low Time	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$		250 250 500 1000			ns
t_{CS}	Minimum CS Low Time	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$		250 250 500 1000			ns
t_{CSS}	CS Setup Time	Relative to SK	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$	50 50 100 200			ns
t_{DIS}	DI Setup Time	Relative to SK	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$	100 100 200 400			ns
t_{CSH}	CS Hold Time	Relative to SK		0			ns
t_{DIH}	DI Hold Time	Relative to SK	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$	100 100 200 400			ns
t_{PD1}	Output Delay to '1'	AC Test	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$			250 250 500 1000	ns
t_{PD0}	Output Delay to '0'	AC Test	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$			250 250 500 1000	ns
t_{SV}	CS to Status Valid	AC Test	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$			250 250 500 1000	ns
t_{DF}	CS to DO in High Impedance	AC Test CS = V_{IL}	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$			100 100 200 400	ns
t_{WP}	Write Cycle Time			0.1		10	ms
			$4.5V \le V_{CC} \le 5.5V$		1		ms
Endurance[1]	5.0V, 25°C, Page Mode			1M			Write Cycle

Note: 1. This parameter is characterized and is not 100% tested.

Instruction Set for the AT93C46A

Instruction	SB	Op Code	Address x 16	Comments
READ	1	10	A_5 - A_0	Reads data stored in memory, at specified address.
EWEN	1	00	11XXXX	Write enable must precede all programming modes.
ERASE	1	11	A_5 - A_0	Erase memory location A_n - A_0.
WRITE	1	01	A_5 - A_0	Writes memory location A_n - A_0.
ERAL	1	00	10XXXX	Erases all memory locations. Valid only at V_{CC} = 4.5V to 5.5V.
WRAL	1	00	01XXXX	Writes all memory locations. Valid only at V_{CC} = 4.5V to 5.5V.
EWDS	1	00	00XXXX	Disables all programming instructions.

Functional Description

The AT93C46A is accessed via a simple and versatile three-wire serial communication interface. Device operation is controlled by seven instructions issued by the host processor. **A valid instruction starts with a rising edge of CS** and consists of a Start Bit (logic "1") followed by the appropriate Op Code and the desired memory Address location.

READ (READ): The Read (READ) instruction contains the Address code for the memory location to be read. After the instruction and address are decoded, data from the selected memory location is available at the serial output pin DO. Output data changes are synchronized with the rising edges of serial clock SK. It should be noted that a dummy bit (logic "0") precedes the 16-bit data output string.

ERASE/WRITE (EWEN): To assure data integrity, the part automatically goes into the Erase/Write Disable (EWDS) state when power is first applied. An Erase/Write Enable (EWEN) instruction must be executed first before any programming instructions can be carried out. Please note that once in the Erase/Write Enable state, programming remains enabled until an Erase/Write Disable (EWDS) instruction is executed or V_{CC} power is removed from the part.

ERASE (ERASE): The Erase (ERASE) instruction programs all bits in the specified memory location to the logical "1" state. The self-timed erase cycle starts once the ERASE instruction and address are decoded. The DO pin outputs the READY/BUSY status of the part if CS is brought high after being kept low for a minimum of 250 ns (t_{CS}). A logic "1" at pin DO indicates that the selected memory location has been erased, and the part is ready for another instruction.

WRITE (WRITE): The Write (WRITE) instruction contains the 16 bits of data to be written into the specified memory location. The self-timed programming cycle, t_{WP}, starts after the last bit of data is received at serial data input pin DI. The DO pin outputs the READY/BUSY status of the part if CS is brought high after being kept low for a minimum of 250 ns (t_{CS}). A logic "0" at DO indicates that programming is still in progress. A logic "1" indicates that the memory location at the specified address has been written with the data pattern contained in the instruction and the part is ready for further instructions. **A READY/BUSY status cannot be obtained if the CS is brought high after the end of the self-timed programming cycle, t_{WP}.**

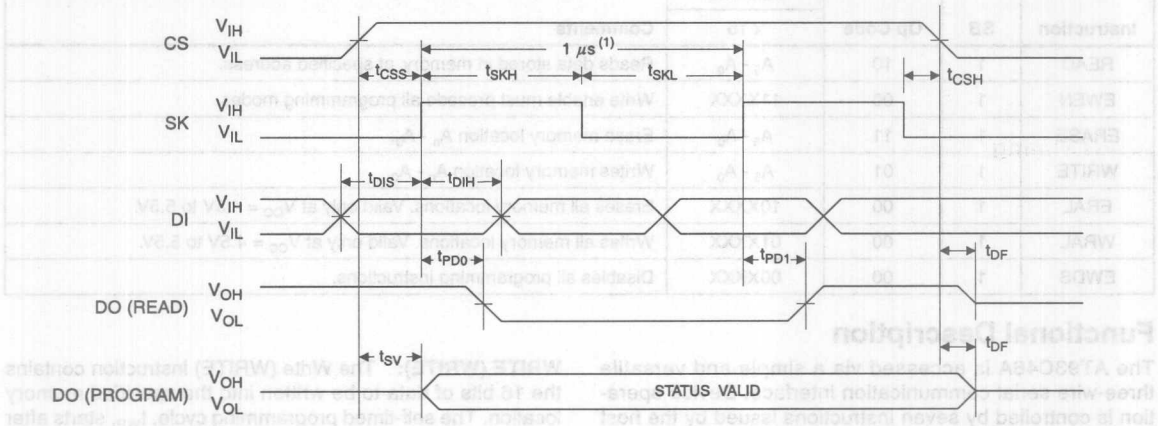
ERASE ALL (ERAL): The Erase All (ERAL) instruction programs every bit in the memory array to the logic "1" state and is primarily used for testing purposes. The DO pin outputs the READY/BUSY status of the part if CS is brought high after being kept low for a minimum of 250 ns (t_{CS}). The ERAL instruction is valid only at V_{CC} = 5.0V ± 10%.

WRITE ALL (WRAL): The Write All (WRAL) instruction programs all memory locations with the data patterns specified in the instruction. The DO pin outputs the READY/BUSY status of the part if CS is brought high after being kept low for a minimum of 250 ns (t_{CS}). The WRAL instruction is valid only at V_{CC} = 5.0V ± 10%.

ERASE/WRITE DISABLE (EWDS): To protect against accidental data disturb, the Erase/Write Disable (EWDS) instruction disables all programming modes and should be executed after all programming operations. The operation of the READ instruction is independent of both the EWEN and EWDS instructions and can be executed at any time.

Timing Diagrams

Synchronous Data Timing

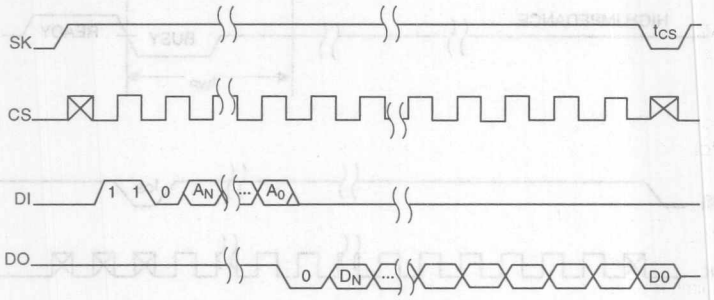


Note: 1. This is the minimum SK period.

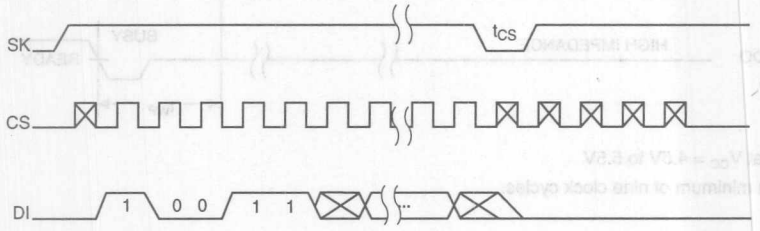
Organization Key for Timing Diagrams

	AT93C46A
I/O	x 16
A_N	A_5
D_N	D_{15}

READ Timing

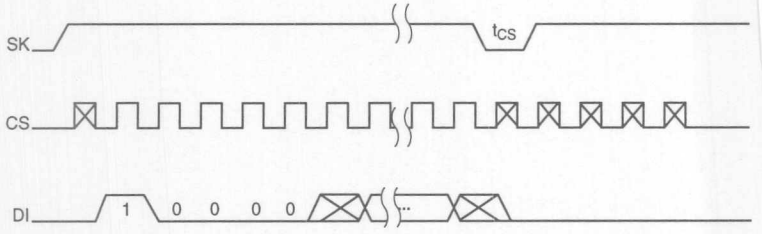


EWEN Timing(1)



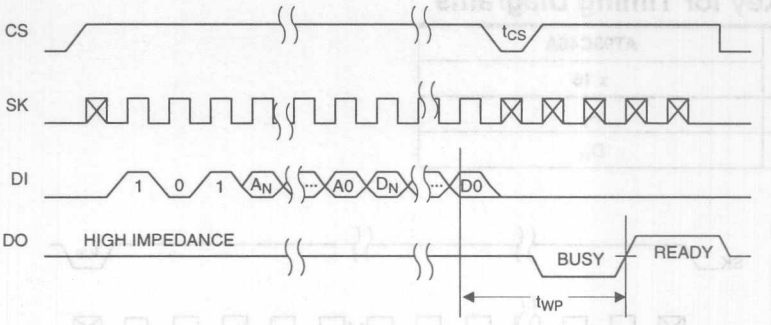
Note: 1. Requires a minimum of nine clock cycles.

EWDS Timing(1)

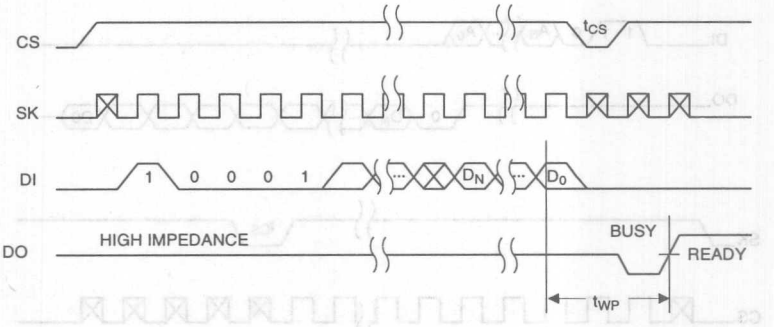


Note: 1. Requires a minimum of nine clock cycles.

WRITE Timing

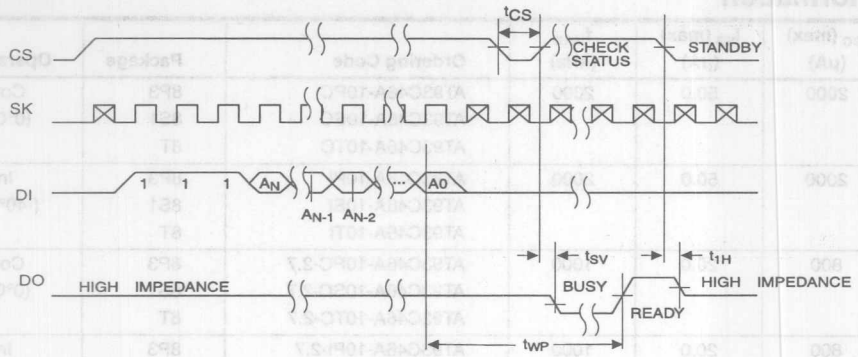


WRAL Timing[1][2]

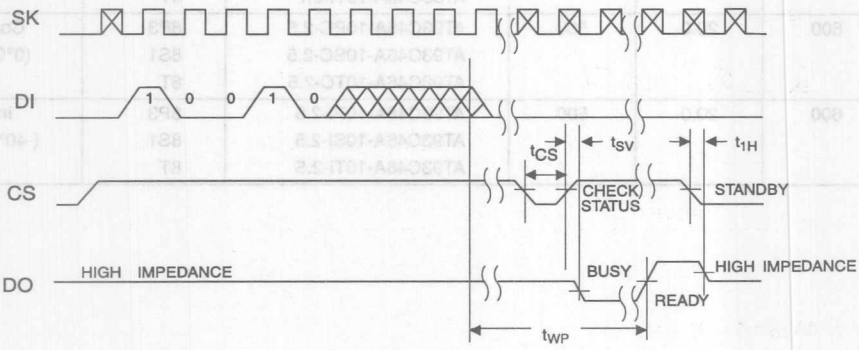


Notes: 1. Valid only at V_{CC} = 4.5V to 5.5V.
2. Requires a minimum of nine clock cycles.

ERASE Timing



TERAL Timing(1)



Note: 1. Valid only at V_{CC} = 4.5V to 5.5V.

Ordering Information

t_{WP} (max) (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	2000	50.0	2000	AT93C46A-10PC AT93C46A-10SC AT93C46A-10TC	8P3 8S1 8T	Commercial (0°C to 70°C)
10	2000	50.0	2000	AT93C46A-10PI AT93C46A-10SI AT93C46A-10TI	8P3 8S1 8T	Industrial (-40°C to 85°C)
10	800	20.0	1000	AT93C46A-10PC-2.7 AT93C46A-10SC-2.7 AT93C46A-10TC-2.7	8P3 8S1 8T	Commercial (0°C to 70°C)
10	800	20.0	1000	AT93C46A-10PI-2.7 AT93C46A-10SI-2.7 AT93C46A-10TI-2.7	8P3 8S1 8T	Industrial (-40°C to 85°C)
10	600	20.0	500	AT93C46A-10PC-2.5 AT93C46A-10SC-2.5 AT93C46A-10TC-2.5	8P3 8S1 8T	Commercial (0°C to 70°C)
10	600	20.0	500	AT93C46A-10PI-2.5 AT93C46A-10SI-2.5 AT93C46A-10TI-2.5	8P3 8S1 8T	Industrial (-40°C to 85°C)

Package Type	
8P3	8-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8T	8-Lead, 0.170" Wide, Thin Small Outline Package (TSSOP)
Options	
Blank	Standard Device (4.5V to 5.5V)
-2.7	Low Voltage (2.7V to 5.5V)
-2.5	Low Voltage (2.5V to 5.5V)

Features

- Low-Voltage and Standard-Voltage Operation
  - 5.0 (V_{CC} = 4.5V to 5.5V)
  - 2.7 (V_{CC} = 2.7V to 5.5V)
  - 2.5 (V_{CC} = 2.5V to 5.5V)
- 3-Wire Serial Interface
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- 2 MHz Clock Rate (5V) Compatibility
- Self-Timed Write Cycle (10 ms max)
- High Reliability
  - Endurance: 1 Million Write Cycles
  - Data Retention: 100 Years
  - ESD Protection: >4000V
- Automotive Grade and Extended Temperature Devices Available
- 8-Pin PDIP and JEDEC SOIC Packages

Description

The AT93C46C provides 1024 bits of serial electrically-erasable programmable read only memory (EEPROM) organized as 64 words of 16 bits each. The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operation are essential. The AT93C46C is available in space saving 8-pin PDIP and 8-pin JEDEC SOIC packages.

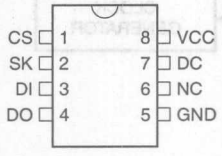
The AT93C46C is enabled through the Chip Select pin (CS), and accessed via a 3-wire serial interface consisting of Data Input (DI), Data Output (DO), and Shift Clock (SK). Upon receiving a READ instruction at DI, the address is decoded and the data is clocked out serially on the data output pin DO. The WRITE cycle is completely self-timed and no separate ERASE cycle is required before WRITE. The WRITE cycle is only enabled when the part is in the ERASE/WRITE ENABLE state. When CS is brought "high" following the initiation of a WRITE cycle, the DO pin outputs the READY/BUSY status of the part.

The AT93C46C is available in 4.5V to 5.5V, 2.7V to 5.5V, and 2.5V to 5.5V versions.

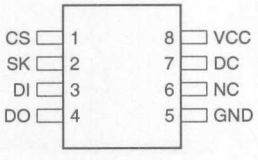
Pin Configurations

Pin Name	Function
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
VCC	Power Supply
NC	No Connect
DC	Don't Connect

8-Pin PDIP



8-Pin SOIC



3-Wire Serial EEPROM

1K (64 x 16)

AT93C46C

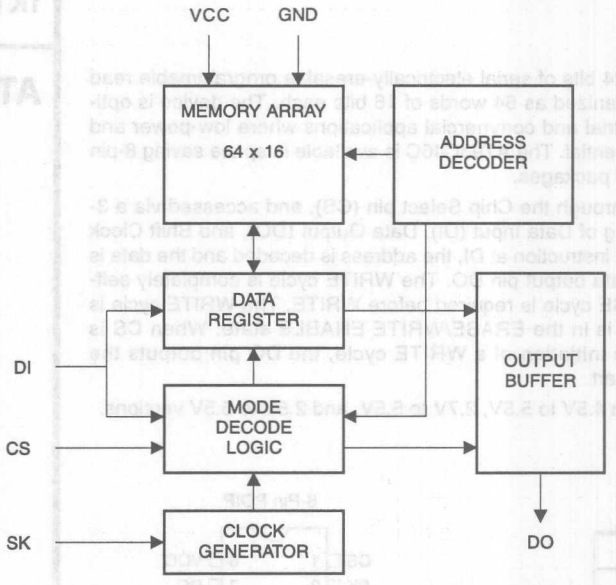
Rev. 1122A–07/98

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Block Diagram



Pin Capacitance[1]

Applicable over recommended operating range from T_A = 25°C, f = 1.0 MHz, V_{CC} = +5.0V (unless otherwise noted).

Symbol	Test Conditions	Max	Units	Conditions
C_{OUT}	Output Capacitance (DO)	5	pF	V_{OUT} = 0V
C_{IN}	Input Capacitance (CS, SK, DI)	5	pF	V_{IN} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

DC Characteristics

Applicable over recommended operating range from: T_{AI} = -40°C to +85°C, V_{CC} = +2.5V to +5.5V, T_{AC} = 0°C to +70°C, V_{CC} = +2.5V to +5.5V (unless otherwise noted).

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
V_{CC1}	Supply Voltage			2.5		5.5	V
V_{CC2}	Supply Voltage			2.7		5.5	V
V_{CC3}	Supply Voltage			4.5		5.5	V
I_{CC}	Supply Current	V_{CC} = 5.0V	READ at 1.0 MHz		0.5	2.0	mA
			WRITE at 1.0 MHz		0.5	2.0	mA
I_{SB1}	Standby Current	V_{CC} = 2.5V	CS = 0V		14.0	20.0	µA
I_{SB2}	Standby Current	V_{CC} = 2.7V	CS = 0V		14.0	20.0	µA
I_{SB3}	Standby Current	V_{CC} = 5.0V	CS = 0V		35.0	50.0	µA
I_{IL}	Input Leakage	V_{IN} = 0V to V_{CC}			0.1	1.0	µA
I_{OL}	Output Leakage	V_{IN} = 0V to V_{CC}			0.1	1.0	µA
V_{IL1}[1] V_{IH1}[1]	Input Low Voltage Input High Voltage	2.5V ≤ V_{CC} ≤ 5.5V		-0.6 V_{CC} x 0.7		V_{CC} x 0.3 V_{CC} + 1	V
V_{OL1}	Output Low Voltage	4.5V ≤ V_{CC} ≤ 5.5V	I_{OL} = 2.1 mA			0.4	V
V_{OH1}	Output High Voltage		I_{OH} = -0.4 mA	2.4			V
V_{OL2}	Output Low Voltage	2.5V ≤ V_{CC} ≤ 2.7V	I_{OL} = 0.15 mA			0.2	V
V_{OH2}	Output High Voltage		I_{OH} = -100 µA	V_{CC} - 0.2			V

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

AC Characteristics

Applicable over recommended operating range from T_A = -40°C to + 85°C, V_{CC} = +2.5V to + 5.5V, CL = 1 TTL Gate and 100 pF (unless otherwise noted).

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
f_{SK}	SK Clock Frequency	4.5V ≤ V_{CC} ≤ 5.5V 2.7V ≤ V_{CC} ≤ 5.5V 2.5V ≤ V_{CC} ≤ 5.5V	0 0 0		2 1 0.5	MHz
t_{SKH}	SK High Time	4.5V ≤ V_{CC} ≤ 5.5V 2.7V ≤ V_{CC} ≤ 5.5V 2.5V ≤ V_{CC} ≤ 5.5V	250 250 500			ns
t_{SKL}	SK Low Time	4.5V ≤ V_{CC} ≤ 5.5V 2.7V ≤ V_{CC} ≤ 5.5V 2.5V ≤ V_{CC} ≤ 5.5V	250 250 500			ns

AC Characteristics (Continued)

Applicable over recommended operating range from T_A = -40°C to + 85°C, V_{CC} = +2.5V to + 5.5V, CL = 1 TTL Gate and 100 pF (unless otherwise noted).

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
t_{CS}	Minimum CS Low Time	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$		250 250 500			ns
t_{CSS}	CS Setup Time	Relative to SK	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$	50 50 100			ns
t_{DIS}	DI Setup Time	Relative to SK	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$	100 100 200			ns
t_{CSH}	CS Hold Time	Relative to SK		0			ns
t_{DIH}	DI Hold Time	Relative to SK	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$	100 100 200			ns
t_{PD1}	Output Delay to '1'	AC Test	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$			250 250 500	ns
t_{PD0}	Output Delay to '0'	AC Test	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$			250 250 500	ns
t_{SV}	CS to Status Valid	AC Test	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$			250 250 500	ns
t_{DF}	CS to DO in High Impedance	AC Test CS = V_{IL}	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$			100 100 200	ns
t_{WP}	Write Cycle Time			0.1		10	ms
			$4.5V \le V_{CC} \le 5.5V$		1		ms
Endurance[1]	5.0V, 25°C, Page Mode			1 M			Write Cycle

Note: 1. This parameter is characterized and is not 100% tested.

Instruction Set for the AT93C46C

Instruction	SB	Op Code	Address x 16	Comments
READ	1	10	A_5 - A_0	Reads data stored in memory, at specified address.
EWEN	1	00	11XXXX	Write enable must precede all programming modes.
ERASE	1	11	A_5 - A_0	Erase memory location A_n - A_0.
WRITE	1	01	A_5 - A_0	Writes memory location A_n - A_0.
ERAL	1	00	10XXXX	Erases all memory locations. Valid only at V_{CC} = 4.5V to 5.5V.
WRAL	1	00	01XXXX	Writes all memory locations. Valid only at V_{CC} = 4.5V to 5.5V.
EWDS	1	00	00XXXX	Disables all programming instructions.

Functional Description

The AT93C46C is accessed via a simple and versatile three-wire serial communication interface. Device operation is controlled by seven instructions issued by the host processor. **A valid instruction starts with a rising edge of CS** and consists of a Start Bit (logic "1") followed by the appropriate Op Code and the desired memory Address location.

READ (READ): The Read (READ) instruction contains the Address code for the memory location to be read. After the instruction and address are decoded, data from the selected memory location is available at the serial output pin DO. Output data changes are synchronized with the rising edges of serial clock SK. It should be noted that a dummy bit (logic "0") precedes the 16-bit data output string.

ERASE/WRITE (EWEN): To assure data integrity, the part automatically goes into the Erase/Write Disable (EWDS) state when power is first applied. An Erase/Write Enable (EWEN) instruction must be executed first before any programming instructions can be carried out. Please note that once in the Erase/Write Enable state, programming remains enabled until an Erase/Write Disable (EWDS) instruction is executed or V_{CC} power is removed from the part.

ERASE (ERASE): The Erase (ERASE) instruction programs all bits in the specified memory location to the logical "1" state. The self-timed erase cycle starts once the ERASE instruction and address are decoded. The DO pin outputs the READY/BUSY status of the part if CS is brought high after being kept low for a minimum of 250 ns (t_{CS}). A logic "1" at pin DO indicates that the selected memory location has been erased, and the part is ready for another instruction.

WRITE (WRITE): The Write (WRITE) instruction contains the 16 bits of data to be written into the specified memory location. The self-timed programming cycle t_W starts after the last bit of data is received at serial data input pin DI. The DO pin outputs the READY/BUSY status of the part if CS is brought high after being kept low for a minimum of 250 ns (t_{CS}). A logic "0" at DO indicates that programming is still in progress. A logic "1" indicates that the memory location at the specified address has been written with the data pattern contained in the instruction and the part is ready for further instructions. **A Ready/Busy Status cannot be obtained if the CS is brought high after the end of the self-timed programming cycle, t_{WP}.**

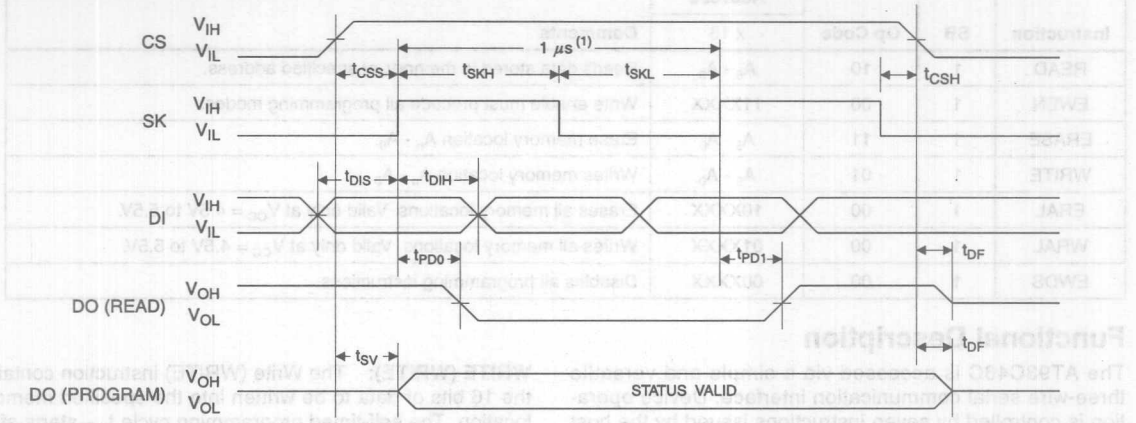
ERASE ALL (ERAL): The Erase All (ERAL) instruction programs every bit in the memory array to the logic "1" state and is primarily used for testing purposes. The DO pin outputs the READY/BUSY status of the part if CS is brought high after being kept low for a minimum of 250 ns (t_{CS}). The ERAL instruction is valid only at V_{CC} = 5.0V ± 10%.

WRITE ALL (WRAL): The Write All (WRAL) instruction programs all memory locations with the data patterns specified in the instruction. The DO pin outputs the READY/BUSY status of the part if CS is brought high after being kept low for a minimum of 250 ns (t_{CS}). The WRAL instruction is valid only at V_{CC} = 5.0V ± 10%.

ERASE/WRITE DISABLE (EWDS): To protect against accidental data disturb, the Erase/Write Disable (EWDS) instruction disables all programming modes and should be executed after all programming operations. The operation of the READ instruction is independent of both the EWEN and EWDS instructions and can be executed at any time.

Timing Diagrams

Synchronous Data Timing

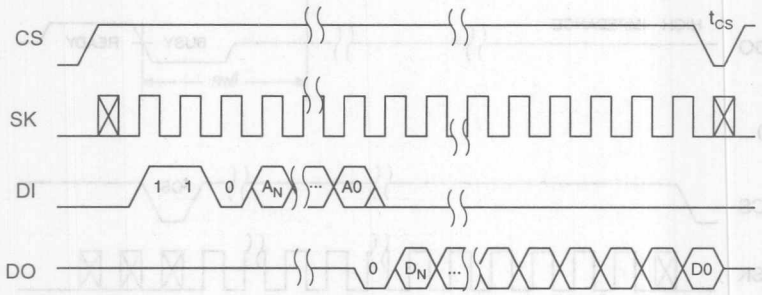


Note: 1. This is the minimum SK period.

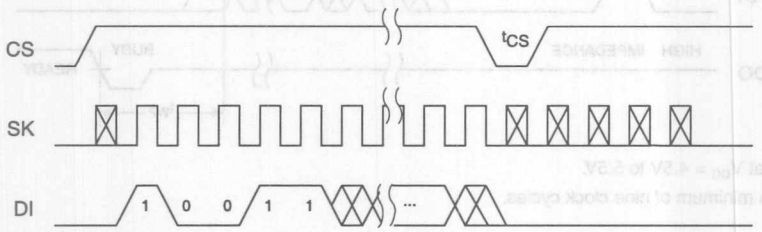
Organization Key for Timing Diagrams

	AT93C46C
I/O	x 16
A_N	A_5
D_N	D_{15}

READ Timing

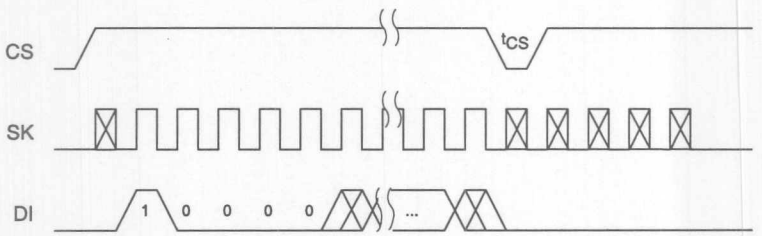


EWEN Timing(1)



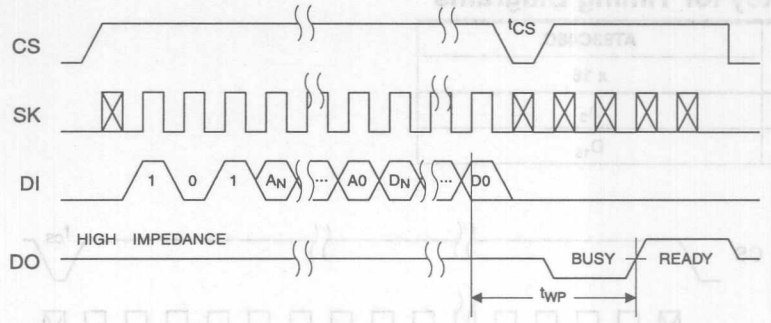
Note: 1. Requires a minimum of nine clock cycles.

EWDS Timing(1)

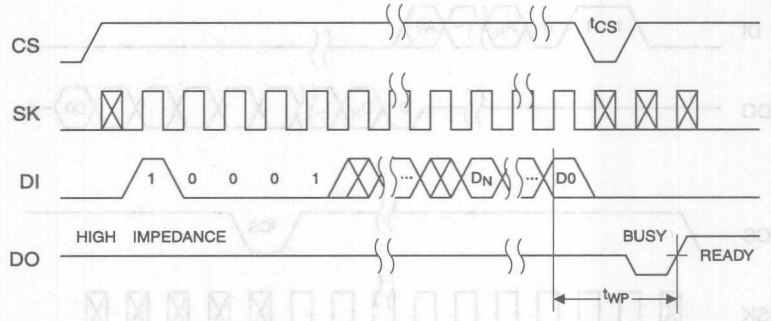


Note: 1. Requires a minimum of nine clock cycles.

WRITE Timing

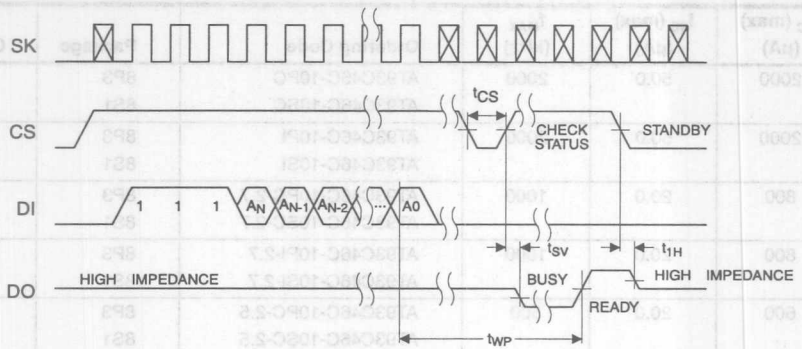


WRAL Timing[1][2]

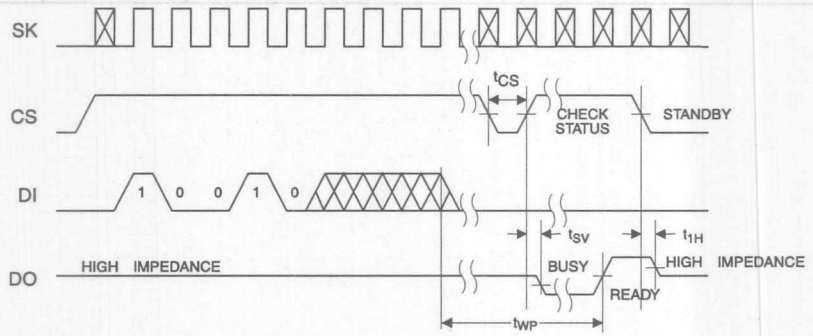


Notes: 1. Valid only at V_{CC} = 4.5V to 5.5V.
2. Requires a minimum of nine clock cycles.

ERASE Timing



TERAL Timing[1]



Note: 1. Valid only at V_{CC} = 4.5V to 5.5V.

Ordering Information

t_{WP} (max) (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	2000	50.0	2000	AT93C46C-10PC AT93C46C-10SC	8P3 8S1	Commercial (0°C to 70°C)
10	2000	50.0	2000	AT93C46C-10PI AT93C46C-10SI	8P3 8S1	Industrial (-40°C to 85°C)
10	800	20.0	1000	AT93C46C-10PC-2.7 AT93C46C-10SC-2.7	8P3 8S1	Commercial (0°C to 70°C)
10	800	20.0	1000	AT93C46C-10PI-2.7 AT93C46C-10SI-2.7	8P3 8S1	Industrial (-40°C to 85°C)
10	600	20.0	500	AT93C46C-10PC-2.5 AT93C46C-10SC-2.5	8P3 8S1	Commercial (0°C to 70°C)
10	600	20.0	500	AT93C46C-10PI-2.5 AT93C46C-10SI-2.5	8P3 8S1	Industrial (-40°C to 85°C)

Package Type	
8P3	8-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
Options	
Blank	Standard Device (4.5V to 5.5V)
-2.7	Low Voltage (2.7V to 5.5V)
-2.5	Low Voltage (2.5V to 5.5V)

Features

- Low Voltage and Standard Voltage Operation
  - 5.0 (V_{CC} = 4.5V to 5.5V)
  - 2.7 (V_{CC} = 2.7V to 5.5V)
  - 2.5 (V_{CC} = 2.5V to 5.5V)
- User Selectable Internal Organization
  - 1K: 128 x 8 or 64 x 16
  - 2K: 256 x 8 or 128 x 16
  - 4K: 512 x 8 or 256 x 16
- 4-Wire Serial Interface
- Self-Timed Write Cycle (10 ms max)
- High Reliability
  - Endurance: 1 Million Write Cycles
  - Data Retention: 100 Years
  - ESD Protection: >4000V
- 8-Pin PDIP and 8-Pin EIAJ SOIC Packages

Description

The AT59C11/22/13 provides 1024/2048/4096 bits of serial EEPROM (Electrically Erasable Programmable Read Only Memory) organized as 64/128/256 words of 16 bits each, when the ORG Pin is connected to V_{CC} and 128/256/512 words of 8 bits each when it is tied to ground. The device is optimized for use in many industrial and commercial applications where low power and low voltage operation are essential. The AT59C11/22/13 is available in space saving 8-pin PDIP and 8-pin EIAJ SOIC packages.

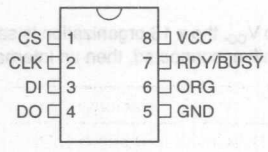
The AT59C11/22/13 is enabled through the Chip Select pin (CS), and accessed via a 4-wire serial interface consisting of Data Input (DI), Data Output (DO), and Clock (CLK). Upon receiving a READ instruction at DI, the address is decoded and the data is clocked out serially on the data output pin DO, the WRITE cycle is completely self-timed and no separate ERASE cycle is required before WRITE. The WRITE cycle is only enabled when the part is in the ERASE/WRITE ENABLE state. Ready/$\overline{\text{Busy}}$ status can be monitored upon completion of a programming operation by polling the Ready/$\overline{\text{Busy}}$ pin.

The AT59C11/22/13 is available in 5.0V ± 10%, 2.7V to 5.5V and 2.5V to 5.5V versions.

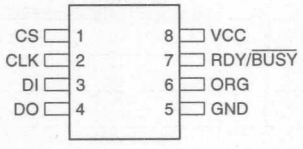
Pin Configurations

Pin Name	Function
CS	Chip Select
CLK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
VCC	Power Supply
ORG	Internal Organization
RDY/$\overline{\text{BUSY}}$	Status Output

8-Pin PDIP



8-Pin SOIC



2

4-Wire Serial EEPROMs

1K (128 x 8 or 64 x 16)

2K (256 x 8 or 128 x 16)

4K (512 x 8 or 256 x 16)

AT59C11
AT59C22
AT59C13

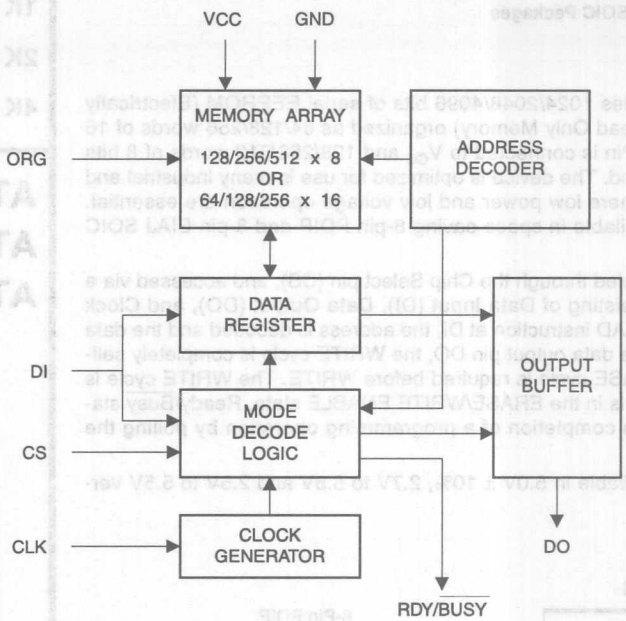
Rev. 0173K–07/98

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under Maximum Ratings" may cause perma age to the device. This is a stress ratin functional operation of the device at thes other conditions beyond those indicated i operational sections of this specification is implied. Exposure to absolute maximum rati conditions for extended periods may affect device reliability

Block Diagram(1)



Note: 1. When the ORG pin is connected to V_{CC}, the x 16 organization is selected. When it is connected to ground, the x 8 organization is selected. If the ORG pin is left unconnected, then an internal pullup device will select the x 16 organization.

Pin Capacitance[1]

Applicable over recommended operating range from T_A = 25°C, f = 1.0 MHz, V_{CC} = +5.0V (unless otherwise noted).

Symbol	Test Conditions	Max	Units	Conditions
C_{OUT}	Output Capacitance (DO)	5	pF	V_{OUT} = 0V
C_{IN}	Input Capacitance (CS, CLK, DI, RDY/$\overline{BUSY}$)	5	pF	V_{IN} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

2

DC Characteristics

Applicable over recommended operating range from: T_{AI} = -40°C to +85°C, V_{CC} = +2.5V to +5.5V, T_{AC} = 0°C to +70°C, V_{CC} = +2.5V to +5.5V (unless otherwise noted).

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
V_{CC1}	Supply Voltage			1.8		5.5	V
V_{CC2}	Supply Voltage			2.5		5.5	V
V_{CC3}	Supply Voltage			2.7		5.5	V
V_{CC4}	Supply Voltage			4.5		5.5	V
I_{CC}	Supply Current	V_{CC} = 5.0V	READ at 1.0 MHz		0.5	2.0	mA
			WRITE at 1.0 MHz		0.5	2.0	mA
I_{SB1}	Standby Current	V_{CC} = 2.5V	CS = 0V		6.0	10.0	µA
I_{SB2}	Standby Current	V_{CC} = 2.7V	CS = 0V		6.0	10.0	µA
I_{SB3}	Standby Current	V_{CC} = 5.0V	CS = 0V		21.0	30.0	µA
I_{IL}	Input Leakage	V_{IN} = 0V to V_{CC}			0.1	1.0	µA
I_{OL}	Output Leakage	V_{IN} = 0V to V_{CC}			0.1	1.0	µA
V_{IL1}[1] V_{IH1}[1]	Input Low Voltage Input High Voltage	4.5V ≤ V_{CC} ≤ 5.5V		-0.6 2.0		0.8 V_{CC} + 1	V
V_{IL2}[1] V_{IH2}[1]	Input Low Voltage Input High Voltage	2.5V ≤ V_{CC} ≤ 2.7V		-0.6 V_{CC} x 0.7		V_{CC} x 0.3 V_{CC} + 1	V
V_{OL1} V_{OH1}	Output Low Voltage Output High Voltage	4.5V ≤ V_{CC} ≤ 5.5V	I_{OL} = 2.1 mA I_{OH} = 0.4 mA	 2.4		0.4	V
V_{OL2} V_{OH2}	Output Low Voltage Output High Voltage	2.5V ≤ V_{CC} ≤ 2.7V	I_{OL} = 0.15 mA I_{OH} = -0.1 mA	 V_{CC} - 0.2		0.2	V

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

AC Characteristics

Applicable over recommended operating range from T_A = -40°C to +85°C, V_{CC} = +2.5V to +5.5V, CL = 1 TTL Gate and 100 pF (unless otherwise noted).

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
f_{CLK}	CLK Clock Frequency	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$		0 0 0 0		1 1 0.5 0.25	MHz
t_{CKH}	CLK High Time	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$		250 250 500 1000			ns
t_{CKL}	CLK Low Time	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$		250 250 500 1000			ns
t_{CS}	Minimum CS Low Time	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$		250 250 500 1000			ns
t_{CSS}	CS Setup Time	Relative to SK	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$	50 50 100 200			ns
t_{DIS}	DI Setup Time	Relative to SK	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$	100 100 200 400			ns
t_{CSH}	CS Hold Time	Relative to SK		0			ns
t_{DIH}	DI Hold Time	Relative to SK	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$	100 100 200 400			ns
t_{PD1}	Output Delay to '1'	AC Test	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$			250 250 500 1000	ns
t_{PD0}	Output Delay to '0'	AC Test	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$			250 250 500 1000	ns
t_{RBD}	RDY/$\overline{BUSY}$ Delay to Status Valid	AC Test	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$			250 250 500 1000	ns
t_{CZ}	CS to DO in High Impedance	AC Test CS = V_{IL}	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$			100 100 200 400	ns
t_{WC}	Write Cycle Time			0.1		10	ms
Endurance[1]	5.0V, 25°C, Page Mode			1M			Write Cycles

Note: 1. This paramter is characterized and is not 100% tested.

Instruction Set for the AT59C11

Instruction	SB	Op Code	Address		Data		Comments
			x 8	x 16	x 8	x 16	
READ	1	10XX	A_6 - A_0	A_5 - A_0			Reads data stored in memory, at specified address.
EWEN	1	0011	XXXXXXX	XXXXXX			Write enable must precede all programming modes.
WRITE	1	X1XX	A_6 - A_0	A_5 - A_0	D_7 - D_0	D_{15} - D_0	Writes memory location A_n - A_0.
ERAL	1	0010	XXXXXXX	XXXXXX			Erases all memory locations. Valid only at V_{CC} = 4.5V to 5.5V.
WRAL	1	0001	XXXXXXX	XXXXXX	D_7 - D_0	D_{15} - D_0	Writes all memory locations. Valid only at V_{CC} = 4.5V to 5.5V.
EWDS	1	0000	XXXXXXX	XXXXXX			Disables all programming instructions.

Instruction Set for the AT59C22

Instruction	SB	Op Code	Address		Data		Comments
			x 8	x 16	x 8	x 16	
READ	1	10XX	A_7 - A_0	A_6 - A_0			Reads data stored in memory, at specified address.
EWEN	1	0011	XXXXXXXX	XXXXXXX			Write enable must precede all programming modes.
WRITE	1	X1XX	A_7 - A_0	A_6 - A_0	D_7 - D_0	D_{15} - D_0	Writes memory location A_n - A_0.
ERAL	1	0010	XXXXXXXX	XXXXXXX			Erases all memory locations. Valid only at V_{CC} = 4.5V to 5.5V.
WRAL	1	0001	XXXXXXXX	XXXXXXX	D_7 - D_0	D_{15} - D_0	Writes all memory locations. Valid when V_{CC} = 5.0V ± 10% and Disable Register cleared.
EWDS	1	0000	XXXXXXXX	XXXXXXX			Disables all programming instructions.

Instruction Set for the AT59C13

Instruction	SB	Op Code	Address		Data		Comments
			x 8	x 16	x 8	x 16	
READ	1	10XX	A_8 - A_0	A_7 - A_0			Reads data stored in memory, at specified address.
EWEN	1	0011	XXXXXXXXX	XXXXXXXX			Write enable must precede all programming modes.
WRITE	1	X1XX	A_8 - A_0	A_7 - A_0	D_7 - D_0	D_{15} - D_0	Writes memory location A_n - A_0.
ERAL	1	0010	XXXXXXXXX	XXXXXXXX			Erases all memory locations. Valid only at V_{CC} = 4.5V to 5.5V.
WRAL	1	0001	XXXXXXXXX	XXXXXXXX	D_7 - D_0	D_{15} - D_0	Writes all memory locations. Valid when V_{CC} = 5.0V ± 10% and Disable Register cleared.
EWDS	1	0000	XXXXXXXXX	XXXXXXXX			Disables all programming instructions.

Functional Description

The AT59C11/22/13 are accessed via a simple and versatile 4-wire serial communication interface. Device operation is controlled by six instructions issued by the host processor. **A valid instruction starts with a rising edge of CS** and consists of a Start Bit (logic "1") followed by the appropriate Op Code and the desired memory Address location.

READ (READ): The Read (READ) instruction contains the Address code for the memory location to be read. After the instruction and address are decoded, data from the selected memory location is available at the serial output pin DO. Output data changes are synchronized with the rising edges of serial clock CLK. It should be noted that a dummy bit (logic "0") precedes the 8- or 16-bit data output string.

ERASE/WRITE (EWEN): To assure data integrity, the part automatically goes into the Erase/Write Disable (EWDS) state when power is first applied. An Erase/Write Enable (EWEN) instruction must be executed first before any programming instructions can be carried out. Please note that once in the Erase/Write Enable state, programming remains enabled until an Erase/Write Disable (EWDS) instruction is executed or V_{CC} power is removed from the part.

WRITE (WRITE): The Write (WRITE) instruction contains the 8 or 16 bits of data to be written into the specified memory location. The self-timed programming cycle, t_{WP}, starts after the last bit of data is received at serial data input pin DI. The Ready/$\overline{\text{Busy}}$ status of the AT59C11/22/13 can be determined by polling the RDY/$\overline{\text{BUSY}}$ pin. A logic "0" at RDY/$\overline{\text{BUSY}}$ indicates that programming is still in progress. A logic "1" indicates that the memory location at the specified address has been written with the data pattern contained in the instruction and the part is ready for further instructions.

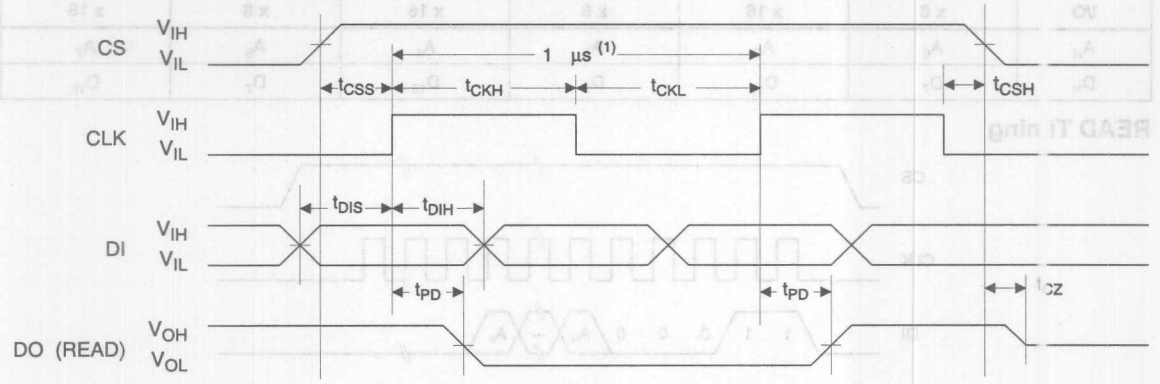
ERASE ALL (ERAL): The Erase All (ERAL) instruction programs every bit in the memory array to the logic "1" state and is primarily used for testing purposes. The Ready/$\overline{\text{Busy}}$ status of the AT59C11/22/13 can be determined by polling the RDY/$\overline{\text{BUSY}}$ pin. The ERAL instruction is valid only at V_{CC} = 5.0V ± 10%.

WRITE ALL (WRAL): The Write All (WRAL) instruction programs all memory locations with the data patterns specified in the instruction. The Ready/$\overline{\text{Busy}}$ status of the AT59C11/22/13 can be determined by polling the RDY/$\overline{\text{BUSY}}$ pin. The WRAL instruction is valid only at V_{CC} = 5.0V ± 10%.

ERASE/WRITE DISABLE (EWDS): To protect against accidental data disturb, the Erase/Write Disable (EWDS) instruction disables all programming modes and should be executed after all programming operations. The operation of the READ instruction is independent of both the EWEN and EWDS instructions and can be executed at any time.

Timing Diagrams

Synchronous Data Timing

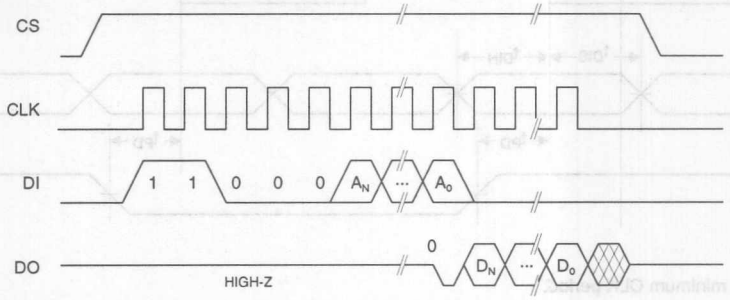


Note: 1. This is the minimum CLK period.

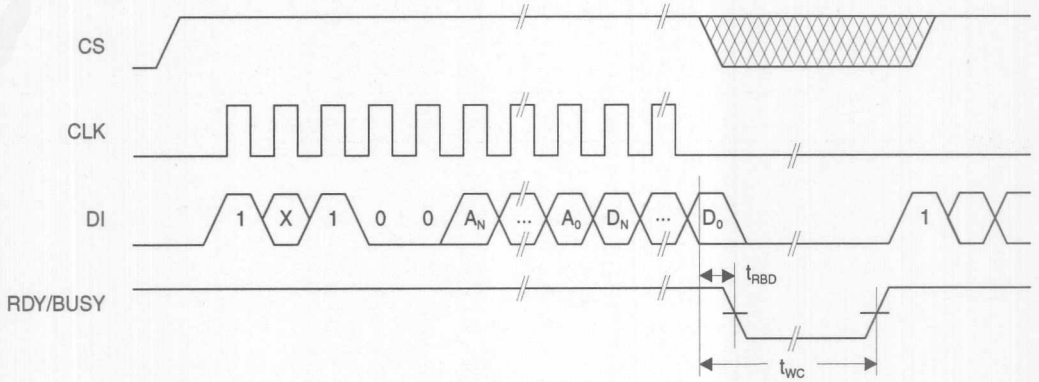
Organization Key for Timing Diagrams

	Density 1K		Density 2K		Density 4K	
I/O	x 8	x 16	x 8	x 16	x 8	x 16
A_N	A_6	A_5	A_7	A_6	A_8	A_7
D_N	D_7	D_{15}	D_7	D_{15}	D_7	D_{15}

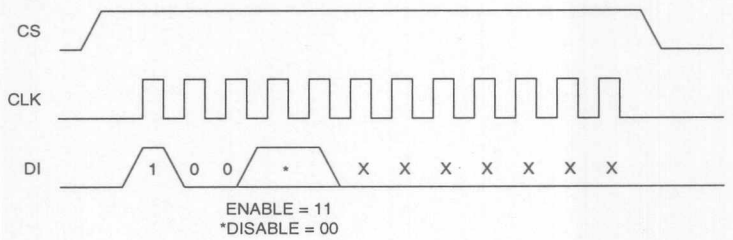
READ Timing



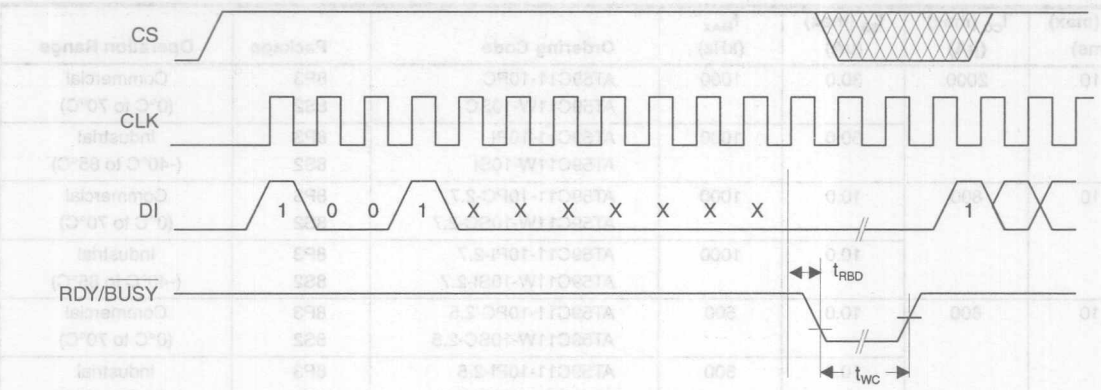
WRITE Timing



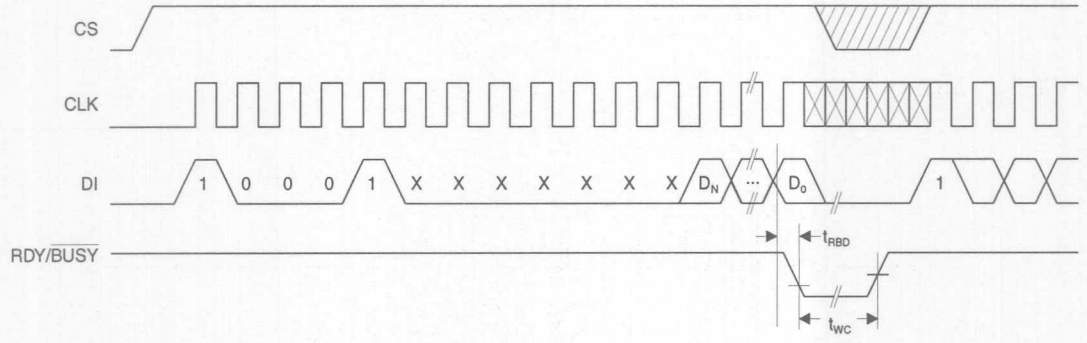
EWEN/EWDS Timing



ERAL Timing



WRAL Timing



AT59C11 Ordering Information

t_{WC} (max) (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	2000	30.0	1000	AT59C11-10PC AT59C11W-10SC	8P3 8S2	Commercial (0°C to 70°C)
		30.0	1000	AT59C11-10PI AT59C11W-10SI	8P3 8S2	Industrial (-40°C to 85°C)
10	800	10.0	1000	AT59C11-10PC-2.7 AT59C11W-10SC-2.7	8P3 8S2	Commercial (0°C to 70°C)
		10.0	1000	AT59C11-10PI-2.7 AT59C11W-10SI-2.7	8P3 8S2	Industrial (-40°C to 85°C)
10	600	10.0	500	AT59C11-10PC-2.5 AT59C11W-10SC-2.5	8P3 8S2	Commercial (0°C to 70°C)
		10.0	500	AT59C11-10PI-2.5 AT59C11W-10SI-2.5	8P3 8S2	Industrial (-40°C to 85°C)

Package Type	
8P3	8-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S2	8-Lead, 0.200" Wide, Plastic Gull Wing Small Outline (EIAJ SOIC)
Options	
Blank	Standard Device (4.5V to 5.5V)
-2.7	Low-Voltage (2.7V to 5.5V)
-2.5	Low-Voltage (2.5V to 5.5V)

AT59C22 Ordering Information

t_{WC} (max) (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	2000	30.0	1000	AT59C22-10PC AT59C22W-10SC	8P3 8S2	Commercial (0°C to 70°C)
		30.0	1000	AT59C22-10PI AT59C22W-10SI	8P3 8S2	Industrial (-40°C to 85°C)
10	800	10.0	1000	AT59C22-10PC-2.7 AT59C22W-10SC-2.7	8P3 8S2	Commercial (0°C to 70°C)
		10.0	1000	AT59C22-10PI-2.7 AT59C22W-10SI-2.7	8P3 8S2	Industrial (-40°C to 85°C)
10	600	10.0	500	AT59C22-10PC-2.5 AT59C22W-10SC-2.5	8P3 8S2	Commercial (0°C to 70°C)
		10.0	500	AT59C22-10PI-2.5 AT59C22W-10SI-2.5	8P3 8S2	Industrial (-40°C to 85°C)

Package Type	
8P3	8-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S2	8-Lead, 0.200" Wide, Plastic Gull Wing Small Outline (EIAJ SOIC)
Options	
Blank	Standard Device (4.5V to 5.5V)
-2.7	Low-Voltage (2.7V to 5.5V)
-2.5	Low-Voltage (2.5V to 5.5V)

AT59C13 Ordering Information

t_{WC} (max) (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	2000	30.0	1000	AT59C13-10PC AT59C13W-10SC	8P3 8S2	Commercial (0°C to 70°C)
		30.0	1000	AT59C13-10PI AT59C13W-10SI	8P3 8S2	Industrial (-40°C to 85°C)
10	800	10.0	1000	AT59C13-10PC-2.7 AT59C13W-10SC-2.7	8P3 8S2	Commercial (0°C to 70°C)
		10.0	1000	AT59C13-10PI-2.7 AT59C13W-10SI-2.7	8P3 8S2	Industrial (-40°C to 85°C)
10	600	10.0	500	AT59C13-10PC-2.5 AT59C13W-10SC-2.5	8P3 8S2	Commercial (0°C to 70°C)
		10.0	500	AT59C13-10PI-2.5 AT59C13W-10SI-2.5	8P3 8S2	Industrial (-40°C to 85°C)

Package Type	
8P3	8-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S2	8-Lead, 0.200" Wide, Plastic Gull Wing Small Outline (EIAJ SOIC)
Options	
Blank	Standard Device (4.5V to 5.5V)
-2.7	Low-Voltage (2.7V to 5.5V)
-2.5	Low-Voltage (2.5V to 5.5V)

Features

- Serial Peripheral Interface (SPI) Compatible
- Supports SPI Modes 0 (0,0) and 3 (1,1)
- Low-Voltage and Standard-Voltage Operation
  - 5.0 (V_{CC} = 4.5V to 5.5V)
  - 2.7 (V_{CC} = 2.7V to 5.5V)
  - 1.8 (V_{CC} = 1.8V to 3.6V)
- 2.1 MHz Clock Rate (5V) Compatibility
- 8-Byte Page Mode
- Block Write Protection
  - Protect 1/4, 1/2, or Entire Array
- Write Protect ($\overline{WP}$) Pin and Write Disable Instructions for Both Hardware and Software Data Protection
- Self-Timed Write Cycle (10 ms max)
- High Reliability
  - Endurance: 1 Million Write Cycles
  - Data Retention: 100 Years
  - ESD Protection: >4000V
- Automotive Grade and Extended Temperature Devices Available
- 8-Pin PDIP and JEDEC SOIC Packages

Description

The AT25010/020/040 provides 1024/2048/4096 bits of serial electrically erasable programmable read only memory (EEPROM) organized as 128/256/512 words of 8 bits each. The device is optimized for use in many industrial and commercial applications where low power and low voltage operation are essential. The AT25010/020/040 is available in space saving 8-pin PDIP and 8-pin JEDEC (SOIC) packages.

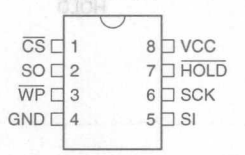
The AT25010/020/040 is enabled through the Chip Select pin ($\overline{CS}$) and accessed via a 3-wire interface consisting of Serial Data Input (SI), Serial Data Output (SO), and Serial Clock (SCK). All programming cycles are completely self-timed, and no separate ERASE cycle is required before WRITE.

BLOCK WRITE protection is enabled by programming the status register with one of four blocks of write protection. Separate program enable and program disable instructions are provided for additional data protection. Hardware data protection is provided via the $\overline{WP}$ pin to protect against inadvertent write attempts. The $\overline{HOLD}$ pin may be used to suspend any serial communication without resetting the serial sequence.

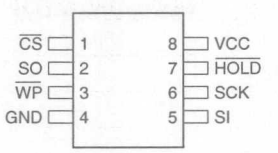
Pin Configurations

Pin Name	Function
$\overline{CS}$	Chip Select
SCK	Serial Data Clock
SI	Serial Data Input
SO	Serial Data Output
GND	Ground
VCC	Power Supply
$\overline{WP}$	Write Protect
$\overline{HOLD}$	Suspends Serial Input

8-Pin PDIP



8-Pin SOIC



2

SPI Serial EEPROMs

1K (128 x 8)

2K (256 x 8)

4K (512 x 8)

AT25010
AT25020
AT25040

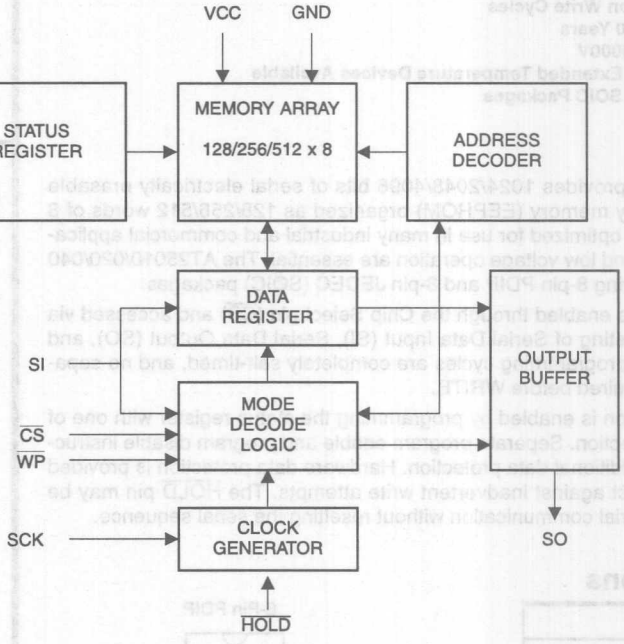
Rev. 0606E–08/98

Absolute Maximum Ratings*

Operating Temperature	-55°C to + 125°C
Storage Temperature	-65°C to + 150°C
Voltage on Any Pin with Respect to Ground	-1.0V to + 7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Block Diagram



Pin Capacitance[1]

Applicable over recommended operating range from T_A = 25°C, f = 1.0 MHz, V_{CC} = +5.0V (unless otherwise noted).

Symbol	Test Conditions	Max	Units	Conditions
C_{OUT}	Output Capacitance (SO)	8	pF	V_{OUT} = 0V
C_{IN}	Input Capacitance ($\overline{CS}$, SCK, SI, $\overline{WP}$, $\overline{HOLD}$)	6	pF	V_{IN} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

DC Characteristics

Applicable over recommended operating range from: T_{AI} = -40°C to +85°C, V_{CC} = +1.8V to +5.5V, T_{AC} = 0°C to +70°C, V_{CC} = +1.8V to +5.5V (unless otherwise noted).

Symbol	Parameter	Test Condition		Min	Max	Units
V_{CC1}[1]	Supply Voltage			1.8	5.5	V
V_{CC2}	Supply Voltage			2.7	5.5	V
V_{CC3}	Supply Voltage			4.5	5.5	V
I_{CC1}	Supply Current	V_{CC} = 5.0V at 1 MHz, SO = Open			3.0	mA
I_{CC2}	Supply Current	V_{CC} = 5.0V at 2 MHz, SO = Open			6.0	mA
I_{SB1}[1]	Standby Current	V_{CC} = 1.8V	$\overline{CS}$ = V_{CC}		100	µA
I_{SB2}	Standby Current	V_{CC} = 2.7V	$\overline{CS}$ = V_{CC}		100	µA
I_{SB3}	Standby Current	V_{CC} = 5.0V	$\overline{CS}$ = V_{CC}		100	µA
I_{IL}	Input Leakage	V_{IN} = 0V to V_{CC}		-0.6	3.0	µA
I_{OL}	Output Leakage	V_{IN} = 0V to V_{CC}, T_{AC} = 0°C to 70°C		-0.6	3.0	µA
V_{IL}[2]	Input Low Voltage			-0.6	V_{CC} x 0.3	V
V_{IH}[2]	Input High Voltage			V_{CC} x 0.7	V_{CC} + 0.5	V
V_{OL1}	Output Low Voltage	4.5V ≤ V_{CC} ≤ 5.5V	I_{OL} = 2.0 mA		0.4	V
V_{OH1}	Output High Voltage		I_{OH} = -1.0 mA	V_{CC} - 0.8		V
V_{OL2}	Output Low Voltage	1.8V ≤ V_{CC} ≤ 3.6V	I_{OL} = 0.15 mA		0.2	V
V_{OH2}	Output High Voltage		I_{OH} = -100 µA	V_{CC} - 0.2		V

Notes: 1. This parameter is preliminary and Atmel may change the specifications upon further characterization.
2. V_{IL} min and V_{IH} max are reference only and are not tested.

AC Characteristics

Applicable over recommended operating range from T_A = -40°C to +85°C, V_{CC} = As Specified, CL = 1 TTL Gate and 100 pF (unless otherwise noted).

Symbol	Parameter	Voltage	Min	Max	Units
f_{SCK}	SCK Clock Frequency	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6	0 0 0	2.1 2.1 0.5	MHz
t_{RI}	Input Rise Time	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6		2 2 2	µs
t_{FI}	Input Fall Time	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6		2 2 2	µs
t_{WH}	SCK High Time	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6	200 200 800		ns
t_{WL}	SCK Low Time	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6	200 200 800		ns
t_{CS}	$\overline{CS}$ High Time	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6	250 250 1000		ns
t_{CSS}	$\overline{CS}$ Setup Time	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6	250 250 1000		ns
t_{CSH}	$\overline{CS}$ Hold Time	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6	250 250 1000		ns
t_{SU}	Data In Setup Time	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6	50 50 100		ns
t_H	Data In Hold Time	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6	50 100 100		ns
t_{HD}	$\overline{Hold}$ Setup Time	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6	100 100 400		ns
t_{CD}	$\overline{Hold}$ Hold Time	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6	200 200 400		ns
t_V	Output Valid	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6	0 0 0	200 400 800	ns
t_{HO}	Output Hold Time	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6	0 0 0		ns

AC Characteristics (Continued)

Applicable over recommended operating range from T_A = -40°C to +85°C, V_{CC} = As Specified, CL = 1 TTL Gate and 100 pF (unless otherwise noted).

Symbol	Parameter	Voltage	Min	Max	Units
t_{LZ}	$\overline{\text{Hold}}$ to Output Low Z	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6	0 0 0	100 100 100	ns
t_{HZ}	$\overline{\text{Hold}}$ to Output High Z	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6		100 100 100	ns
t_{DIS}	Output Disable Time	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6		250 500 1000	ns
t_{WC}	Write Cycle Time	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6		10	ms
Endurance	5.0V, 25°C, Page Mode		1M		Write Cycles

Note: 1. This parameter is characterized and is not 100% tested.

Serial Interface Description

MASTER: The device that generates the serial clock.

SLAVE: Because the Serial Clock pin (SCK) is always an input, the AT25010/020/040 always operates as a slave.

TRANSMITTER/RECEIVER: The AT25010/020/040 has separate pins designated for data transmission (SO) and reception (SI).

MSB: The Most Significant Bit (MSB) is the first bit transmitted and received.

SERIAL OP-CODE: After the device is selected with $\overline{CS}$ going low, the first byte will be received. This byte contains the op-code that defines the operations to be performed. The op-code also contains address bit A8 in both the READ and WRITE instructions.

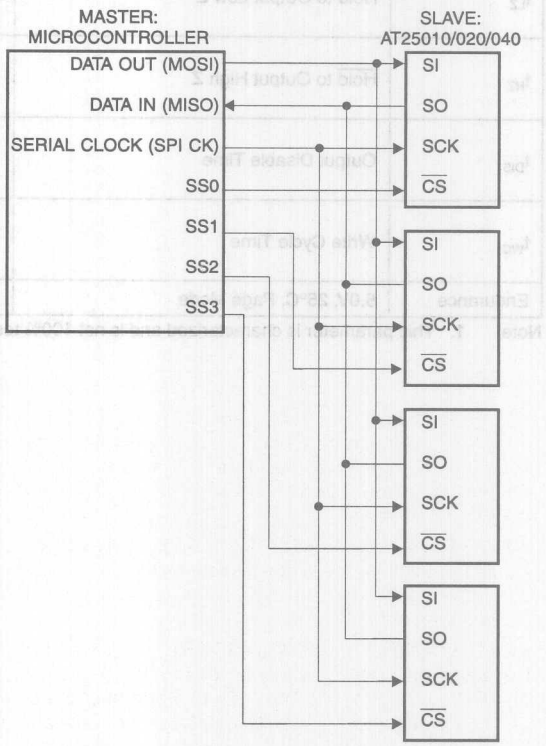
INVALID OP-CODE: If an invalid op-code is received, no data will be shifted into the AT25010/020/040, and the serial output pin (SO) will remain in a high impedance state until the falling edge of $\overline{CS}$ is detected again. This will reinitialize the serial communication.

CHIP SELECT: The AT25010/020/040 is selected when the $\overline{CS}$ pin is low. When the device is not selected, data will not be accepted via the SI pin, and the serial output pin (SO) will remain in a high impedance state.

HOLD: The $\overline{HOLD}$ pin is used in conjunction with the $\overline{CS}$ pin to select the AT25010/020/040. When the device is selected and a serial sequence is underway, $\overline{HOLD}$ can be used to pause the serial communication with the master device without resetting the serial sequence. To pause, the $\overline{HOLD}$ pin must be brought low while the SCK pin is low. To resume serial communication, the $\overline{HOLD}$ pin is brought high while the SCK pin is low (SCK may still toggle during $\overline{HOLD}$). Inputs to the SI pin will be ignored while the SO pin is in the high impedance state.

WRITE PROTECT: The write protect pin ($\overline{WP}$) will allow normal read/write operations when held high. When the $\overline{WP}$ pin is brought low, all write operations are inhibited. $\overline{WP}$ going low while $\overline{CS}$ is still low will interrupt a write to the AT25010/020/040. If the internal write cycle has already been initiated, $\overline{WP}$ going low will have no effect on any write operation.

SPI Serial Interface



Functional Description

The AT25010/020/040 is designed to interface directly with the synchronous serial peripheral interface (SPI) of the 6805 and 68HC11 series of microcontrollers.

The AT25010/020/040 utilizes an 8-bit instruction register. The list of instructions and their operation codes are contained in Table 1. All instructions, addresses, and data are transferred with the MSB first and start with a high-to-low $\overline{CS}$ transition.

Table 1. Instruction Set for the AT25010/020/040

Instruction Name	Instruction Format	Operation
WREN	0000 X110	Set Write Enable Latch
WRDI	0000 X100	Reset Write Enable Latch
RDSR	0000 X101	Read Status Register
WRSR	0000 X001	Write Status Register
READ	0000 A011	Read Data from Memory Array
WRITE	0000 A010	Write Data to Memory Array

Note: "A" represents MSB address bit A8.

WRITE ENABLE (WREN): The device will power up in the write disable state when V_{CC} is applied. All programming instructions must therefore be preceded by a Write Enable instruction. The $\overline{WP}$ pin must be held high during a WREN instruction.

WRITE DISABLE (WRDI): To protect the device against inadvertent writes, the Write Disable instruction disables all programming modes. The WRDI instruction is independent of the status of the $\overline{WP}$ pin.

READ STATUS REGISTER (RDSR): The Read Status Register instruction provides access to the status register. The READY/BUSY and Write Enable status of the device can be determined by the RDSR instruction. Similarly, the Block Write Protection bits indicate the extent of protection employed. These bits are set by using the WRSR instruction.

Table 2. Status Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	X	X	X	BP1	BP0	WEN	$\overline{RDY}$

Table 3. Read Status Register Bit Definition

Bit	Definition
Bit 0 ($\overline{RDY}$)	Bit 0 = 0 ($\overline{RDY}$) indicates the device is READY. Bit 0 = 1 indicates the write cycle is in progress.
Bit 1 (WEN)	Bit 1 = 0 indicates the device *is not* WRITE ENABLED. Bit 1 = 1 indicates the device is WRITE ENABLED.
Bit 2 (BP0)	See Table 4.
Bit 3 (BP1)	See Table 4.
Bits 4-7 are 0s when device is not in an internal write cycle.	
Bits 0-7 are 1s during an internal write cycle.	

WRITE STATUS REGISTER (WRSR): The WRSR instruction allows the user to select one of four levels of protection. The AT25010/020/040 is divided into four array segments. Top quarter (1/4), Top half (1/2), or all of the memory segments can be protected. Any of the data within any selected segment will therefore be READ only. The block write protection levels and corresponding status register control bits are shown in Table 4.

The two bits, BP1 and BP0 are nonvolatile cells that have the same properties and functions as the regular memory cells (e.g. WREN, t_{WC}, RDSR).

Table 4. Block Write Protect Bits

Level	Status Register Bits		Array Addresses Protected		
	BP1	BP0	AT25010	AT25020	AT25040
0	0	0	None	None	None
1 (1/4)	0	1	60-7F	C0-FF	180-1FF
2 (1/2)	1	0	40-7F	80-FF	100-1FF
3 (All)	1	1	00-7F	00-FF	000-1FF

READ SEQUENCE (READ): Reading the AT25010/020/040 via the SO (Serial Output) pin requires the following sequence. After the $\overline{CS}$ line is pulled low to select a device, the READ op-code (including A8) is transmitted via the SI line followed by the byte address to be read (A7-A0). Upon completion, any data on the SI line will be ignored. The data (D7-D0) at the specified address is then shifted out onto the SO line. If only one byte is to be read, the $\overline{CS}$ line should be driven high after the data comes out. The READ sequence can be continued since the byte address is automatically incremented and data will continue to be shifted out. When the highest address is reached, the address counter will roll over to the lowest address allowing the entire memory to be read in one continuous READ cycle.

WRITE SEQUENCE (WRITE): In order to program the AT25010/020/040, the Write Protect pin ($\overline{WP}$) must be held high and two separate instructions must be executed. First, the device **must be write enabled** via the Write Enable (WREN) Instruction. Then a Write (WRITE) Instruction may be executed. Also, the address of the memory location(s) to be programmed must be outside the protected address field location selected by the Block Write Protection Level. During an internal write cycle, all commands will be ignored except the RDSR instruction.

A Write Instruction requires the following sequence. After the $\overline{CS}$ line is pulled low to select the device, the WRITE op-code (including A8) is transmitted via the SI line followed by the byte address (A7-A0) and the data (D7-D0) to be programmed. Programming will start after the $\overline{CS}$ pin is brought high. (The LOW to High transition of the $\overline{CS}$ pin must occur during the SCK low time immediately after clocking in the D0 (LSB) data bit.

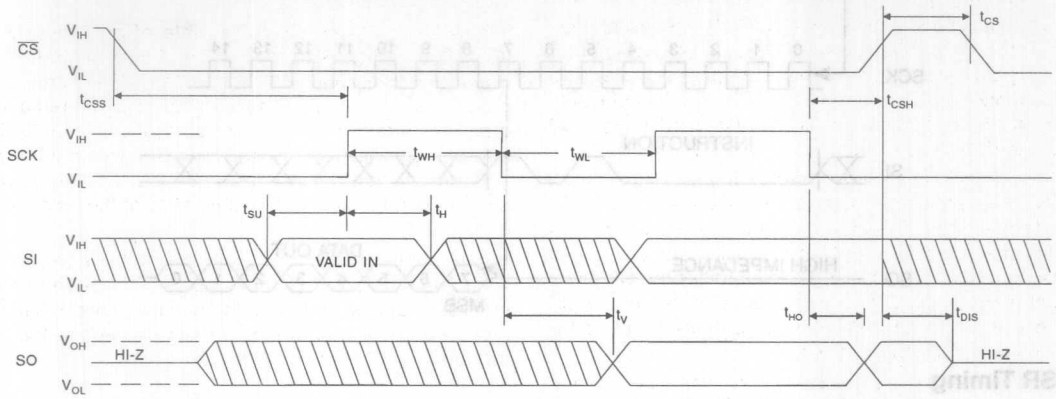
The READY/BUSY status of the device can be determined by initiating a READ STATUS REGISTER (RDSR) Instruction. If Bit 0 = 1, the WRITE cycle is still in progress. If Bit 0 = 0, the WRITE cycle has ended. Only the READ STATUS REGISTER instruction is enabled during the WRITE programming cycle.

The AT25010/020/040 is capable of an 8-byte PAGE WRITE operation. After each byte of data is received, the three low order address bits are internally incremented by one; the six high order bits of the address will remain constant. If more than 8 bytes of data are transmitted, the address counter will roll over and the previously written data will be overwritten. The AT25010/020/040 is automatically returned to the write disable state at the completion of a WRITE cycle.

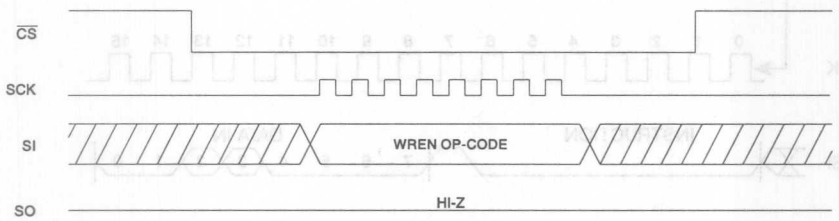
NOTE: If the $\overline{WP}$ pin is brought low or if the device is not Write enabled (WREN), the device will ignore the Write instruction and will return to the standby state, when $\overline{CS}$ is brought high. A new CS falling edge is required to re-initiate the serial communication.

Timing Diagrams

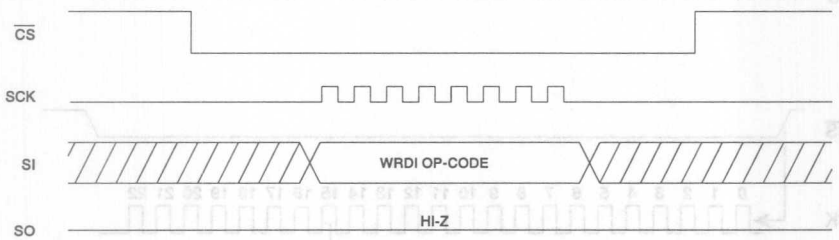
Synchronous Data Timing (for mode 0)



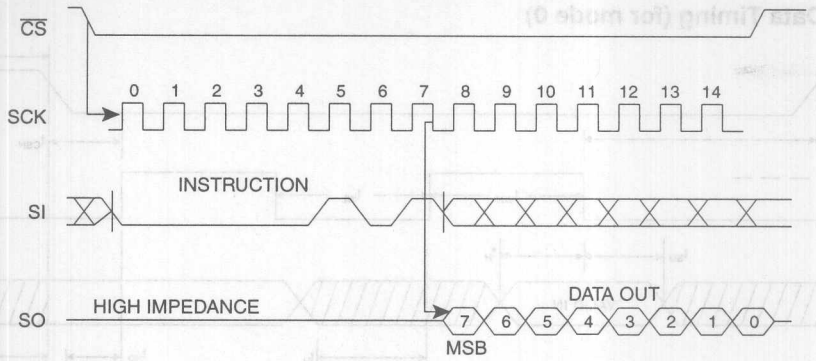
WREN Timing



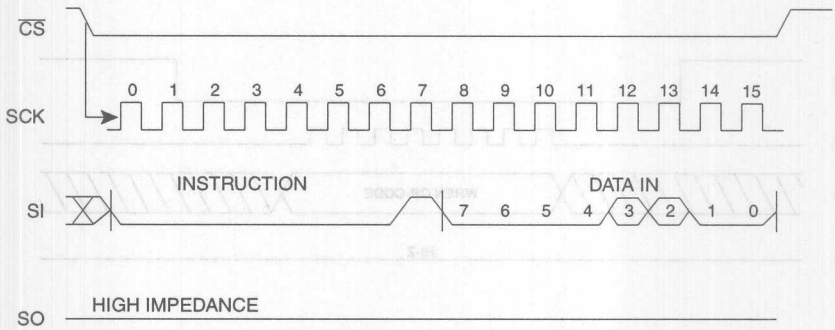
WRDI Timing



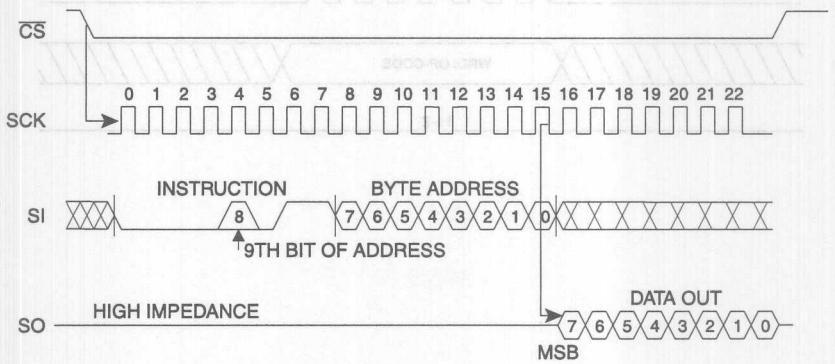
RDSR Timing



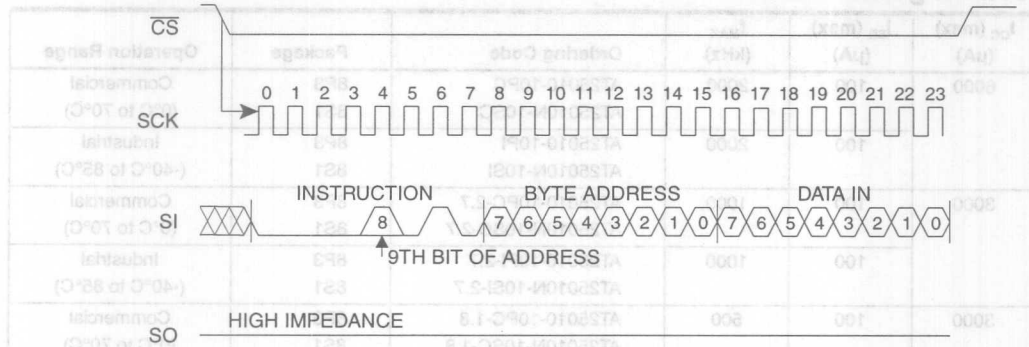
WRSR Timing



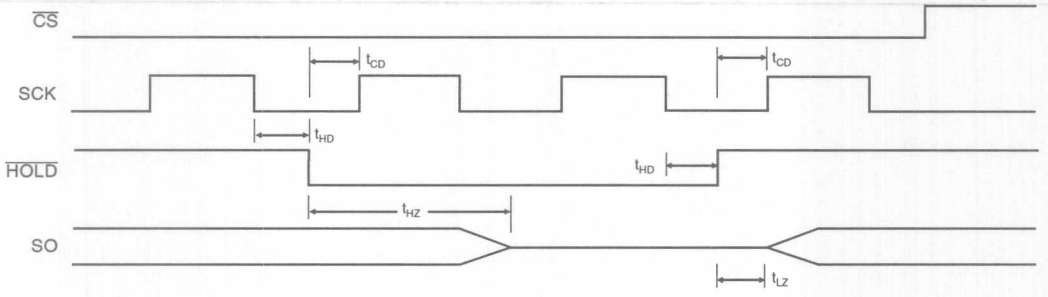
READ Timing



WRITE Timing



HOLD Timing



AT25010 Ordering Information

t_{WP} (max) (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	6000	100	2000	AT25010-10PC AT25010N-10SC	8P3 8S1	Commercial (0°C to 70°C)
		100	2000	AT25010-10PI AT25010N-10SI	8P3 8S1	Industrial (-40°C to 85°C)
10	3000	100	1000	AT25010-10PC-2.7 AT25010N-10SC-2.7	8P3 8S1	Commercial (0°C to 70°C)
		100	1000	AT25010-10PI-2.7 AT25010N-10SI-2.7	8P3 8S1	Industrial (-40°C to 85°C)
10	3000	100	500	AT25010-10PC-1.8 AT25010N-10SC-1.8	8P3 8S1	Commercial (0°C to 70°C)
		100	500	AT25010-10PI-1.8 AT25010N-10SI-1.8	8P3 8S1	Industrial (-40°C to 85°C)

Package Type	
8P3	8-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8-Lead, 0.150" Wide, Plastic Gull Wing Small Outline Package (JEDEC SOIC)
Options	
Blank	Standard Device (4.5V to 5.5V)
-2.7	Low Voltage (2.7V to 5.5V)
-1.8	Low Voltage (1.8V to 5.5V)

AT25020 Ordering Information

t_{WP} (max) (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	6000	100	2100	AT25020-10PC AT25020N-10SC	8P3 8S1	Commercial (0°C to 70°C)
		100	2100	AT25020-10PI AT25020N-10SI	8P3 8S1	Industrial (-40°C to 85°C)
10	3000	100	2100	AT25020-10PC-2.7 AT25020N-10SC-2.7	8P3 8S1	Commercial (0°C to 70°C)
		100	2100	AT25020-10PI-2.7 AT25020N-10SI-2.7	8P3 8S1	Industrial (-40°C to 85°C)
10	3000	100	500	AT25020-10PC-1.8 AT25020N-10SC-1.8	8P3 8S1	Commercial (0°C to 70°C)
		100	500	AT25020-10PI-1.8 AT25020N-10SI-1.8	8P3 8S1	Industrial (-40°C to 85°C)

Package Type	
8P3	8-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8-Lead, 0.150" Wide, Plastic Gull Wing Small Outline Package (JEDEC SOIC)
Options	
Blank	Standard Device (4.5V to 5.5V)
-2.7	Low Voltage (2.7V to 5.5V)
-1.8	Low Voltage (1.8V to 5.5V)

AT25040 Ordering Information

t_{WP} (max) (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	6000	100	2100	AT25040-10PC AT25040N-10SC	8P3 8S1	Commercial (0°C to 70°C)
		100	2100	AT25040-10PI AT25040N-10SI	8P3 8S1	Industrial (-40°C to 85°C)
10	3000	100	2100	AT25040-10PC-2.7 AT25040N-10SC-2.7	8P3 8S1	Commercial (0°C to 70°C)
		100	2100	AT25040-10PI-2.7 AT25040N-10SI-2.7	8P3 8S1	Industrial (-40°C to 85°C)
10	3000	100	500	AT25040-10PC-1.8 AT25040N-10SC-1.8	8P3 8S1	Commercial (0°C to 70°C)
		100	500	AT25040-10PI-1.8 AT25040N-10SI-1.8	8P3 8S1	Industrial (-40°C to 85°C)

Package Type	
8P3	8-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8-Lead, 0.150" Wide, Plastic Gull Wing Small Outline Package (JEDEC SOIC)
Options	
Blank	Standard Device (4.5V to 5.5V)
-2.7	Low Voltage (2.7V to 5.5V)
-1.8	Low Voltage (1.8V to 5.5V)

Features

- Serial Peripheral Interface (SPI) Compatible
- Supports SPI Modes 0 (0,0) and 3 (1,1)
- Low Voltage and Standard Voltage Operation
  - 5.0 (V_{CC} = 4.5V to 5.5V)
  - 2.7 (V_{CC} = 2.7V to 5.5V)
  - 1.8 (V_{CC} = 1.8V to 3.6V)
- 2.1 MHz Clock Rate
- 32-Byte Page Mode
- Block Write Protection
  - Protect 1/4, 1/2, or Entire Array
- Write Protect ($\overline{WP}$) Pin and Write Disable Instructions for Both Hardware and Software Data Protection
- Self-Timed Write Cycle (5 ms Typical)
- High Reliability
  - Endurance: 1 Million Write Cycles
  - Data Retention: 100 Years
  - ESD Protection: >4000V
- Automotive Grade and Extended Temperature Devices Available
- 8-Pin PDIP, JEDEC SOIC, and 14-Pin and 20-Pin TSSOP Packages

Description

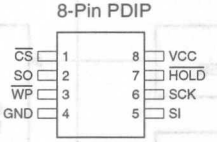
The AT25080/160/320/640 provides 8192/16384/32768/65536 bits of serial electrically erasable programmable read only memory (EEPROM) organized as 1024/2048/4096/8192 words of 8 bits each. The device is optimized for use in many industrial and commercial applications where low power and low voltage operation are

(continued)

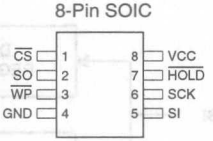
Pin Configuration

Pin Name	Function
$\overline{CS}$	Chip Select
SCK	Serial Data Clock
SI	Serial Data Input
SO	Serial Data Output
GND	Ground
VCC	Power Supply
$\overline{WP}$	Write Protect
$\overline{HOLD}$	Suspends Serial Input
NC	No Connect
DC	Don't Connect

8-Pin PDIP



8-Pin SOIC



14-Lead TSSOP



20-Lead TSSOP*



Note: *Pins 3, 4 and 17, 18 are internally connected

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SPI Serial EEPROMs

8K (1024 x 8)

16K (2048 x 8)

32K (4096 x 8)

64K (8192 x 8)

AT25080
AT25160
AT25320
AT25640

Rev. 0675C–08/98

essential. The AT25080/160/320/640 is available in space saving 8-pin PDIP, JEDEC SOIC, and 14-pin and 20-pin TSSOP packages.

The AT25080/160/320/640 is enabled through the Chip Select pin ($\overline{CS}$) and accessed via a 3-wire interface consisting of Serial Data Input (SI), Serial Data Output (SO), and Serial Clock (SCK). All programming cycles are completely self-timed, and no separate ERASE cycle is required before WRITE.

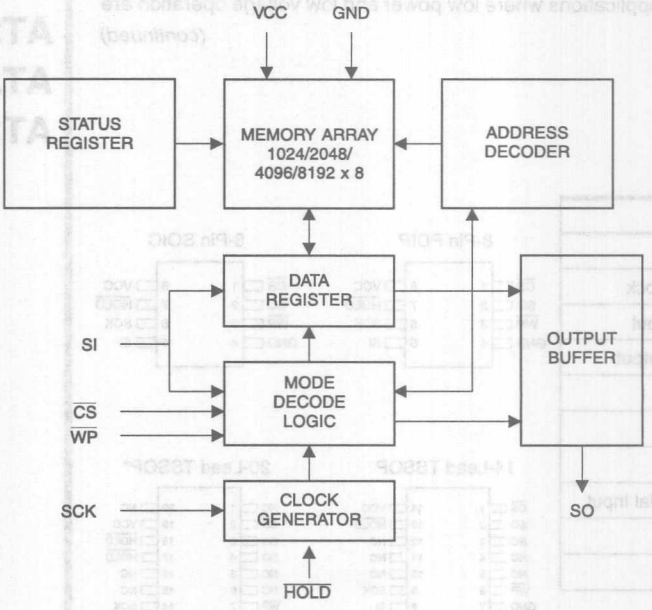
BLOCK WRITE protection is enabled by programming the status register with one of four blocks of write protection. Separate program enable and program disable instructions are provided for additional data protection. Hardware data protection is provided via the $\overline{WP}$ pin to protect against inadvertent write attempts to the status register. The $\overline{HOLD}$ pin may be used to suspend any serial communication without resetting the serial sequence.

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Block Diagram



Pin Capacitance[1]

Applicable over recommended operating range from T_A = 25°C, f = 1.0 MHz, V_{CC} = +5.0V (unless otherwise noted).

Symbol	Test Conditions	Max	Units	Conditions
C_{OUT}	Output Capacitance (SO)	8	pF	V_{OUT} = 0V
C_{IN}	Input Capacitance($\overline{CS}$, SCK, SI, $\overline{WP}$, $\overline{HOLD}$)	6	pF	V_{IN} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

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DC Characteristics

Applicable over recommended operating range from: T_{AI} = -40°C to +85°C, V_{CC} = +1.8V to +5.5V, T_{AC} = 0°C to +70°C, V_{CC} = +1.8V to +5.5V (unless otherwise noted).

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
V_{CC1}	Supply Voltage			1.8		3.6	V
V_{CC2}	Supply Voltage			2.7		5.5	V
V_{CC3}	Supply Voltage			4.5		5.5	V
I_{CC1}	Supply Current	V_{CC} = 5.0V at 1 MHz, SO = Open				3.0	mA
I_{CC2}	Supply Current	V_{CC} = 5.0V at 2 MHz, SO = Open				5.0	mA
I_{SB1}	Standby Current	V_{CC} = 1.8V, $\overline{CS}$ = V_{CC}				0.1	∝A
I_{SB2}	Standby Current	V_{CC} = 2.7V, $\overline{CS}$ = V_{CC}			0.2	0.5	∝A
I_{SB3}	Standby Current	V_{CC} = 5.0V, $\overline{CS}$ = V_{CC}			0.5	2.0	∝A
I_{IL}	Input Leakage	V_{IN} = 0V to V_{CC}		-3.0		3.0	∝A
I_{OL}	Output Leakage	V_{IN} = 0V to V_{CC}, T_{AC} = 0°C to 70°C		-3.0		3.0	∝A
V_{IL}[1]	Input Low Voltage			-0.6		V_{CC} x 0.3	V
V_{IH}[1]	Input High Voltage			V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL1}	Output Low Voltage	4.5V ≤ V_{CC} ≤ 5.5V	I_{OL} = 3.0 mA			0.4	V
V_{OH1}	Output High Voltage		I_{OH} = -1.6 mA	V_{CC} - 0.8			V
V_{OL2}	Output Low Voltage	1.8V ≤ V_{CC} ≤ 3.6V	I_{OL} = 0.15 mA			0.2	V
V_{OH2}	Output High Voltage		I_{OH} = -100 ∝A	V_{CC} - 0.2			V

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

AC Characteristics

Applicable over recommended operating range from T_A = -40°C to +85°C, V_{CC} = As Specified, CL = 1 TTL Gate and 100 pF (unless otherwise noted).

Symbol	Parameter	Voltage	Min	Max	Units
f_{SCK}	SCK Clock Frequency	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6	0 0 0	2.1 2.1 0.5	MHz
t_{RI}	Input Rise Time	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6		2 2 2	µs
t_{FI}	Input Fall Time	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6		2 2 2	µs
t_{WH}	SCK High Time	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6	200 200 800		ns
t_{WL}	SCK Low Time	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6	200 200 800		ns
t_{CS}	$\overline{CS}$ High Time	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6	250 250 1000		ns
t_{CSS}	$\overline{CS}$ Setup Time	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6	250 250 1000		ns
t_{CSH}	$\overline{CS}$ Hold Time	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6	250 250 1000		ns
t_{SU}	Data In Setup Time	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6	50 50 100		ns
t_H	Data In Hold Time	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6	50 50 100		ns
t_{HD}	$\overline{Hold}$ Setup Time	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6	100 100 400		
t_{CD}	$\overline{Hold}$ Hold Time	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6	200 200 400		ns
t_V	Output Valid	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6	0 0 0	200 200 800	ns
t_{HO}	Output Hold Time	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6	0 0 0		ns

AC Characteristics (Continued)

Applicable over recommended operating range from T_A = -40°C to +85°C, V_{CC} = As Specified, CL = 1 TTL Gate and 100 pF (unless otherwise noted).

Symbol	Parameter	Voltage	Min	Max	Units
t_{LZ}	$\overline{\text{Hold}}$ to Output Low Z	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6	0 0 0	100 100 100	ns
t_{HZ}	$\overline{\text{Hold}}$ to Output High Z	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6		100 100 100	ns
t_{DIS}	Output Disable Time	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6		250 250 1000	ns
t_{WC}	Write Cycle Time	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6		5 10 20	ms
Endurance[1]	5.0V, 25°C, Page Mode		1M		Write Cycles

Note: 1. This parameter is characterized and is not 100% tested.

Serial Interface Description

MASTER: The device that generates the serial clock.

SLAVE: Because the Serial Clock pin (SCK) is always an input, the AT25080/160/320/640 always operates as a slave.

TRANSMITTER/RECEIVER: The AT25080/160/320/640 has separate pins designated for data transmission (SO) and reception (SI).

MSB: The Most Significant Bit (MSB) is the first bit transmitted and received.

SERIAL OP-CODE: After the device is selected with $\overline{CS}$ going low, the first byte will be received. This byte contains the op-code that defines the operations to be performed.

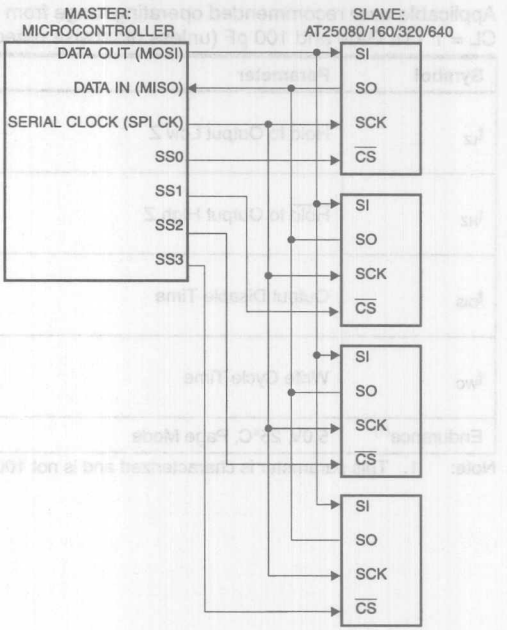
INVALID OP-CODE: If an invalid op-code is received, no data will be shifted into the AT25080/160/320/640, and the serial output pin (SO) will remain in a high impedance state until the falling edge of $\overline{CS}$ is detected again. This will reinitialize the serial communication.

CHIP SELECT: The AT25080/160/320/640 is selected when the $\overline{CS}$ pin is low. When the device is not selected, data will not be accepted via the SI pin, and the serial output pin (SO) will remain in a high impedance state.

HOLD: The $\overline{HOLD}$ pin is used in conjunction with the $\overline{CS}$ pin to select the AT25080/160/320/640. When the device is selected and a serial sequence is underway, $\overline{HOLD}$ can be used to pause the serial communication with the master device without resetting the serial sequence. To pause, the $\overline{HOLD}$ pin must be brought low while the SCK pin is low. To resume serial communication, the $\overline{HOLD}$ pin is brought high while the SCK pin is low (SCK may still toggle during $\overline{HOLD}$). Inputs to the SI pin will be ignored while the SO pin is in the high impedance state.

WRITE PROTECT: The write protect pin ($\overline{WP}$) will allow normal read/write operations when held high. When the WP pin is brought low and WPEN bit is "1", all write operations to the status register are inhibited. $\overline{WP}$ going low while $\overline{CS}$ is still low will interrupt a write to the status register. If the internal write cycle has already been initiated, $\overline{WP}$ going low will have no effect on any write operation to the status register. The $\overline{WP}$ pin function is blocked when the WPEN bit in the status register is "0". This will allow the user to install the AT25080/160/320/640 in a system with the $\overline{WP}$ pin tied to ground and still be able to write to the status register. All $\overline{WP}$ pin functions are enabled when the WPEN bit is set to "1".

SPI Serial Interface



Functional Description

The AT25080/160/320/640 is designed to interface directly with the synchronous serial peripheral interface (SPI) of the 6805 and 68HC11 series of microcontrollers.

The AT25080/160/320/640 utilizes an 8 bit instruction register. The list of instructions and their operation codes are contained in Table 1. All instructions, addresses, and data are transferred with the MSB first and start with a high-to-low CS transition.

Table 1. Instruction Set for the AT25080/160/320/640

Instruction Name	Instruction Format	Operation
WREN	0000 X110	Set Write Enable Latch
WRDI	0000 X100	Reset Write Enable Latch
RDSR	0000 X101	Read Status Register
WRSR	0000 X001	Write Status Register
READ	0000 X011	Read Data from Memory Array
WRITE	0000 X010	Write Data to Memory Array

WRITE ENABLE (WREN): The device will power up in the write disable state when V_{CC} is applied. All programming instructions must therefore be preceded by a Write Enable instruction.

WRITE DISABLE (WRDI): To protect the device against inadvertent writes, the Write Disable instruction disables all programming modes. The WRDI instruction is independent of the status of the $\overline{WP}$ pin.

READ STATUS REGISTER (RDSR): The Read Status Register instruction provides access to the status register. The READY/BUSY and Write Enable status of the device can be determined by the RDSR instruction. Similarly, the Block Write Protection bits indicate the extent of protection employed. These bits are set by using the WRSR instruction.

Table 2. Status Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WPEN	X	X	X	BP1	BP0	WEN	$\overline{RDY}$

Table 3. Read Status Register Bit Definition

Bit	Definition
Bit 0 ($\overline{RDY}$)	Bit 0 = 0 ($\overline{RDY}$) indicates the device is READY. Bit 0 = 1 indicates the write cycle is in progress.
Bit 1 (WEN)	Bit 1= 0 indicates the device is not WRITE ENABLED. Bit 1 = 1 indicates the device is WRITE ENABLED.
Bit 2 (BP0)	See Table 3.
Bit 3 (BP1)	See Table 3.
Bits 4-6 are 0s when device is not in an internal write cycle.	
Bit 7 (WPEN)	See Table 4.
Bits 0-7 are 1s during an internal write cycle.	

WRITE STATUS REGISTER (WRSR): The WRSR instruction allows the user to select one of four levels of protection. The AT25080/160/320/640 is divided into four array segments. One quarter (1/4), one half (1/2), or all of the memory segments can be protected. Any of the data within any selected segment will therefore be READ only. The block write protection levels and corresponding status register control bits are shown in Table 4.

The three bits, BP0, BP1, and WPEN are nonvolatile cells that have the same properties and functions as the regular memory cells (e.g. WREN, t_{WC}, RDSR).

Table 4. Block Write Protect Bits

	Status Register Bits		Array Addresses Protected			
Level	BP1	BP0	AT25080	AT25160	AT25320	AT25640
0	0	0	None	None	None	None
1(1/4)	0	1	0300 -03FF	0600 -07FF	0C00 -0FFF	1800 -1FFF
2(1/2)	1	0	0200 -03FF	0400 -07FF	0800 -0FFF	1000 -1FFF
3(All)	1	1	0000 -03FF	0000 -07FF	0000 -0FFF	0000 -1FFF

The WRSR instruction also allows the user to enable or disable the write protect ($\overline{WP}$) pin through the use of the Write Protect Enable (WPEN) bit. Hardware write protection is enabled when the $\overline{WP}$ pin is low and the WPEN bit is "1". Hardware write protection is disabled when either the $\overline{WP}$ pin is high or the WPEN bit is "0". When the device is hardware write protected, writes to the Status Register, including the Block Protect bits and the WPEN bit, and the block-protected sections in the memory array are disabled.

Writes are only allowed to sections of the memory which are not block-protected.

NOTE: When the WPEN bit is hardware write protected, it cannot be changed back to "0", as long as the $\overline{WP}$ pin is held low.

Table 5. WPEN Operation

WPEN	$\overline{WP}$	WEN	Protected Blocks	Unprotected Blocks	Status Register
0	X	0	Protected	Protected	Protected
0	X	1	Protected	Writable	Writable
1	Low	0	Protected	Protected	Protected
1	Low	1	Protected	Writable	Protected
X	High	0	Protected	Protected	Protected
X	High	1	Protected	Writable	Writable

READ SEQUENCE (READ): Reading the AT25080/160/320/640 via the SO (Serial Output) pin requires the following sequence. After the $\overline{CS}$ line is pulled low to select a device, the READ op-code is transmitted via the SI line followed by the byte address to be read (A15-A0, Refer to Table 6). Upon completion, any data on the SI line will be ignored. The data (D7-D0) at the specified address is then shifted out onto the SO line. If only one byte is to be read, the $\overline{CS}$ line should be driven high after the data comes out. The READ sequence can be continued since the byte address is automatically incremented and data will continue to be shifted out. When the highest address is reached, the address counter will roll over to the lowest address allowing the entire memory to be read in one continuous READ cycle.

WRITE SEQUENCE (WRITE): In order to program the AT25080/160/320/640, two separate instructions must be executed. First, the device **must be write enabled** via the Write Enable (WREN) Instruction. Then a Write (WRITE) Instruction may be executed. Also, the address of the memory location(s) to be programmed must be outside the protected address field location selected by the Block Write Protection Level. During an internal write cycle, all commands will be ignored except the RDSR instruction.

A Write Instruction requires the following sequence. After the $\overline{CS}$ line is pulled low to select the device, the WRITE op-code is transmitted via the SI line followed by the byte address (A15-A0) and the data (D7-D0) to be programmed (Refer to Table 6). Programming will start after the $\overline{CS}$ pin is brought high. (The LOW to High transition of the $\overline{CS}$ pin must occur during the SCK low time immediately after clocking in the D0 (LSB) data bit.

The READY/BUSY status of the device can be determined by initiating a READ STATUS REGISTER (RDSR) Instruction. If Bit 0 = 1, the WRITE cycle is still in progress. If Bit 0 = 0, the WRITE cycle has ended. Only the READ STATUS REGISTER instruction is enabled during the WRITE programming cycle.

The AT25080/160/320/640 is capable of a 32-byte PAGE WRITE operation. After each byte of data is received, the five low order address bits are internally incremented by one; the high order bits of the address will remain constant. If more than 32-bytes of data are transmitted, the address counter will roll over and the previously written data will be overwritten. The AT25080/160/320/640 is automatically returned to the write disable state at the completion of a WRITE cycle.

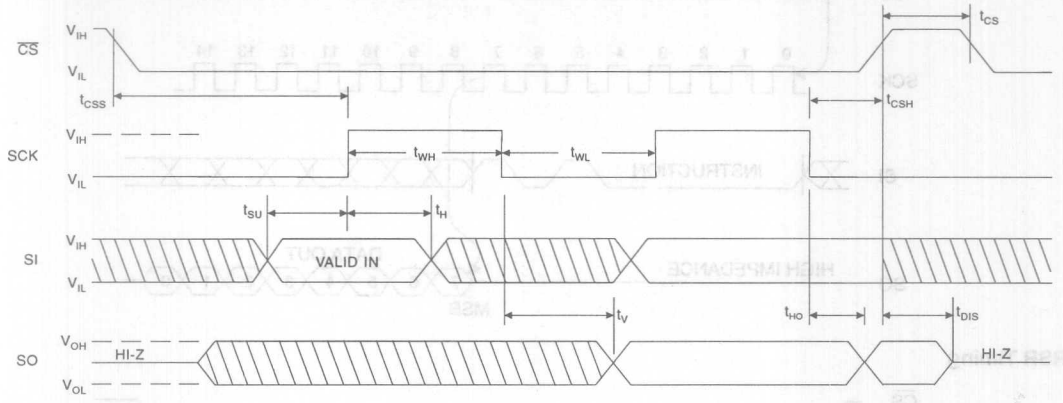
NOTE: If the device is not Write enabled (WREN), the device will ignore the Write instruction and will return to the standby state, when $\overline{CS}$ is brought high. A new $\overline{CS}$ falling edge is required to re-initiate the serial communication.

Table 6. Address Key

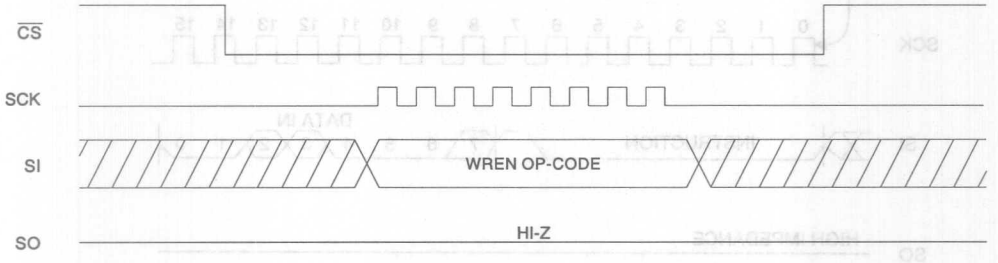
Address	AT25080	AT25160	AT25320	AT25640
A_N	A_9 - A_0	A_{10} - A_0	A_{11} - A_0	A_{12} - A_0
Don't Care Bits	A_{15} - A_{10}	A_{15} - A_{11}	A_{15} - A_{12}	A_{15} - A_{13}

Timing Diagrams

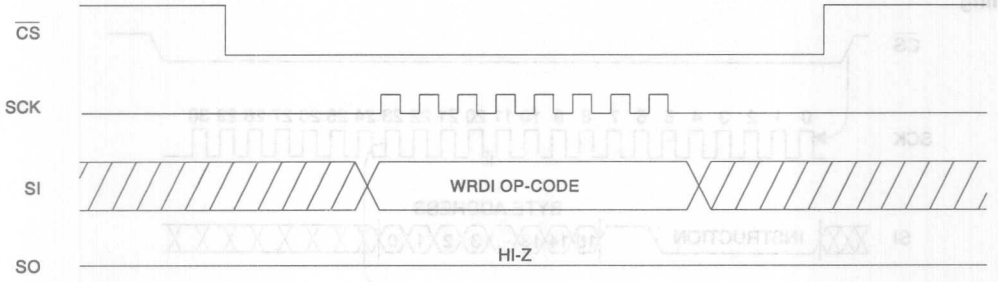
Synchronous Data Timing (for Mode 0)



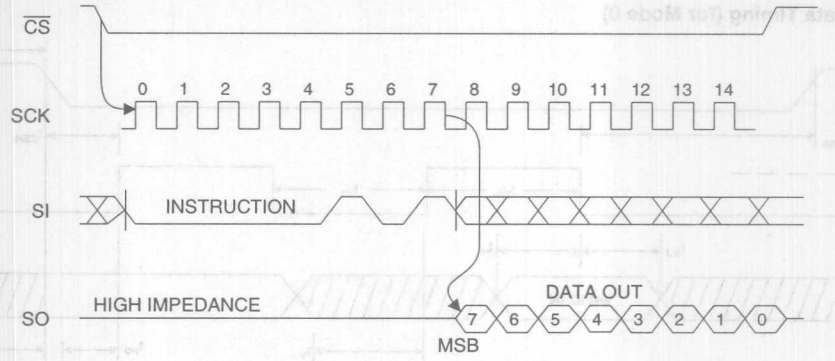
WREN Timing



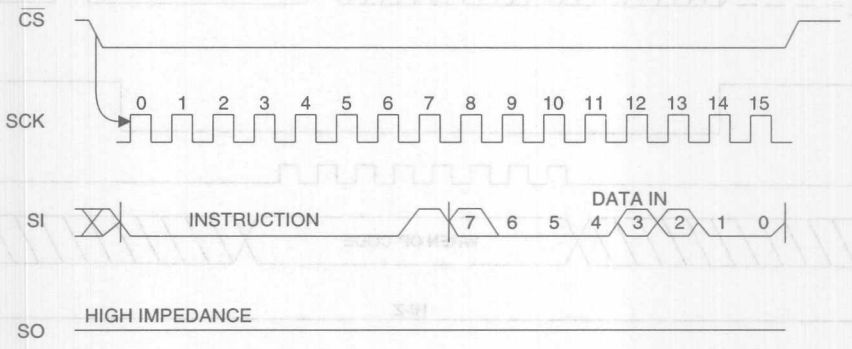
WRDI Timing



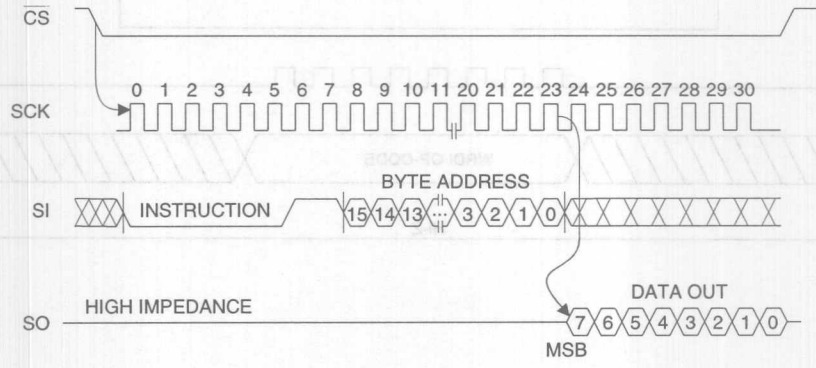
RDST Timing



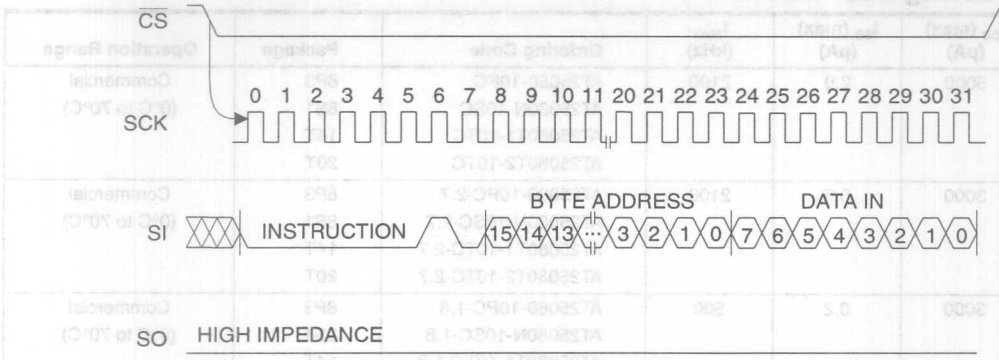
WRSR Timing



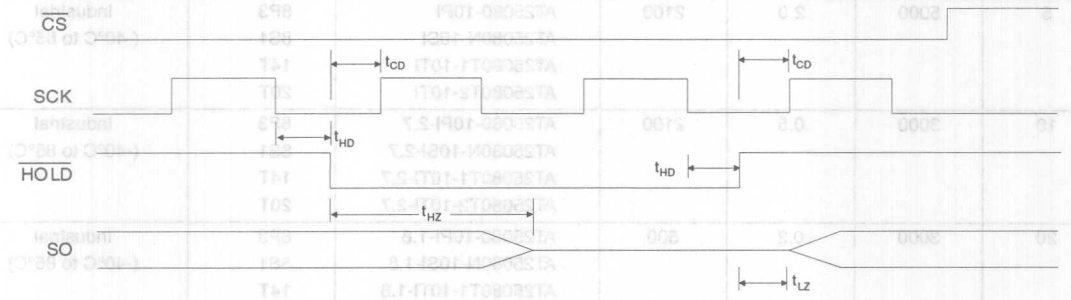
READ Timing



WRITE Timing



$\overline{\text{HOLD}}$ Timing



AT25080 Ordering Information

t_{WC} (max) (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
5	5000	2.0	2100	AT25080-10PC AT25080N-10SC AT25080T1-10TC AT25080T2-10TC	8P3 8S1 14T 20T	Commercial (0°C to 70°C)
10	3000	0.5	2100	AT25080-10PC-2.7 AT25080N-10SC-2.7 AT25080T1-10TC-2.7 AT25080T2-10TC-2.7	8P3 8S1 14T 20T	Commercial (0°C to 70°C)
20	3000	0.2	500	AT25080-10PC-1.8 AT25080N-10SC-1.8 AT25080T1-10TC-1.8 AT25080T2-10TC-1.8	8P3 8S1 14T 20T	Commercial (0°C to 70°C)
5	5000	2.0	2100	AT25080-10PI AT25080N-10SI AT25080T1-10TI AT25080T2-10TI	8P3 8S1 14T 20T	Industrial (-40°C to 85°C)
10	3000	0.5	2100	AT25080-10PI-2.7 AT25080N-10SI-2.7 AT25080T1-10TI-2.7 AT25080T2-10TI-2.7	8P3 8S1 14T 20T	Industrial (-40°C to 85°C)
20	3000	0.2	500	AT25080-10PI-1.8 AT25080N-10SI-1.8 AT25080T1-10TI-1.8 AT25080T2-10TI-1.8	8P3 8S1 14T 20T	Industrial (-40°C to 85°C)

Package Type	
8P3	8-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
14T	14-Lead, 0.170" Wide, Thin Shrink Small Outline Package (TSSOP)
20T	20-Lead, 0.170" Wide, Thin Shrink Small Outline Package (TSSOP)
Options	
Blank	Standard Device (4.5V to 5.5V)
-2.7	Low Voltage (2.7V to 5.5V)

AT25160 Ordering Information

t_{WC} (max) (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
5	5000	2.0	2100	AT25160-10PC	8P3	Commercial
				AT25160N-10SC	8S1	(0°C to 70°C)
				AT25160T1-10TC	14T	
				AT25160T2-10TC	20T	
10	3000	0.5	2100	AT25160-10PC-2.7	8P3	Commercial
				AT25160N-10SC-2.7	8S1	(0°C to 70°C)
				AT25160T1-10TC-2.7	14T	
				AT25160T2-10TC-2.7	20T	
20	3000	0.2	500	AT25160-10PC-1.8	8P3	Commercial
				AT25160N-10SC-1.8	8S1	(0°C to 70°C)
				AT25160T1-10TC-1.8	14T	
				AT25160T2-10TC-1.8	20T	
5	5000	2.0	2100	AT25160-10PI	8P3	Industrial
				AT25160N-10SI	8S1	(-40°C to 85°C)
				AT25160T1-10TI	14T	
				AT25160T2-10TI	20T	
10	3000	0.5	2100	AT25160-10PI-2.7	8P3	Industrial
				AT25160N-10SI-2.7	8S1	(-40°C to 85°C)
				AT25160T1-10TI-2.7	14T	
				AT25160T2-10TI-2.7	20T	
20	3000	0.2	500	AT25160-10PI-1.8	8P3	Industrial
				AT25160N-10SI-1.8	8S1	(-40°C to 85°C)
				AT25160T1-10TI-1.8	14T	
				AT25160T2-10TI-1.8	20T	

Package Type	
8P3	8-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
14T	14-Lead, 0.170" Wide, Thin Shrink Small Outline Package (TSSOP)
20T	20-Lead, 0.170" Wide, Thin Shrink Small Outline Package (TSSOP)
Options	
Blank	Standard Device (4.5V to 5.5V)
-2.7	Low Voltage (2.7V to 5.5V)
-1.8	Low Voltage (1.8V to 3.6V)

AT25320 Ordering Information

t_{WC} (max) (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
5	5000	2.0	2100	AT25320-10PC	8P3	Commercial
				AT25320N-10SC	8S1	(0°C to 70°C)
				AT25320T1-10TC	14T	
				AT25320T2-10TC	20T	
10	3000	0.5	2100	AT25320-10PC-2.7	8P3	Commercial
				AT25320N-10SC-2.7	8S1	(0°C to 70°C)
				AT25320T1-10TC-2.7	14T	
				AT25320T2-10TC-2.7	20T	
20	3000	0.2	500	AT25320-10PC-1.8	8P3	Commercial
				AT25320N-10SC-1.8	8S1	(0°C to 70°C)
				AT25320T1-10TC-1.8	14T	
				AT25320T2-10TC-1.8	20T	
5	5000	2.0	2100	AT25320-10PI	8P3	Industrial
				AT25320N-10SI	8S1	(-40°C to 85°C)
				AT25320T1-10TI	14T	
				AT25320T2-10TI	20T	
10	3000	0.5	2100	AT25320-10PI-2.7	8P3	Industrial
				AT25320N-10SI-2.7	8S	(-40°C to 85°C)
				AT25320T1-10TI-2.7	14T	
				AT25320T2-10TI-2.7	20T	
20	3000	0.2	500	AT25320-10PI-1.8	8P3	Industrial
				AT25320N-10SI-1.8	8S1	(-40°C to 85°C)
				AT25320T1-10TI-1.8	14T	
				AT25320T2-10TI-1.8	20T	

Package Type	
8P3	8-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
14T	14-Lead, 0.170" Wide, Thin Shrink Small Outline Package (TSSOP)
20T	20-Lead, 0.170" Wide, Thin Shrink Small Outline Package (TSSOP)
Options	
Blank	Standard Device (4.5V to 5.5V)
-2.7	Low Voltage (2.7V to 5.5V)
-1.8	Low Voltage (1.8V to 3.6V)

AT25640 Ordering Information

t_{WC} (max) (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
5	5000	2.0	2100	AT25640-10PC AT25640N-10SC AT25640T1-10TC AT25640T2-10TC	8P3 8S1 14T 20T	Commercial (0°C to 70°C)
10	3000	0.5	2100	AT25640-10PC-2.7 AT25640N-10SC-2.7 AT25640T1-10TC-2.7 AT25640T2-10TC-2.7	8P3 8S1 14T 20T	Commercial (0°C to 70°C)
20	3000	0.2	500	AT25640-10PC-1.8 AT25640N-10SC-1.8 AT25640T1-10TC-1.8 AT25640T2-10TC-1.8	8P3 8S1 14T 20T	Commercial (0°C to 70°C)
5	5000	2.0	2100	AT25640-10PI AT25640N-10SI AT25640T1-10TI AT25640T2-10TI	8P3 8S1 14T 20T	Industrial (-40°C to 85°C)
10	3000	0.5	2100	AT25640-10PI-2.7 AT25640N-10SI-2.7 AT25640T1-10TI-2.7 AT25640T2-10TI-2.7	8P3 8S1 14T 20T	Industrial (-40°C to 85°C)
20	3000	0.2	500	AT25640-10PI-1.8 AT25640N-10SI-1.8 AT25640T1-10TI-1.8 AT25640T2-10TI-1.8	8P3 8S1 14T 20T	Industrial (-40°C to 85°C)

Package Type	
8P3	8-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
14T	14-Lead, 0.170" Wide, Thin Shrink Small Outline Package (TSSOP)
20T	20-Lead, 0.170" Wide, Thin Shrink Small Outline Package (TSSOP)
Options	
Blank	Standard Device (4.5V to 5.5V)
-2.7	Low Voltage (2.7V to 5.5V)
-1.8	Low Voltage (1.8V to 3.6V)

t_{WC} (max) (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
5	3000	2.0	2100	AT25640-10PC AT25640N-10SC AT25640T-10TC AT25640Y2-10TC	8P3 8S1 14T 20T	Commercial (0°C to 70°C)
10	3000	0.5	2100	AT25640-10PC-2.7 AT25640N-10SC-2.7 AT25640T-10TC-2.7 AT25640Y2-10TC-2.7	8P3 8S1 14T 20T	Commercial (0°C to 70°C)
20	3000	0.2	500	AT25640-10PC-1.8 AT25640N-10SC-1.8 AT25640T-10TC-1.8 AT25640Y2-10TC-1.8	8P3 8S1 14T 20T	Commercial (0°C to 70°C)
5	3000	2.0	2100	AT25640-10PI AT25640N-10SI AT25640T-10TI AT25640Y2-10TI	8P3 8S1 14T 20T	Industrial (-40°C to 85°C)
10	3000	0.5	2100	AT25640-10PI-2.7 AT25640N-10SI-2.7 AT25640T-10TI-2.7 AT25640Y2-10TI-2.7	8P3 8S1 14T 20T	Industrial (-40°C to 85°C)
20	3000	0.2	500	AT25640-10PI-1.8 AT25640N-10SI-1.8 AT25640T-10TI-1.8 AT25640Y2-10TI-1.8	8P3 8S1 14T 20T	Industrial (-40°C to 85°C)

Package Type	
8P3	8-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
14T	14-Lead, 0.170" Wide, Thin Shrink Small Outline Package (TSSOP)
20T	20-Lead, 0.170" Wide, Thin Shrink Small Outline Package (TSSOP)

Options	
Blank	Standard Device (4.5V to 5.5V)
-2.7	Low Voltage (2.7V to 5.5V)
-1.8	Low Voltage (1.8V to 3.6V)

Features

- Serial Peripheral Interface (SPI) Compatible
- Supports SPI Modes 0 (0,0) and 3 (1,1)
- Low Voltage and Standard Voltage Operation
  - 5.0 (V_{CC} = 4.5V to 5.5V)
  - 2.7 (V_{CC} = 2.7V to 5.5V)
  - 1.8 (V_{CC} = 1.8V to 3.6V)
- 3 MHz Clock Rate
- 64-Byte Page Mode and Byte Write Operation
- Block Write Protection
  - Protect 1/4, 1/2, or Entire Array
- Write Protect ($\overline{WP}$) Pin and Write Disable Instructions for Both Hardware and Software Data Protection
- Self-Timed Write Cycle (5 ms typical)
- High Reliability
  - Endurance: 100,000 Write Cycles
  - Data Retention: >200 Years
  - ESD Protection: >4000V
- Automotive Grade and Extended Temperature Devices Available
- 8-Pin PDIP, 8-Pin EIAJ SOIC, 8-Pin and 16-Pin JEDEC SOIC, 14-Pin and 20-Pin TSSOP, and 8-Pin Leadless Array Packages

Description

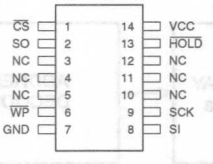
The AT25128/256 provides 131,072/262,144 bits of serial electrically erasable programmable read only memory (EEPROM) organized as 16,384/32,768 words of 8 bits each. The device is optimized for use in many industrial and commercial applications where low power and low voltage operation are essential. The devices are available in

(continued)

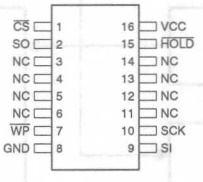
Pin Configurations

Pin Name	Function
$\overline{CS}$	Chip Select
SCK	Serial Data Clock
SI	Serial Data Input
SO	Serial Data Output
GND	Ground
VCC	Power Supply
$\overline{WP}$	Write Protect
$\overline{HOLD}$	Suspends Serial Input
NC	No Connect
DC	Don't Connect

14-Lead TSSOP



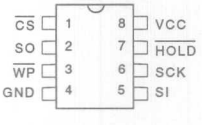
16-Pin SOIC



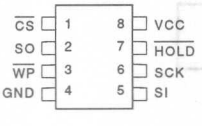
20-Lead TSSOP*



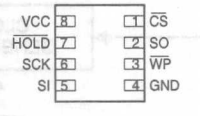
8-Pin PDIP



8-Pin SOIC



8-Pin Leadless Array



Bottom View

*Note: Pins 3, 4 and 17, 18 are internally connected for 14-lead TSSOP socket compatibility.

2

SPI Serial EEPROMs

128K (16,384 x 8)

256K (32,768 x 8)

AT25128
AT25256

Rev. 0872E–08/98

space saving 8-pin PDIP (AT25128/256), 8-pin EIAJ SOIC (AT25128/256), 8-pin and 16-pin JEDEC SOIC (AT25128), 14-pin TSSOP (AT25128), 20-pin TSSOP (AT25128/256), and 8-pin Leadless Array (AT25128/256) packages. In addition, the entire family is available in 5.0V (4.5V to 5.5V), 2.7V (2.7V to 5.5V) and 1.8V (1.8V to 3.6V) versions.

The AT25128/256 is enabled through the Chip Select pin ($\overline{CS}$) and accessed via a 3-wire interface consisting of Serial Data Input (SI), Serial Data Output (SO), and Serial Clock (SCK). All programming cycles are completely self-timed, and no separate ERASE cycle is required before WRITE.

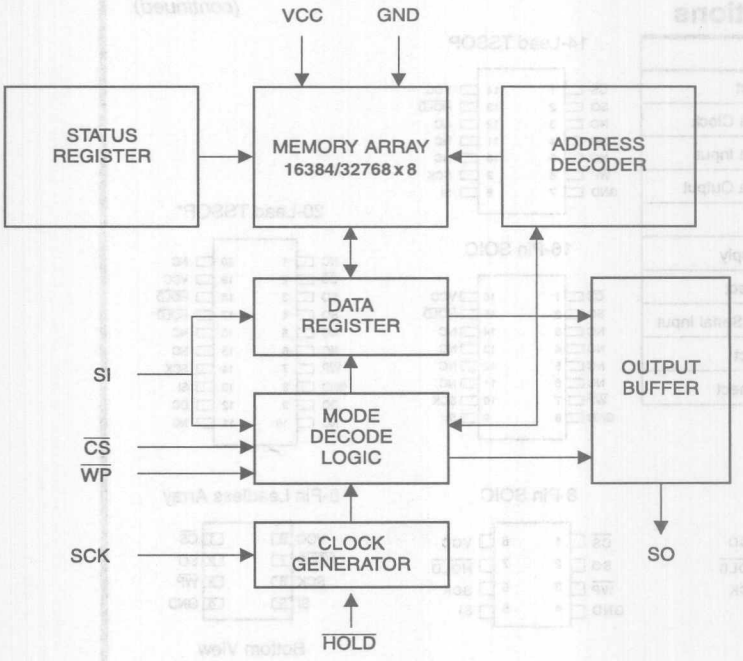
BLOCK WRITE protection is enabled by programming the status register with top ¼, top ½ or entire array of write protection. Separate program enable and program disable instructions are provided for additional data protection. Hardware data protection is provided via the $\overline{WP}$ pin to protect against inadvertent write attempts to the status register. The $\overline{HOLD}$ pin may be used to suspend any serial communication without resetting the serial sequence.

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Block Diagram



Pin Capacitance

Applicable over recommended operating range from T_A = 25°C, f = 1.0 MHz, V_{CC} = +5.0V (unless otherwise noted).

Symbol	Test Conditions	Max	Units	Conditions
C_{OUT}	Output Capacitance (SO)	8	pF	V_{OUT} = 0V
C_{IN}	Input Capacitance ($\overline{CS}$, SCK, SI, $\overline{WP}$, $\overline{HOLD}$)	6	pF	V_{IN} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

2

DC Characteristics

Applicable over recommended operating range from T_{AI} = -40°C to +85°C, V_{CC} = +1.8V to +5.5V, T_{AC} = 0°C to +70°C, V_{CC} = +1.8V to +5.5V(unless otherwise noted).

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
V_{CC1}	Supply Voltage			1.8		3.6	V
V_{CC2}	Supply Voltage			2.7		5.5	V
V_{CC3}	Supply Voltage			4.5		5.5	V
I_{CC1}	Supply Current	V_{CC} = 5.0V at 1 MHz, SO = Open, Read			2.0	3.0	mA
I_{CC2}	Supply Current	V_{CC} = 5.0V at 2 MHz, SO = Open, Read, Write			3.0	5.0	mA
I_{SB1}	Standby Current	V_{CC} = 1.8V, $\overline{CS}$ = V_{CC}			0.1	2.0	µA
I_{SB2}	Standby Current	V_{CC} = 2.7V, $\overline{CS}$ = V_{CC}			0.2	2.0	µA
I_{SB3}	Standby Current	V_{CC} = 5.0V, $\overline{CS}$ = V_{CC}			2.0	5.0	µA
I_{IL}	Input Leakage	V_{IN} = 0V to V_{CC}		-3.0		3.0	µA
I_{OL}	Output Leakage	V_{IN} = 0V to V_{CC}, T_{AC} = 0°C to 70°C		-3.0		3.0	µA
V_{IL} (1)	Input Low Voltage			-1.0		V_{CC} x 0.3	V
V_{IH} (1)	Input High Voltage			V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL1}	Output Low Voltage	4.5 ≤ V_{CC} ≤ 5.5V	I_{OL} = 3.0 mA			0.4	V
V_{OH1}	Output High Voltage		I_{OH} = -1.6 mA	V_{CC} - 0.8			V
V_{OL2}	Output Low Voltage	1.8V ≤ V_{CC} ≤ 3.6V	I_{OL} = 0.15mA			0.2	V
V_{OH2}	Output High Voltage		I_{OH} = -100µA	V_{CC} - 0.2			V

Note: 1. V_{IL} and V_{IH} max are reference only and are not tested.

AC Characteristics

Applicable over recommended operating range from T_A = -40°C to + 85°C, V_{CC} = As Specified, CL = 1 TTL Gate and 100 pF (unless otherwise noted).

Symbol	Parameter	Voltage	Min	Max	Units
f_{SCK}	SCK Clock Frequency	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6	0 0 0	3.0 2.1 0.5	MHz
t_{RI}	Input Rise Time	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6		2 2 2	µs
t_{FI}	Input Fall Time	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6		2 2 2	µs
t_{WH}	SCK High Time	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6	150 200 800		ns
t_{WL}	SCK Low Time	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6	150 200 800		ns
t_{CS}	$\overline{CS}$ High Time	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6	250 250 1000		ns
t_{CSS}	$\overline{CS}$ Setup Time	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6	100 250 1000		ns
t_{CSH}	$\overline{CS}$ Hold Time	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6	150 250 1000		ns
t_{SU}	Data In Setup Time	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6	30 50 100		ns
t_H	Data In Hold Time	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6	50 50 100		ns
t_{HD}	$\overline{Hold}$ Setup Time	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6	100 100 400		ns
t_{CD}	$\overline{Hold}$ Hold Time	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6	200 300 400		ns
t_V	Output Valid	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6	0 0 0	150 200 800	ns
t_{HO}	Output Hold Time	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6	0 0 0		ns

AC Characteristics (Continued)

Applicable over recommended operating range from T_A = -40°C to + 85°C, V_{CC} = As Specified, CL = 1 TTL Gate and 100 pF (unless otherwise noted).

Symbol	Parameter	Voltage	Min	Max	Units
t_{LZ}	$\overline{Hold}$ to Output Low Z	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6	0 0 0	100 200 300	ns
t_{HZ}	$\overline{Hold}$ to Output High Z	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6		100 200 300	ns
t_{DIS}	Output Disable Time	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6		200 250 1000	ns
t_{WC}	Write Cycle Time	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6		5 10 10	ms
Endurance[1]	5.0V, 25°C, Page Mode		100K		Write Cycles

Note: 1. This parameter is characterized and is not 100% tested. Contact Atmel for further information.

Serial Interface Description

MASTER: The device that generates the serial clock.

SLAVE: Because the Serial Clock pin (SCK) is always an input, the AT25128/256 always operates as a slave.

TRANSMITTER/RECEIVER: The AT25128/256 has separate pins designated for data transmission (SO) and reception (SI).

MSB: The Most Significant Bit (MSB) is the first bit transmitted and received.

SERIAL OP-CODE: After the device is selected with $\overline{CS}$ going low, the first byte will be received. This byte contains the op-code that defines the operations to be performed.

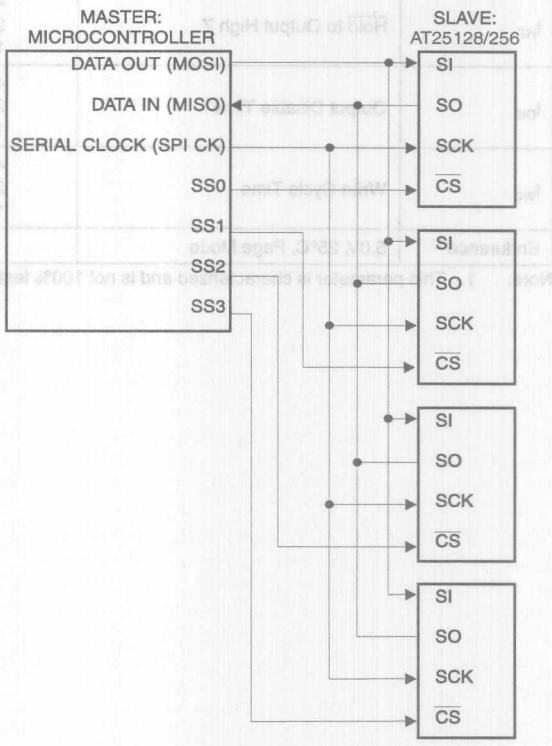
INVALID OP-CODE: If an invalid op-code is received, no data will be shifted into the AT25128/256, and the serial output pin (SO) will remain in a high impedance state until the falling edge of $\overline{CS}$ is detected again. This will reinitialize the serial communication.

CHIP SELECT: The AT25128/256 is selected when the $\overline{CS}$ pin is low. When the device is not selected, data will not be accepted via the SI pin, and the serial output pin (SO) will remain in a high impedance state.

HOLD: The $\overline{HOLD}$ pin is used in conjunction with the $\overline{CS}$ pin to select the AT25128/256. When the device is selected and a serial sequence is underway, $\overline{HOLD}$ can be used to pause the serial communication with the master device without resetting the serial sequence. To pause, the $\overline{HOLD}$ pin must be brought low while the SCK pin is low. To resume serial communication, the $\overline{HOLD}$ pin is brought high while the SCK pin is low (SCK may still toggle during $\overline{HOLD}$). Inputs to the SI pin will be ignored while the SO pin is in the high impedance state.

WRITE PROTECT: The write protect pin ($\overline{WP}$) will allow normal read/write operations when held high. When the $\overline{WP}$ pin is brought low and WPEN bit is "1", all write operations to the status register are inhibited. $\overline{WP}$ going low while $\overline{CS}$ is still low will interrupt a write to the status register. If the internal write cycle has already been initiated, $\overline{WP}$ going low will have no effect on any write operation to the status register. The $\overline{WP}$ pin function is blocked when the WPEN bit in the status register is "0". This will allow the user to install the AT25128/256 in a system with the $\overline{WP}$ pin tied to ground and still be able to write to the status register. All $\overline{WP}$ pin functions are enabled when the WPEN bit is set to "1".

SPI Serial Interface



Functional Description

The AT25128/256 is designed to interface directly with the synchronous serial peripheral interface (SPI) of the 6800 type series of microcontrollers.

The AT25128/256 utilizes an 8-bit instruction register. The list of instructions and their operation codes are contained in Table 1. All instructions, addresses, and data are transferred with the MSB first and start with a high-to-low $\overline{CS}$ transition..

Table 1. Instruction Set for the AT25128/256

Instruction Name	Instruction Format	Operation
WREN	0000 X110	Set Write Enable Latch
WRDI	0000 X100	Reset Write Enable Latch
RDSR	0000 X101	Read Status Register
WRSR	0000 X001	Write Status Register
READ	0000 X011	Read Data from Memory Array
WRITE	0000 X010	Write Data to Memory Array

WRITE ENABLE (WREN): The device will power up in the write disable state when V_{CC} is applied. All programming instructions must therefore be preceded by a Write Enable instruction.

WRITE DISABLE (WRDI): To protect the device against inadvertent writes, the Write Disable instruction disables all programming modes. The WRDI instruction is independent of the status of the $\overline{WP}$ pin.

READ STATUS REGISTER (RDSR): The Read Status Register instruction provides access to the status register. The READY/BUSY and Write Enable status of the device can be determined by the RDSR instruction. Similarly, the Block Write Protection bits indicate the extent of protection employed. These bits are set by using the WRSR instruction.

Table 2. Status Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WPEN	X	X	X	BP1	BP0	WEN	$\overline{RDY}$

Table 3. Read Status Register Bit Definition

Bit	Definition
Bit 0 ($\overline{RDY}$)	Bit 0 = 0 ($\overline{RDY}$) indicates the device is READY. Bit 0 = 1 indicates the write cycle is in progress.
Bit 1 (WEN)	Bit 1 = 0 indicates the device *is not* WRITE ENABLED. Bit 1 = 1 indicates the device is WRITE ENABLED.
Bit 2 (BP0)	See Table 4.
Bit 3 (BP1)	See Table 4.
Bits 4-6 are 0s when device is not in an internal write cycle.	
Bit 7 (WPEN)	See Table 5.
Bits 0-7 are 1s during an internal write cycle.	

WRITE STATUS REGISTER (WRSR): The WRSR instruction allows the user to select one of four levels of protection. The AT25128/256 is divided into four array segments. Top quarter (1/4), top half (1/2), or all of the memory segments can be protected. Any of the data within any selected segment will therefore be READ only. The block write protection levels and corresponding status register control bits are shown in Table 4.

The three bits, BP0, BP1, and WPEN are nonvolatile cells that have the same properties and functions as the regular memory cells (e.g. WREN, t_{WC}, RDSR).

Table 4. Block Write Protect Bits

Level	Status Register Bits		Array Addresses Protected	
	BP1	BP0	AT25128	AT25256
0	0	0	None	None
1(1/4)	0	1	3000 - 3FFF	6000 - 7FFF
2(1/2)	1	0	2000 - 3FFF	4000 - 7FFF
3(All)	1	1	0000 - 3FFF	0000 - 7FFF

The WRSR instruction also allows the user to enable or disable the write protect ($\overline{WP}$) pin through the use of the Write Protect Enable (WPEN) bit. Hardware write protection is enabled when the $\overline{WP}$ pin is low and the WPEN bit is "1". Hardware write protection is disabled when *either* the $\overline{WP}$ pin is high or the WPEN bit is "0." When the device is hardware write protected, writes to the Status Register, including the Block Protect bits and the WPEN bit, and the block-protected sections in the memory array are disabled. Writes are only allowed to sections of the memory which are not block-protected.

NOTE: When the WPEN bit is hardware write protected, it cannot be changed back to "0", as long as the $\overline{WP}$ pin is held low.

Table 5. WPEN Operation

WPEN	WP	WEN	Protected Blocks	Unprotected Blocks	Status Register
0	X	0	Protected	Protected	Protected
0	X	1	Protected	Writable	Writable
1	Low	0	Protected	Protected	Protected
1	Low	1	Protected	Writable	Protected
X	High	0	Protected	Protected	Protected
X	High	1	Protected	Writable	Writable

READ SEQUENCE (READ): Reading the AT25128/256 via the SO (Serial Output) pin requires the following sequence. After the $\overline{CS}$ line is pulled low to select a device, the READ op-code is transmitted via the SI line followed by the byte address to be read (Refer to Table 6). Upon completion, any data on the SI line will be ignored. The data (D7-D0) at the specified address is then shifted out onto the SO line. If only one byte is to be read, the $\overline{CS}$ line should be driven high after the data comes out. The READ sequence can be continued since the byte address is automatically incremented and data will continue to be shifted out. When the highest address is reached, the address counter will roll over to the lowest address allowing the entire memory to be read in one continuous READ cycle.

WRITE SEQUENCE (WRITE): In order to program the AT25128/256, two separate instructions must be executed. First, the device **must be write enabled** via the Write Enable (WREN) Instruction. Then a Write (WRITE) Instruction may be executed. Also, the address of the memory location(s) to be programmed must be outside the protected address field location selected by the Block Write Protection Level. During an internal write cycle, all commands will be ignored except the RDSR instruction.

A Write Instruction requires the following sequence. After the $\overline{CS}$ line is pulled low to select the device, the WRITE op-code is transmitted via the SI line followed by the byte address and the data (D7-D0) to be programmed (Refer to Table 6). Programming will start after the $\overline{CS}$ pin is brought high. (The LOW to High transition of the $\overline{CS}$ pin must occur during the SCK low time immediately after clocking in the D0 (LSB) data bit.

The READY/BUSY status of the device can be determined by initiating a READ STATUS REGISTER (RDSR) Instruction. If Bit 0 = 1, the WRITE cycle is still in progress. If Bit 0 = 0, the WRITE cycle has ended. Only the READ STATUS REGISTER instruction is enabled during the WRITE programming cycle.

The AT25128/256 is capable of a 64-byte PAGE WRITE operation. After each byte of data is received, the five low order address bits are internally incremented by one; the high order bits of the address will remain constant. If more than 64-bytes of data are transmitted, the address counter will roll over and the previously written data will be overwritten. The AT25128/256 is automatically returned to the write disable state at the completion of a WRITE cycle.

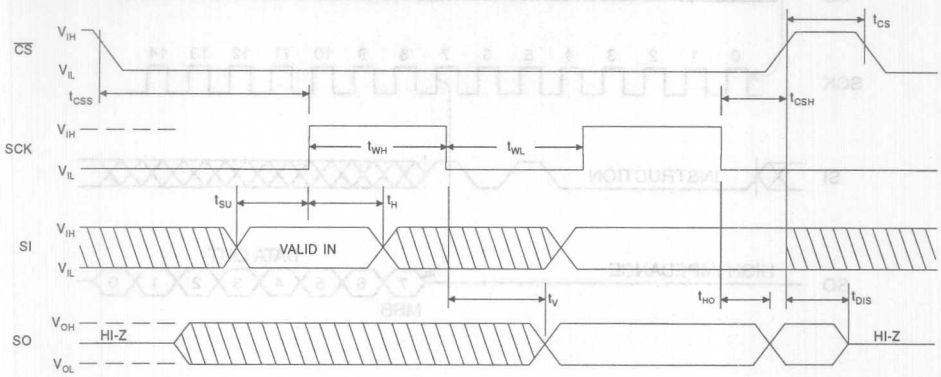
NOTE: If the device is not Write enabled (WREN), the device will ignore the Write instruction and will return to the standby state, when $\overline{CS}$ is brought high. A new CS falling edge is required to re-initiate the serial communication.

Table 6. Address Key

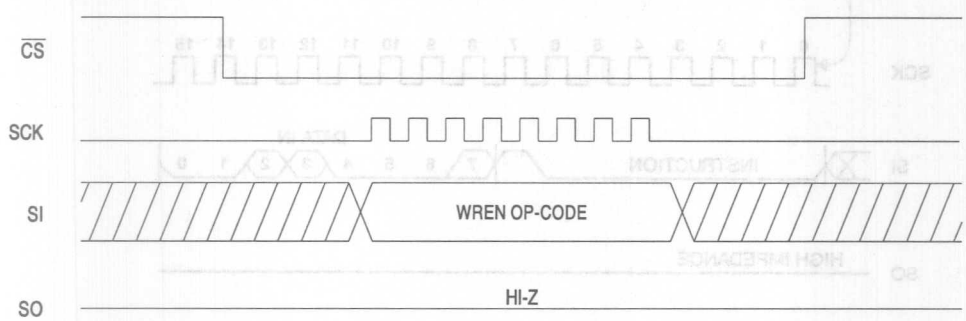
Address	AT25128	AT25256
A_N	$A_{13} - A_0$	$A_{14} - A_0$
Don't Care Bits	$A_{15} - A_{14}$	A_{15}

Timing Diagrams (for SPI Mode 0 (0, 0))

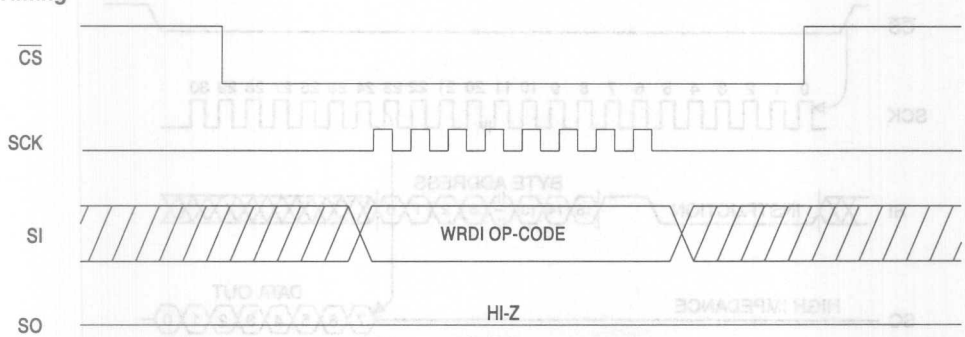
Synchronous Data Timing



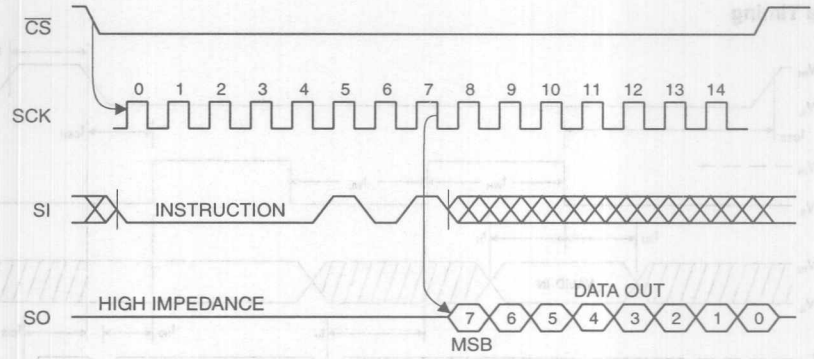
WREN Timing



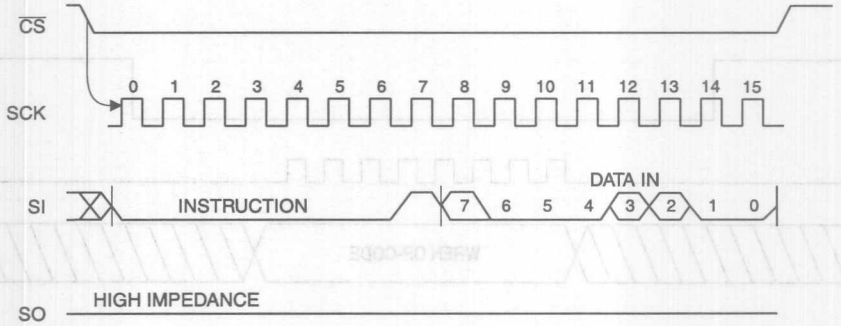
WRDI Timing



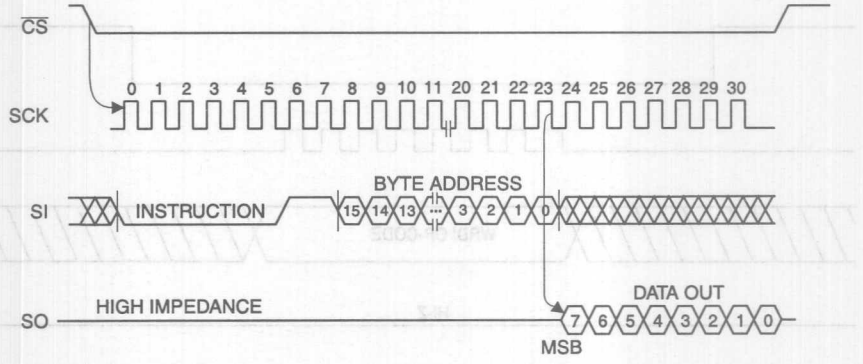
RDSR Timing



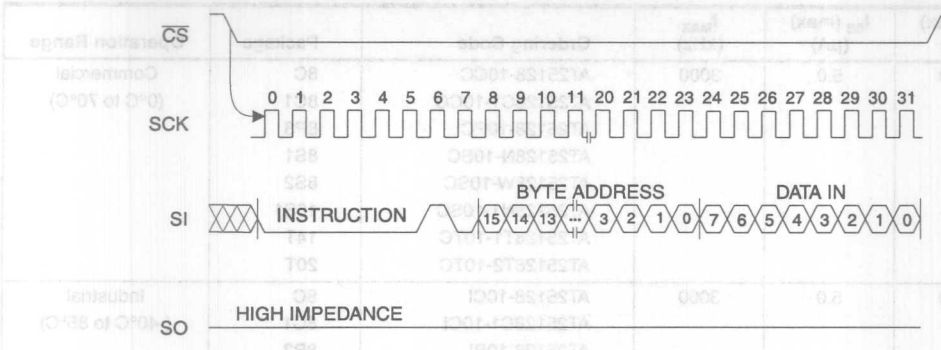
WRSR Timing



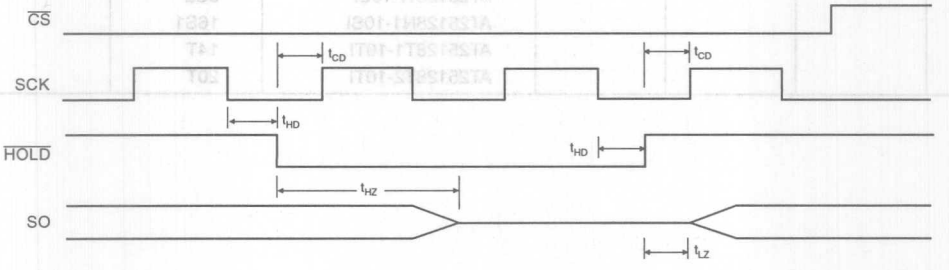
READ Timing



WRITE Timing



HOLD Timing



AT25128 Ordering Information

t_{WC} (max) (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
5	5000	5.0	3000	AT25128-10CC	8C	Commercial (0°C to 70°C)
				AT25128C1-10CC	8C1	
				AT25128-10PC	8P3	
				AT25128N-10SC	8S1	
				AT25128W-10SC	8S2	
				AT25128N1-10SC	16S1	
				AT25128T1-10TC	14T	
				AT25128T2-10TC	20T	
	5000	5.0	3000	AT25128-10CI	8C	Industrial (-40°C to 85°C)
				AT25128C1-10CI	8C1	
				AT25128-10PI	8P3	
				AT25128N-10SI	8S1	
				AT25128W-10SI	8S2	
				AT25128N1-10SI	16S1	
				AT25128T1-10TI	14T	
				AT25128T2-10TI	20T	

Package Type	
8C	8-Lead, 0.230" Wide, Leadless Array Package (LAP)
8C1	8-Lead, 0.300" Wide, Leadless Array Package (LAP)
8P3	8-Lead, 0.300" Wide, Plastic Dual In-line Package (PDIP)
8S1	8-Lead, 0.150" Wide, Plastic Gull Wing Small Outline Package (JEDEC SOIC)
8S2	8-Lead, 0.200" Wide, Plastic Gull Wing Small Outline Package (EIAJ SOIC)
16S1	16-Lead, 0.150" Wide, Plastic Gull Wing Small Outline Package (JEDEC SOIC)
14T	14-Lead, 0.170" Wide, Thin Shrink Small Outline Package (TSSOP)
20T	20-Lead, 0.170" Wide, Thin Shrink Small Outline Package (TSSOP)
Options	
Blank	Standard Device (4.5V to 5.5V)
-2.7	Low Voltage (2.7V to 5.5V)
-1.8	Low Voltage (1.8V to 3.6V)

AT25128 Ordering Information (Continued)

t_{WC} (max) (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	2000	2.0	2100	AT25128-10CC-2.7	8C	Commercial (0°C to 70°C)
				AT25128C1-10CC-2.7	8C1	
				AT25128-10PC-2.7	8P3	
				AT25128N-10SC-2.7	8S1	
				AT25128W-10SC-2.7	8S2	
				AT25128N1-10SC-2.7	16S1	
				AT25128T1-10TC-2.7	14T	
				AT25128T2-10TC-2.7	20T	
	2000	2.0	2100	AT25128-10CI-2.7	8C	Industrial (-40°C to 85°C)
				AT25128C1-10CI-2.7	8C1	
				AT25128-10PI-2.7	8P3	
				AT25128N-10SI-2.7	8S1	
				AT25128W-10SI-2.7	8S2	
				AT25128N1-10SI-2.7	16S1	
				AT25128T1-10TI-2.7	14T	
				AT25128T2-10TI-2.7	20T	

Package Type	
8C	8-Lead, 0.230" Wide, Leadless Array Package (LAP)
8C1	8-Lead, 0.300" Wide, Leadless Array Package (LAP)
8P3	8-Lead, 0.300" Wide, Plastic Dual In-line Package (PDIP)
8S1	8-Lead, 0.150" Wide, Plastic Gull Wing Small Outline Package (JEDEC SOIC)
8S2	8-Lead, 0.200" Wide, Plastic Gull Wing Small Outline Package (EIAJ SOIC)
16S1	16-Lead, 0.150" Wide, Plastic Gull Wing Small Outline Package (JEDEC SOIC)
14T	14-Lead, 0.170" Wide, Thin Shrink Small Outline Package (TSSOP)
20T	20-Lead, 0.170" Wide, Thin Shrink Small Outline Package (TSSOP)
Options	
Blank	Standard Device (4.5V to 5.5V)
-2.7	Low Voltage (2.7V to 5.5V)
-1.8	Low Voltage (1.8V to 3.6V)

AT25128 Ordering Information (Continued)

t_{WC} (max) (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	1000	2.0	500	AT25128-10CC-1.8	8C	Commercial (0°C to 70°C)
				AT25128C1-10CC-1.8	8C1	
				AT25128-10PC-1.8	8P3	
				AT25128N-10SC-1.8	8S1	
				AT25128W-10SC-1.8	8S2	
				AT25128N1-10SC-1.8	16S1	
				AT25128T1-10TC-1.8	14T	
				AT25128T2-10TC-1.8	20T	
	1000	2.0	500	AT25128-10CI-1.8	8C	Industrial (-40°C to 85°C)
				AT25128C1-10CI-1.8	8C1	
				AT25128-10PI-1.8	8P3	
				AT25128N-10SI-1.8	8S1	
				AT25128W-10SI-1.8	8S2	
				AT25128N1-10SI-1.8	16S1	
				AT25128T1-10TI-1.8	14T	
				AT25128T2-10TI-1.8	20T	

Package Type	
8C	8-Lead, 0.230" Wide, Leadless Array Package (LAP)
8C1	8-Lead, 0.300" Wide, Leadless Array Package (LAP)
8P3	8-Lead, 0.300" Wide, Plastic Dual In-line Package (PDIP)
8S1	8-Lead, 0.150" Wide, Plastic Gull Wing Small Outline Package (JEDEC SOIC)
8S2	8-Lead, 0.200" Wide, Plastic Gull Wing Small Outline Package (EIAJ SOIC)
16S1	16-Lead, 0.150" Wide, Plastic Gull Wing Small Outline Package (JEDEC SOIC)
14T	14-Lead, 0.170" Wide, Thin Shrink Small Outline Package (TSSOP)
20T	20-Lead, 0.170" Wide, Thin Shrink Small Outline Package (TSSOP)
Options	
Blank	Standard Device (4.5V to 5.5V)
-2.7	Low Voltage (2.7V to 5.5V)
-1.8	Low Voltage (1.8V to 3.6V)

AT25256 Ordering Information

t_{WC} (max) (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
5	5000	5.0	3000	AT25256-10CC AT25256C1-10CC AT25256-10PC AT25256W-10SC AT25256T2-10TC	8C 8C1 8P3 8S2 20T	Commercial (0°C to 70°C)
	5000	5.0	3000	AT25256-10CI AT25256C1-10CI AT25256-10PI AT25256W-10SI AT25256T2-10TI	8C 8C1 8P3 8S2 20T	Industrial (-40°C to 85°C)
10	2000	2.0	2100	AT25256-10CC-2.7 AT25256C1-10CC-2.7 AT25256-10PC-2.7 AT25256W-10SC-2.7 AT25256T2-10TC-2.7	8C 8C1 8P3 8S2 20T	Commercial (0°C to 70°C)
	2000	2.0	2100	AT25256-10CI-2.7 AT25256C1-10CI-2.7 AT25256-10PI-2.7 AT25256W-10SI-2.7 AT25256T2-10TI-2.7	8C 8C1 8P3 8S2 20T	Industrial (-40°C to 85°C)
10	1000	2.0	500	AT25256-10CC-1.8 AT25256C1-10CC-1.8 AT25256-10PC-1.8 AT25256W-10SC-1.8 AT25256T2-10TC-1.8	8C 8C1 8P3 8S2 20T	Commercial (0°C to 70°C)
	1000	2.0	500	AT25256-10CI-1.8 AT25256C1-10CI-1.8 AT25256-10PI-1.8 AT25256W-10SI-1.8 AT25256T2-10TI-1.8	8C 8C1 8P3 8S2 20T	Industrial (-40°C to 85°C)

Package Type	
8C	8-Lead, 0.230" Wide, Leadless Array Package (LAP)
8C1	8-Lead, 0.300" Wide, Leadless Array Package (LAP)
8P3	8-Lead, 0.300" Wide, Plastic Dual In-line Package (PDIP)
8S2	8-Lead, 0.200" Wide, Plastic Gull Wing Small Outline Package (EIAJ SOIC)
20T	20-Lead, 0.170" Wide, Thin Shrink Small Outline Package (TSSOP)
Options	
Blank	Standard Device (4.5V to 5.5V)
-2.7	Low Voltage (2.7V to 5.5V)
-1.8	Low Voltage (1.8V to 3.6V)

t_{WC} (max) (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
5	3000	5.0	3000	AT25128-10CC	8C	Commercial
				AT25128N-10CC	8C1	(0°C to 70°C)
				AT25128-10PC	8P3	
				AT25128W-10SC	8S2	
				AT25128TS-10TC	20T	
	5000	5.0	3000	AT25128-10CI	8C	Industrial
				AT25128N-10CI	8C1	(-40°C to 85°C)
				AT25128-10PI	8P3	
				AT25128W-10SI	8S2	
				AT25128TS-10TI	20T	
10	2000	2.0	2100	AT25128-10CC-2.7	8C	Commercial
				AT25128N-10CC-2.7	8C1	(0°C to 70°C)
				AT25128-10PC-2.7	8P3	
				AT25128W-10SC-2.7	8S2	
				AT25128TS-10TC-2.7	20T	
	2000	2.0	2100	AT25128-10CI-2.7	8C	Industrial
				AT25128N-10CI-2.7	8C1	(-40°C to 85°C)
				AT25128-10PI-2.7	8P3	
				AT25128W-10SI-2.7	8S2	
				AT25128TS-10TI-2.7	20T	
10	1000	2.0	500	AT25128-10CC-1.8	8C	Commercial
				AT25128N-10CC-1.8	8C1	(0°C to 70°C)
				AT25128-10PC-1.8	8P3	
				AT25128W-10SC-1.8	8S2	
				AT25128TS-10TC-1.8	20T	
	1000	2.0	500	AT25128-10CI-1.8	8C	Industrial
				AT25128N-10CI-1.8	8C1	(-40°C to 85°C)
				AT25128-10PI-1.8	8P3	
				AT25128W-10SI-1.8	8S2	
				AT25128TS-10TI-1.8	20T	

Package Types	
8C	8-Lead, 0.230" Wide, Leadless Array Package (LAP)
8C1	8-Lead, 0.300" Wide, Leadless Array Package (LAP)
8P3	8-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S2	8-Lead, 0.220" Wide, Plastic Gull Wing Small Outline Package (EIAJ SOIC)
20T	20-Lead, 0.170" Wide, Thin Shrink Small Outline Package (TSSOP)

Options	
Blank	Standard Device (4.5V to 5.5V)
-2.7	Low Voltage (2.7V to 5.5V)
-1.8	Low Voltage (1.8V to 5.5V)

Features

- Serial Peripheral Interface (SPI) Compatible
- Supports SPI Modes 0 (0,0) and 3 (1,1)
- 10 MHz Clock Rate
- 128-Byte Page Mode Only for Write Operations
- Low-Voltage and Standard-Voltage Operation
  - 5.0 (V_{CC} = 4.5V to 5.5V)
  - 2.7 (V_{CC} = 2.7V to 5.5V)
  - 1.8 (V_{CC} = 1.8V to 3.6V)
- Block Write Protection
  - Protect 1/4, 1/2, or Entire Array
- Write Protect ($\overline{WP}$) Pin and Write Disable Instructions for Both Hardware and Software Data Protection
- High Reliability
  - Endurance: 100K Write Cycles
  - Data Retention: >40 Years
  - ESD Protection: >3000V
- 8-Pin PDIP, 8-Pin EIAJ SOIC, and 8-Pin Leadless Array Package

Description

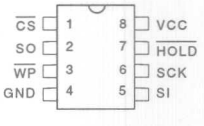
The AT25HP256/512 provides 262,144/524,288 bits of serial electrically erasable programmable read only memory (EEPROM) organized as 32,768/65,536 words of 8-bits each. The device is optimized for use in many industrial and commercial applications where high-speed, low-power, and low-voltage operation are essential. The AT25HP256/512 is available in a space saving 8-pin PDIP (AT25HP256/512), 8-pin EIAJ SOIC (AT25HP256), and 8-pin Leadless Array (AT25HP256/512) packages. In

(continued)

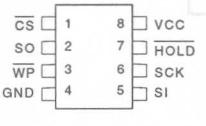
Pin Configurations

Pin Name	Function
$\overline{CS}$	Chip Select
SCK	Serial Data Clock
SI	Serial Data Input
SO	Serial Data Output
GND	Ground
VCC	Power Supply
$\overline{WP}$	Write Protect
$\overline{HOLD}$	Suspends Serial Input

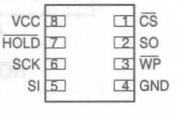
8-Pin PDIP



8-Pin SOIC



8-Pin Leadless Array



Bottom View

2

SPI Serial EEPROMs

256K (32,768 x 8)

512K (65,536 x 8)

AT25HP256
AT25HP512
Preliminary

Rev. 1113B–07/98

Note: Please contact Atmel Corporation for more information on this product.

addition, the entire family is available in 5.0V (4.5V to 5.5V), 2.7V (2.7V to 5.5V), and 1.8V (1.8V to 3.6V) versions.

The AT25HP256/512 is enabled through the Chip Select pin ($\overline{CS}$) and accessed via a 3-wire interface consisting of Serial Data Input (SI), Serial Data Output (SO), and Serial Clock (SCK). All programming cycles are completely self-timed, and no separate ERASE cycle is required before WRITE.

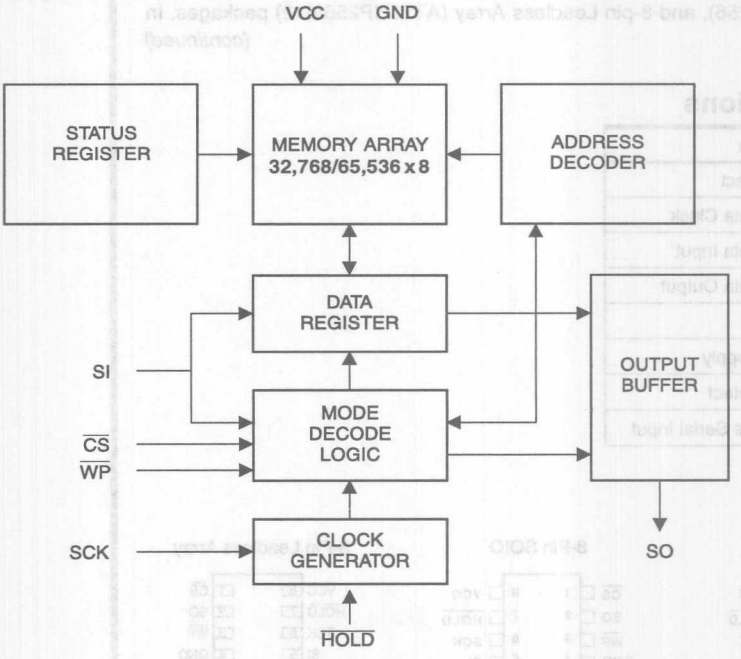
BLOCK WRITE protection is enabled by programming the status register with top ¼, top ½ or entire array of write protection. Separate program enable and program disable instructions are provided for additional data protection. Hardware data protection is provided via the $\overline{WP}$ pin to protect against inadvertent write attempts to the status register. The $\overline{HOLD}$ pin may be used to suspend any serial communication without resetting the serial sequence.

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Block Diagram



Features

- Serial Peripheral Interface (SPI) Compatible
- Supports SPI Modes 0 (0,0) and 3 (1,1)
- 2.1 MHz Clock Rate
- 128-Byte Page Mode Only for Write Operations
- Low Voltage and Standard Voltage Operation
  - 5.0 (V_{CC} = 4.5V to 5.5V)
  - 2.7 (V_{CC} = 2.7V to 5.5V)
  - 1.8 (V_{CC} = 1.8V to 3.6V)
- Block Write Protection
  - Protect 1/4, 1/2, or Entire Array
- Write Protect ($\overline{WP}$) Pin and Write Disable Instructions for Both Hardware and Software Data Protection
- Self-Timed Write Cycle (5 ms Typical)
- High Reliability
  - Endurance: 100,000 Write Cycles
  - Data Retention: >40 Years
  - ESD Protection: >3000V
- 20-Pin JEDEC SOIC and 8-Pin Leadless Array Package

Description

The AT25P1024 provides 1,048,576 bits of serial electrically erasable programmable read only memory (EEPROM) organized as 131,072 words of 8 bits each. The device is optimized for use in many industrial and commercial applications where low power and low voltage operation are essential. The AT25P1024 is available in space saving 20-pin JEDEC SOIC and 8-pin leadless array (LAP) packages.

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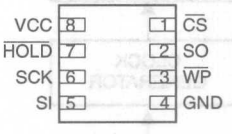
Pin Configurations

Pin Name	Function
$\overline{CS}$	Chip Select
SCK	Serial Data Clock
SI	Serial Data Input
SO	Serial Data Output
GND	Ground
VCC	Power Supply
$\overline{WP}$	Write Protect
$\overline{HOLD}$	Suspends Serial Input
NC	No Connect

20-Lead SOIC



8-Pin LAP



Bottom View

SPI Serial EEPROMs

1M (131,072 x 8)

AT25P1024 Preliminary

Rev. 1082C–08/98

The AT25P1024 is enabled through the Chip Select pin ($\overline{CS}$) and accessed via a 3-wire interface consisting of Serial Data Input (SI), Serial Data Output (SO), and Serial Clock (SCK). All programming cycles are completely self-timed, and no separate ERASE cycle is required before WRITE.

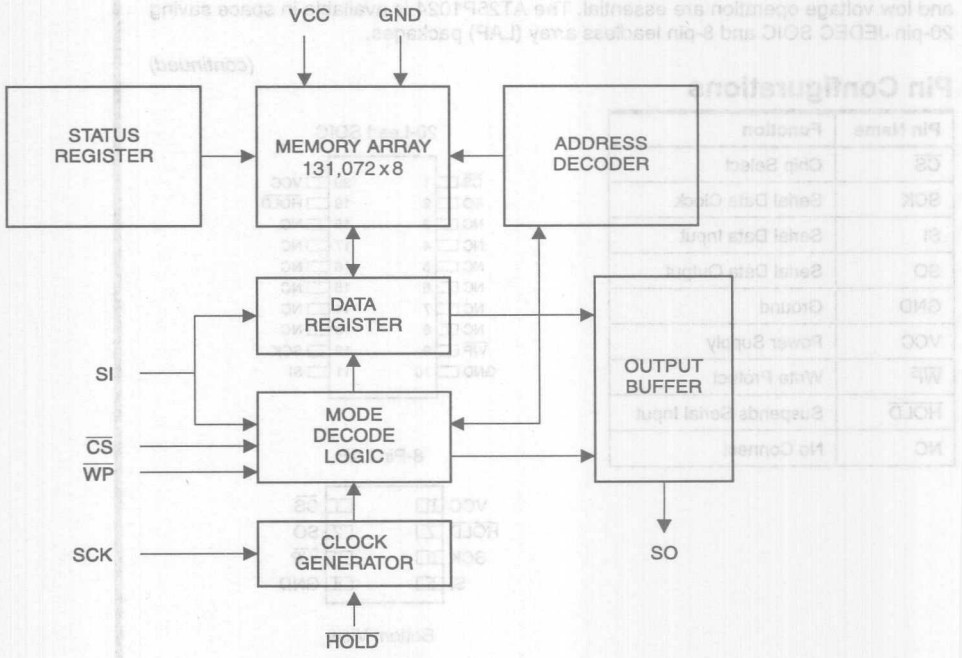
BLOCK WRITE protection is enabled by programming the status register with top ¼, top ½ or entire array of write protection. Separate program enable and program disable instructions are provided for additional data protection. Hardware data protection is provided via the $\overline{WP}$ pin to protect against inadvertent write attempts to the status register. The $\overline{HOLD}$ pin may be used to suspend any serial communication without resetting the serial sequence.

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Block Diagram



Pin Capacitance[1]

Applicable over recommended operating range from T_A = 25°C, f = 1.0 MHz, V_{CC} = +5.0V (unless otherwise noted).

Symbol	Test Conditions	Max	Units	Conditions
C_{OUT}	Output Capacitance (SO)	8	pF	V_{OUT} = 0V
C_{IN}	Input Capacitance ($\overline{CS}$, SCK, SI, $\overline{WP}$, $\overline{HOLD}$)	6	pF	V_{IN} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

2

DC Characteristics

Applicable over recommended operating range from: T_{AI} = -40°C to +85°C, V_{CC} = +1.8V to +5.5V, T_{AC} = 0°C to +70°C, V_{CC} = +1.8V to +5.5V (unless otherwise noted).

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
V_{CC1}	Supply Voltage			1.8		3.6	V
V_{CC2}	Supply Voltage			2.7		5.5	V
V_{CC3}	Supply Voltage			4.5		5.5	V
I_{CC1}	Supply Current	V_{CC} = 5.0V at 1 MHz, SO = Open Read			2.0	5.0	mA
I_{CC2}	Supply Current	V_{CC} = 5.0V at 2 MHz, SO = Open Write			4.0	7.0	mA
I_{SB1}	Standby Current	V_{CC} = 1.8V, $\overline{CS}$ = V_{CC}			0.1	3.0	µA
I_{SB2}	Standby Current	V_{CC} = 2.7V, $\overline{CS}$ = V_{CC}			0.2	3.0	µA
I_{SB3}	Standby Current	V_{CC} = 5.0V, $\overline{CS}$ = V_{CC}			2.0	7.0	µA
I_{IL}	Input Leakage	V_{IN} = 0V to V_{CC}		-3.0		3.0	µA
I_{OL}	Output Leakage	V_{IN} = 0V to V_{CC}, T_{AC} = 0°C to 70°C		-3.0		3.0	µA
V_{IL}[1]	Input Low Voltage			-0.6		V_{CC} x 0.3	V
V_{IH}[1]	Input High Voltage			V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL1}	Output Low Voltage	4.5V ≤ V_{CC} ≤ 5.5V	I_{OL} = 3.0 mA			0.4	V
V_{OH1}	Output High Voltage		I_{OH} = -1.6 mA	V_{CC} - 0.8			V
V_{OL2}	Output Low Voltage	1.8V ≤ V_{CC} ≤ 3.6V	I_{OL} = 0.15 mA			0.2	V
V_{OH2}	Output High Voltage		I_{OH} = -100 µA	V_{CC} - 0.2			V

Note: 1. V_{IL} and V_{IH} max are reference only and are not tested.

AC Characteristics

Applicable over recommended operating range from T_A = -40°C to +85°C, V_{CC} = As Specified, C_L = 1 TTL Gate and 100 pF (unless otherwise noted).

Symbol	Parameter	Voltage	Min	Max	Units
f_{SCK}	SCK Clock Frequency	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6	0 0 0	2.1 1.0 0.5	MHz
t_{RI}	Input Rise Time	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6		2 2 2	µs
t_{FI}	Input Fall Time	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6		2 2 2	µs
t_{WH}	SCK High Time	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6	200 400 800		ns
t_{WL}	SCK Low Time	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6	200 400 800		ns
t_{CS}	$\overline{CS}$ High Time	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6	250 500 1000		ns
t_{CSS}	$\overline{CS}$ Setup Time	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6	100 250 1000		ns
t_{CSH}	$\overline{CS}$ Hold Time	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6	150 250 1000		ns
t_{SU}	Data In Setup Time	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6	30 50 100		ns
t_H	Data In Hold Time	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6	50 50 100		ns
t_{HD}	$\overline{Hold}$ Setup Time	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6	100 100 400		ns
t_{CD}	$\overline{Hold}$ Hold Time	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6	200 300 400		ns
t_V	Output Valid	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6	0 0 0	200 400 800	ns
t_{HO}	Output Hold Time	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6	0 0 0		ns

AC Characteristics (Continued)

Applicable over recommended operating range from T_A = -40°C to +85°C, V_{CC} = As Specified, C_L = 1 TTL Gate and 100 pF (unless otherwise noted).

Symbol	Parameter	Voltage	Min	Max	Units
t_{LZ}	$\overline{Hold}$ to Output Low Z	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6	0 0 0	100 200 300	ns
t_{HZ}	$\overline{Hold}$ to Output High Z	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6		100 200 300	ns
t_{DIS}	Output Disable Time	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6		200 250 1000	ns
t_{WC}	Write Cycle Time	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6		5 10 10	ms
Endurance[1]	5.0V, 25°C, Page Mode	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6	100K		Write Cycles

Note: 1. This parameter is characterized and is not 100% tested.

Serial Interface Description

MASTER: The device that generates the serial clock.

SLAVE: Because the Serial Clock pin (SCK) is always an input, the AT25P1024 always operates as a slave.

TRANSMITTER/RECEIVER: The AT25P1024 has separate pins designated for data transmission (SO) and reception (SI).

MSB: The Most Significant Bit (MSB) is the first bit transmitted and received.

SERIAL OP-CODE: After the device is selected with $\overline{CS}$ going low, the first byte will be received. This byte contains the op-code that defines the operations to be performed.

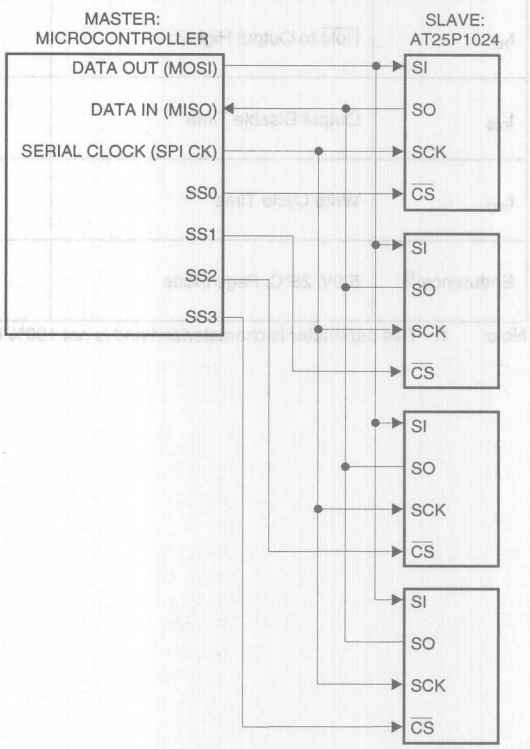
INVALID OP-CODE: If an invalid op-code is received, no data will be shifted into the AT25P1024, and the serial output pin (SO) will remain in a high impedance state until the falling edge of $\overline{CS}$ is detected again. This will reinitialize the serial communication.

CHIP SELECT: The AT25P1024 is selected when the $\overline{CS}$ pin is low. When the device is not selected, data will not be accepted via the SI pin, and the serial output pin (SO) will remain in a high impedance state.

HOLD: The $\overline{HOLD}$ pin is used in conjunction with the $\overline{CS}$ pin to select the AT25P1024. When the device is selected and a serial sequence is underway, $\overline{HOLD}$ can be used to pause the serial communication with the master device without resetting the serial sequence. To pause, the $\overline{HOLD}$ pin must be brought low while the SCK pin is low. To resume serial communication, the $\overline{HOLD}$ pin is brought high while the SCK pin is low (SCK may still toggle during $\overline{HOLD}$). Inputs to the SI pin will be ignored while the SO pin is in the high impedance state.

WRITE PROTECT: The write protect pin ($\overline{WP}$) will allow normal read/write operations when held high. When the $\overline{WP}$ pin is brought low and WPEN bit is "1", all write operations to the status register are inhibited. $\overline{WP}$ going low while $\overline{CS}$ is still low will interrupt a write to the status register. If the internal write cycle has already been initiated, $\overline{WP}$ going low will have no effect on any write operation to the status register. The $\overline{WP}$ pin function is blocked when the WPEN bit in the status register is "0". This will allow the user to install the AT25P1024 in a system with the $\overline{WP}$ pin tied to ground and still be able to write to the status register. All $\overline{WP}$ pin functions are enabled when the WPEN bit is set to "1".

SPI Serial Interface



Functional Description

The AT25P1024 is designed to interface directly with the synchronous serial peripheral interface (SPI) of the 6800 type series of microcontrollers.

The AT25P1024 utilizes an 8-bit instruction register. The list of instructions and their operation codes are contained in Table 1. All instructions, addresses, and data are transferred with the MSB first and start with a high-to-low transition.

Table 1. Instruction Set for the AT25P1024

Instruction Name	Instruction Format	Operation
WREN	0000 X110	Set Write Enable Latch
WRDI	0000 X100	Reset Write Enable Latch
RDSR	0000 X101	Read Status Register
WRSR	0000 X001	Write Status Register
READ	0000 X011	Read Data from Memory Array
WRITE	0000 X010	Write Data to Memory Array

WRITE ENABLE (WREN): The device will power up in the write disable state when V_{CC} is applied. All programming instructions must therefore be preceded by a Write Enable instruction.

WRITE DISABLE (WRDI): To protect the device against inadvertent writes, the Write Disable instruction disables all programming modes. The WRDI instruction is independent of the status of the $\overline{WP}$ pin.

READ STATUS REGISTER (RDSR): The Read Status Register instruction provides access to the status register. The READY/BUSY and Write Enable status of the device can be determined by the RDSR instruction. Similarly, the Block Write Protection bits indicate the extent of protection employed. These bits are set by using the WRSR instruction.

Table 2. Status Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WPEN	X	X	X	BP1	BP0	WEN	$\overline{RDY}$

Table 3. Read Status Register Bit Definition

Bit	Definition
Bit 0 ($\overline{RDY}$)	Bit 0 = 0 ($\overline{RDY}$) indicates the device is READY. Bit 0 = 1 indicates the write cycle is in progress.
Bit 1 (WEN)	Bit 1 = 0 indicates the device *is not* WRITE ENABLED. Bit 1 = 1 indicates the device is WRITE ENABLED.
Bit 2 (BP0)	See Table 4.
Bit 3 (BP1)	See Table 4.
Bits 4-6 are 0s when device is not in an internal write cycle.	
Bit 7 (WPEN)	See Table 5.
Bits 0-7 are 1s during an internal write cycle.	

WRITE STATUS REGISTER (WRSR): The WRSR instruction allows the user to select one of four levels of protection. The AT25P1024 is divided into four array segments. Top quarter (1/4), top half (1/2), or all of the memory segments can be protected. Any of the data within any selected segment will therefore be READ only. The block write protection levels and corresponding status register control bits are shown in Table 4.

The three bits, BP0, BP1, and WPEN are nonvolatile cells that have the same properties and functions as the regular memory cells (e.g. WREN, t_{WC}, RDSR).

Table 4. Block Write Protect Bits

Level	Status Register Bits		Array Addresses Protected
	BP1	BP0	AT25P1024
0	0	0	None
1(1/4)	0	1	01800 - 01FFFF
2(1/2)	1	0	010000 - 01FFFF
3(All)	1	1	0000 - 01FFFF

The WRSR instruction also allows the user to enable or disable the write protect ($\overline{WP}$) pin through the use of the Write Protect Enable (WPEN) bit. Hardware write protection is enabled when the $\overline{WP}$ pin is low and the WPEN bit is "1". Hardware write protection is disabled when *either* the $\overline{WP}$ pin is high or the WPEN bit is "0." When the device is hardware write protected, writes to the Status Register, including the Block Protect bits and the WPEN bit, and the block-protected sections in the memory array are disabled. Writes are only allowed to sections of the memory which are not block-protected.

NOTE: When the WPEN bit is hardware write protected, it cannot be changed back to "0", as long as the $\overline{WP}$ pin is held low.

Table 5. WPEN Operation

WPEN	WP	WEN	Protected Blocks	Unprotected Blocks	Status Register
0	X	0	Protected	Protected	Protected
0	X	1	Protected	Writable	Writable
1	Low	0	Protected	Protected	Protected
1	Low	1	Protected	Writable	Protected
X	High	0	Protected	Protected	Protected
X	High	1	Protected	Writable	Writable

READ SEQUENCE (READ): Reading the AT25P1024 via the SO (Serial Output) pin requires the following sequence. After the $\overline{CS}$ line is pulled low to select a device, the READ op-code is transmitted via the SI line followed by the byte address to be read (Refer to Table 6). Upon completion, any data on the SI line will be ignored. The data (D7-D0) at the specified address is then shifted out onto the SO line. If only one byte is to be read, the $\overline{CS}$ line should be driven high after the data comes out. The READ sequence can be continued since the byte address is automatically incremented and data will continue to be shifted out. When the highest address is reached, the address counter will roll over to the lowest address allowing the entire memory to be read in one continuous READ cycle.

WRITE SEQUENCE (WRITE): In order to program the AT25P1024, two separate instructions must be executed. First, the device **must be write enabled** via the Write Enable (WREN) Instruction. Then a Write (WRITE) Instruction may be executed. Also, the address of the memory location(s) to be programmed must be outside the protected address field location selected by the Block Write Protection Level. During an internal write cycle, all commands will be ignored except the RDSR instruction.

A Write Instruction requires the following sequence. After the $\overline{CS}$ line is pulled low to select the device, the WRITE op-code is transmitted via the SI line followed by the byte address and the data (D7-D0) to be programmed (Refer to Table 6). Programming will start after the $\overline{CS}$ pin is brought high. (The LOW to High transition of the $\overline{CS}$ pin must occur during the SCK low time immediately after clocking in the D0 (LSB) data bit.

The READY/BUSY status of the device can be determined by initiating a READ STATUS REGISTER (RDSR) Instruction. If Bit 0 = 1, the WRITE cycle is still in progress. If Bit 0 = 0, the WRITE cycle has ended. Only the READ STATUS REGISTER instruction is enabled during the WRITE programming cycle.

The AT25P1024 is capable of a 128-byte PAGE WRITE operation ONLY. Content of the page in the array will not be guaranteed if less than 128 bytes of data is received (byte operation is not supported). After each byte of data is received, the seven low order address bits are internally incremented by one; the high order bits of the address will remain constant. If more than 128 bytes of data are transmitted, the address counter will roll over and the previously written data will be overwritten. The AT25P1024 is automatically returned to the write disable state at the completion of a WRITE cycle.

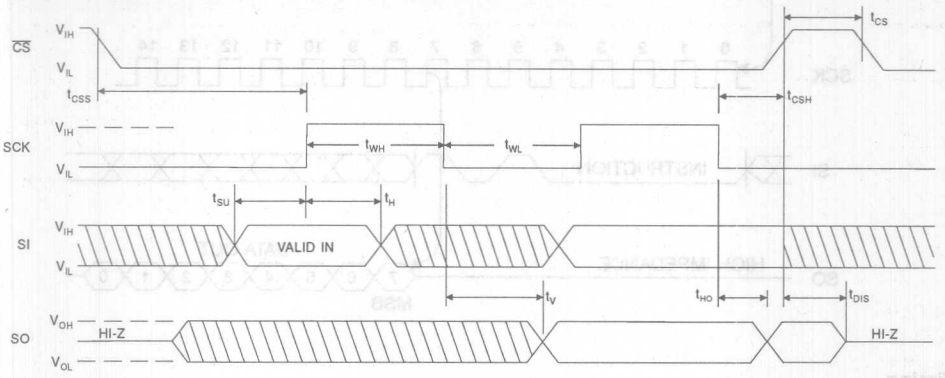
NOTE: If the device is not Write enabled (WREN), the device will ignore the Write instruction and will return to the standby state, when $\overline{CS}$ is brought high. A new CS falling edge is required to re-initiate the serial communication.

Table 6. Address Key

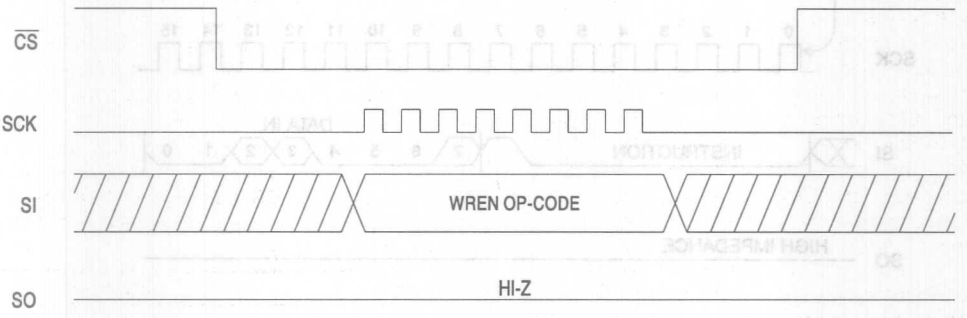
Address	AT25P1024
A_N	$A_{16} - A_0$
Don't Care Bits	$A_{23} - A_{17}$

Timing Diagrams (for SPI Mode 0 (0, 0))

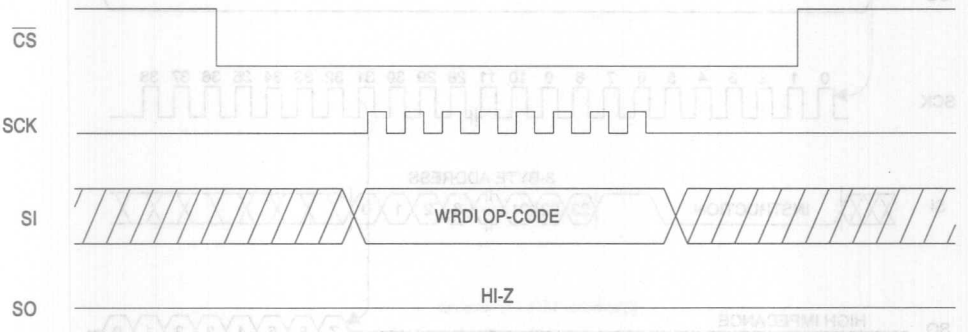
Synchronous Data Timing



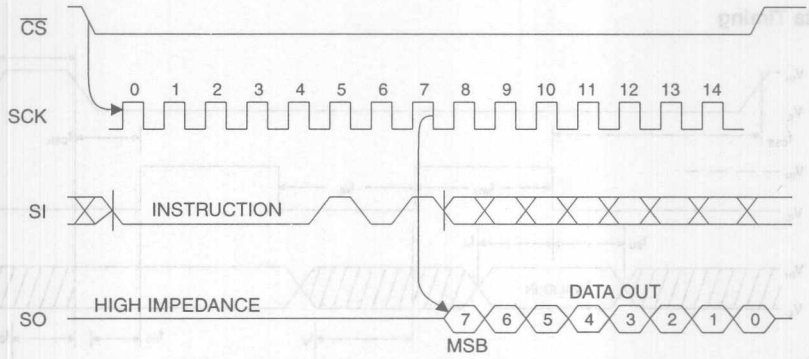
WREN Timing



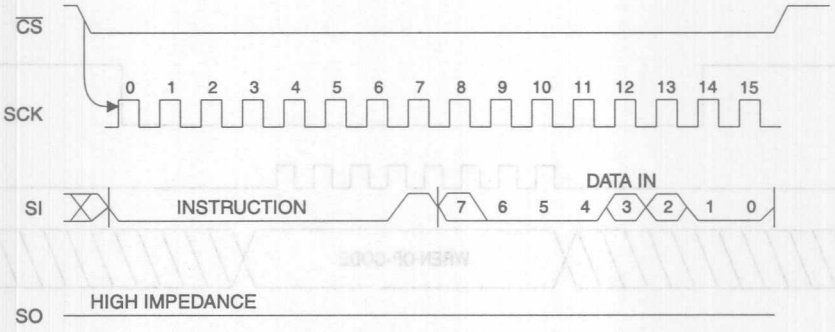
WRDI Timing



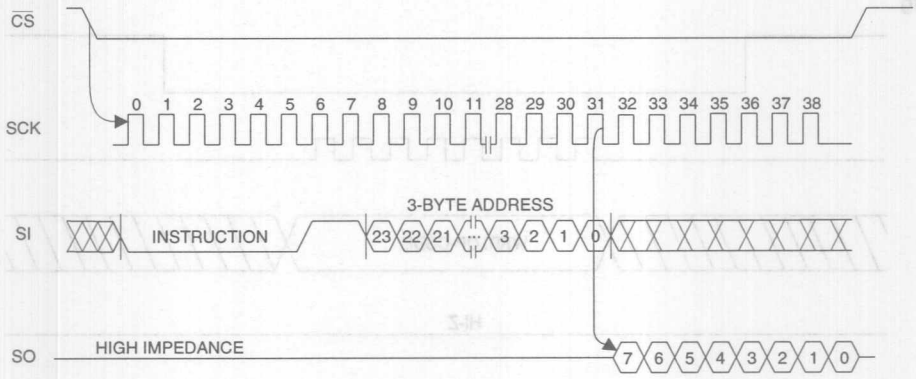
RDSR Timing



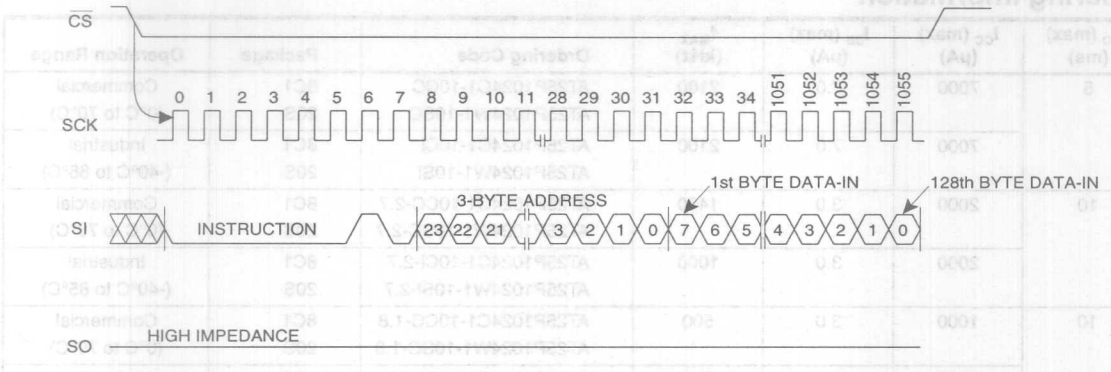
WRSR Timing



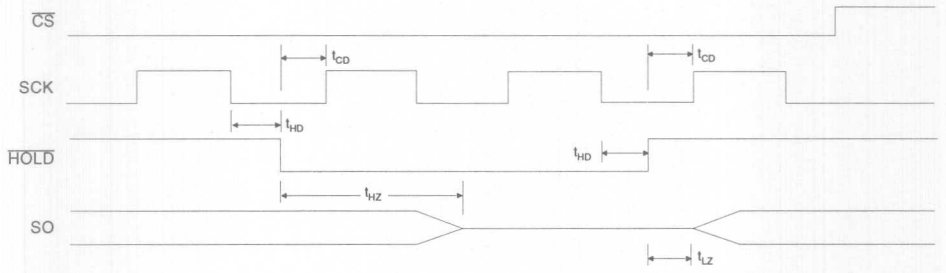
READ Timing



WRITE Timing



HOLD Timing



Ordering Information

t_{WC} (max) (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
5	7000	7.0	2100	AT25P1024C1-10CC AT25P1024W1-10SC	8C1 20S	Commercial (0°C to 70°C)
	7000	7.0	2100	AT25P1024C1-10CI AT25P1024W1-10SI	8C1 20S	Industrial (-40°C to 85°C)
10	2000	3.0	1400	AT25P1024C1-10CC-2.7 AT25P1024W1-10SC-2.7	8C1 20S	Commercial (0°C to 70°C)
	2000	3.0	1000	AT25P1024C1-10CI-2.7 AT25P1024W1-10SI-2.7	8C1 20S	Industrial (-40°C to 85°C)
10	1000	3.0	500	AT25P1024C1-10CC-1.8 AT25P1024W1-10SC-1.8	8C1 20S	Commercial (0°C to 70°C)
	1000	3.0	500	AT25P1024C1-10CI-1.8 AT25P1024W1-10SI-1.8	8C1 20S	Industrial (-40°C to 85°C)

Package Type	
8C1	8-Lead, 0.300" Wide, Leadless Array Package (LAP)
20S	20-Lead, 0.300" Wide, Plastic Gull Wing Small Outline Package (JEDEC SOIC)
Options	
Blank	Standard Device (4.5V to 5.5V)
-2.7	Low Voltage (2.7V to 5.5V)
-1.8	Low Voltage (1.8V to 3.6V)

Interfacing AT24CXX Serial EEPROMs with AT89CX051 Microcontrollers

Interfacing 24CXX Serial EEPROMs

Application Note

Serial memory devices offer significant advantages over parallel devices in applications where lower data transfer rates are acceptable. In addition to requiring less board space, serial devices allow microcontroller I/O pins to be conserved. This is especially valuable when adding external memory to low pin count microcontrollers such as the Atmel AT89C1051 and AT89C2051.

This application note presents a suite of software routines which may be incorporated into a user's application to allow an AT89CX051 microcontroller to read and write AT24CXX serial EEPROMs. The software supports all members of the AT24CXX family, and may easily be modified for compatibility with any of the Atmel 8051-code compatible microcontrollers.

Hardware

A typical interconnection between an AT89CX051 microcontroller and an AT24CXX serial EEPROM is shown in Figure 1. As indicated in the figure, up to eight members of the AT24CXX family may share the bus, utilizing the same two microcontroller I/O pins. Each device on the bus must have its address inputs (A0, A1, A2) hard-wired to a unique address. In the figure, the first device recognizes address zero (A0, A1, A2 tied low), while the eighth recognizes address seven (A0, A1, A2 tied high). Not all members of the AT24CXX family recognize all three address inputs, limiting the number of some devices which may be present to less than eight. The exact number of devices of each type which may share the bus is shown in Table 1.

Bidirectional Data Transfer Protocol

The Bidirectional Data Transfer Protocol utilized by the AT24CXX family allows a number of compatible devices to share a

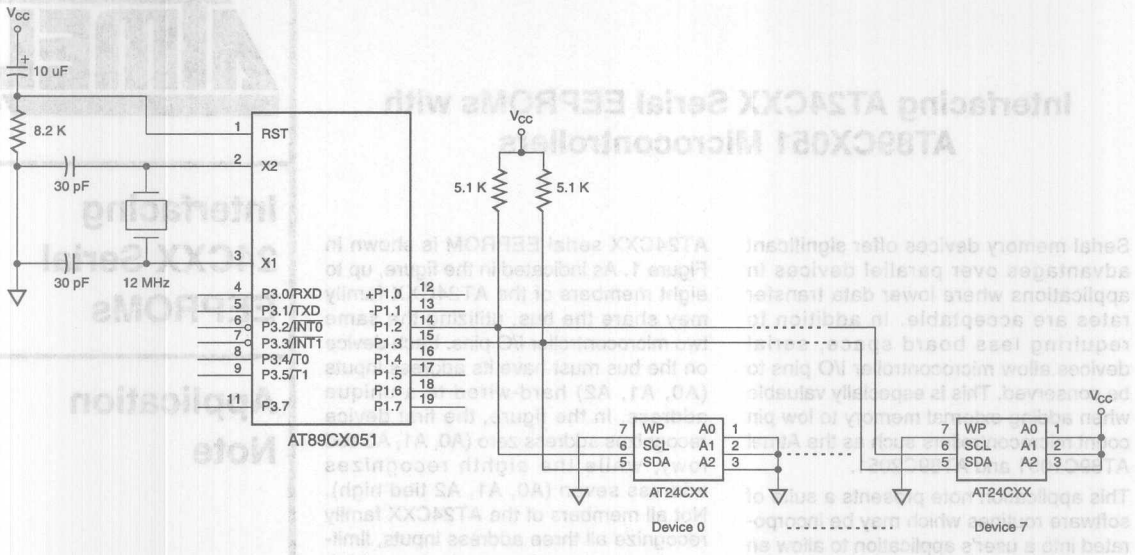
(continued)

Table 1. Atmel's 2-wire Serial EEPROM Family

Device	Size (Bytes)	Page Size (Bytes)	Max Per Bus	Addresses Used
AT24C01	1K	8	1	None
AT24C01A	1K	8	8	A0, A1, A2
AT24C02	2K	8	8	A0, A1, A2
AT24C04	4K	16	4	A1, A2
AT24C08	8K	16	2	A2
AT24C16	16K	16	1	None
AT24C164	16K	16	8	A0, A1, A2
AT24C32	32K	32	8	A0, A1, A2
AT24C64	64K	32	8	A0, A1, A2

Rev. 0507C–10/98

Figure 1. Typical Circuit Configuration



common 2-wire bus. The bus consists of a serial clock (SCL) line and a serial data (SDA) line. The clock is generated by the bus master and data is transmitted serially on the data line, most significant bit first, synchronized to the clock. The protocol supports bidirectional data transfers in 8-bit bytes.

In this application, the microcontroller serves as the bus master, initiating all data transfers and generating the clock which regulates the flow of data. The serial devices present on the bus are considered slaves, accepting or sending data in response to orders from the master.

The bus master initiates a data transfer by generating a start condition on the bus. This is followed by transmission of a byte containing the device address of the intended recipient. The device address consists of a 4-bit fixed portion and a 3-bit programmable portion. The fixed portion must match the value hard-wired into the slave, while the programmable portion allows the master to select between a maximum of eight slaves of similar type on the bus.

AT24CXX serial EEPROMs respond to device addresses with a fixed portion equal to '1010' and a programmable portion matching the address inputs (A0, A1, A2). Not all members of the AT24CXX family examine all three address inputs; Table 1 shows which of the three address inputs are valid for each member of the family.

The eighth bit in the device address byte specifies a write or read operation. After the eighth bit is transmitted, the master releases the data line and generates a ninth clock. If a slave has recognized the transmitted device address, it will respond to the ninth clock by generating an acknowledge condition on the data line. A slave which is busy when addressed may not generate an acknowledge. This is true for the AT24CXX when a write operation is in progress.

Following receipt of the slave's address acknowledgment, the master continues with the data transfer. If a write operation has been ordered, the master transmits the remaining data, with the slave acknowledging receipt of each byte. If the master has ordered a read operation, it releases the data line and clocks in data sent by the slave. After each byte is received, the master generates an acknowledge condition on the bus. The acknowledge is omitted following receipt of the last byte. The master terminates all operations by generating a stop condition on the bus. The master may also abort a data transfer at any time by generating a stop condition.

Refer to the AT24CXX family data sheets for detailed information on AT24CXX device operation and Bidirectional Data Transfer Protocol bus timing.

The software for this application may be obtained by downloading from Atmel's Web Site or BBS: (408) 436-4309. Consult the comment block at the beginning of the source code file for detailed information on features and operation.

Web Site: http://www.atmel.com

BBS: 1-(408) 436-4309

Interfacing AT93CXX Serial EEPROMs with AT89CX051 Microcontrollers

Serial memory devices offer significant advantages over parallel devices in applications where lower data transfer rates are acceptable. In addition to requiring less board space, serial devices allow microcontroller I/O pins to be conserved. This is especially valuable when adding external memory to low pin count microcontrollers such as the Atmel AT89C1051 and AT89C2051.

This application note presents a suite of software routines which may be incorporated into a user's application to allow AT89CX051 microcontrollers to read and write AT93CXX serial EEPROMs. All seven AT93CXX device functions are supported: read, write, write all, erase, erase all, erase/write enable and erase/write disable. The routines are general purpose, supporting both eight-bit and sixteen-bit accesses to all members of the 93CXX family. In addition, both 3-wire and 4-wire configurations are supported.

The AT93CXX may be connected to the AT89CX051 microcontroller in either a 3-wire (Figure 1) or 4-wire (Figure 2) configuration. In the 3-wire configuration, the EEPROM serial data in (DI) and serial data out (DO) pins are both connected to the same microcontroller I/O pin, thereby saving a pin. This is possible because the microcontroller I/O pins can be dynamically reprogrammed as input or output.

Note the strapping of the AT93CXX ORG pins shown in Figure 1 and Figure 2. The ORG (internal organization) pin selects 8-bit data when grounded and 16-bit data when floating or tied to V_{CC}. The ORG pin connections shown in the figures are for illustration only; 8-bit or 16-bit data may be selected in either the 3-wire or 4-wire configuration.

The software for this application may be obtained by downloading from Atmel's Web Site or BBS. Consult the comment block at the beginning of the source code file for detailed information on features and operation.

Web Site: http://www.atmel.com
BBS: 1-(408) 436-4309

Rev. 0521C–10/98

Figure 1. 3-Wire Configuration

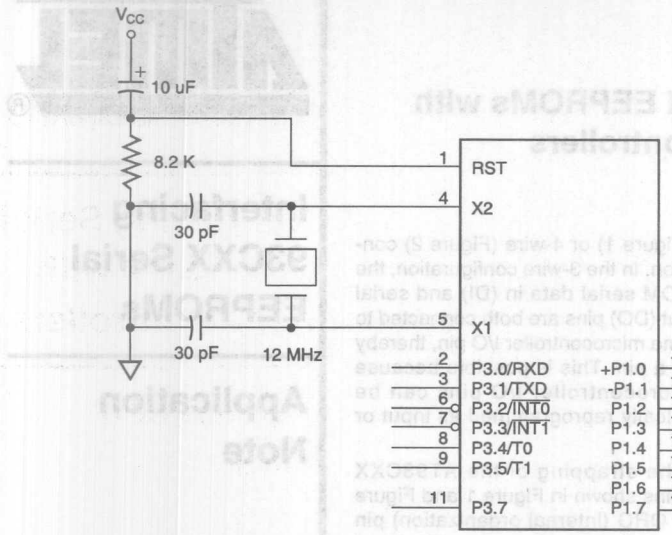
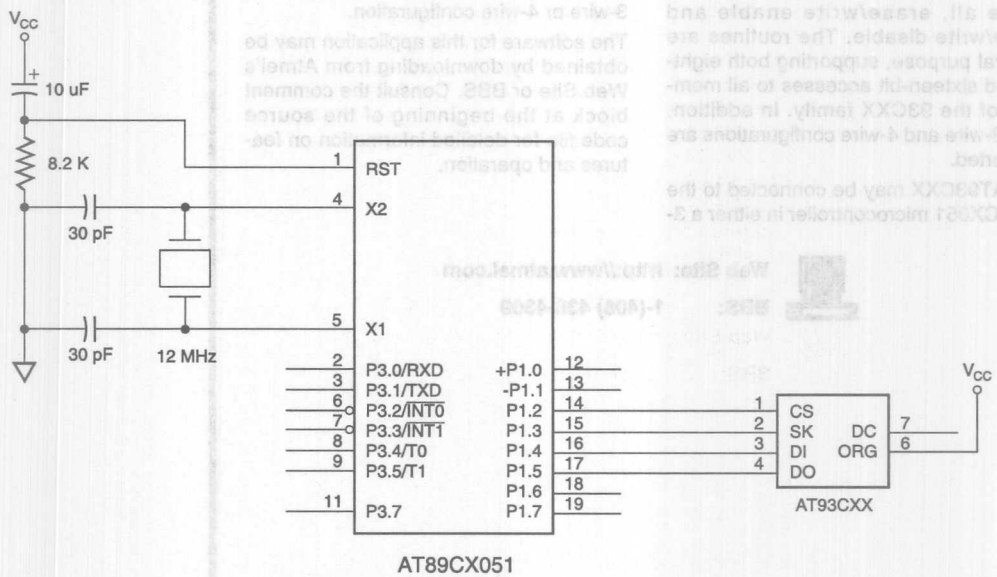


Figure 2. Typical Circuit Configuration



Interfacing AT25XXX Serial EEPROMs with AT89CXX Microcontrollers

Serial Peripheral Interface

Serial memory devices offer significant advantages over parallel devices in applications where lower data transfer rates are acceptable. In addition to requiring less board space, serial devices allow microcontroller I/O pins to be conserved. This is especially valuable when adding external memory to low pin count microcontrollers such as the Atmel AT89C1051 and AT89C2051.

This application note presents a suite of software routines which may be incorporated into a user's application to allow AT89CXX microcontrollers to read from and write to AT25XXX serial EEPROMs. All six AT25XXX device operations are supported: read memory, write memory, read status, write status, (set write protection levels), write enable and write disable. Routines are also provided to read from and write to memory utilizing the page mode of the AT25XXX. The software supports both 3-wire and 4-wire configurations and meets all AT25XXX family timing requirements when run on an AT89CXX microcontroller with a 24 MHz clock.

Hardware

The AT25XXX may be connected to the AT89CXX microcontroller in either a 3-wire (Figure 1) or 4-wire (Figure 2) configuration. In the 3-wire configuration, the EEPROM serial data in (SI) and serial data out (SO) pins are both connected to the same microcontroller I/O pin, thereby saving a pin. This is possible because the microcontroller I/O pins can be dynamically reprogrammed as input or output.

Software

Software for this application note may be downloaded from Atmel's Web Site or BBS. Consult the comment block at the beginning of the source code file for detailed information on features and operation.

Web Site: http://www.atmel.com

BBS: 1-(408) 436-4309

2

Interfacing Serial EEPROMs with Microcontrollers

Application Note

Rev. 0628C–10/98

Figure 1. 3-Wire Configuration

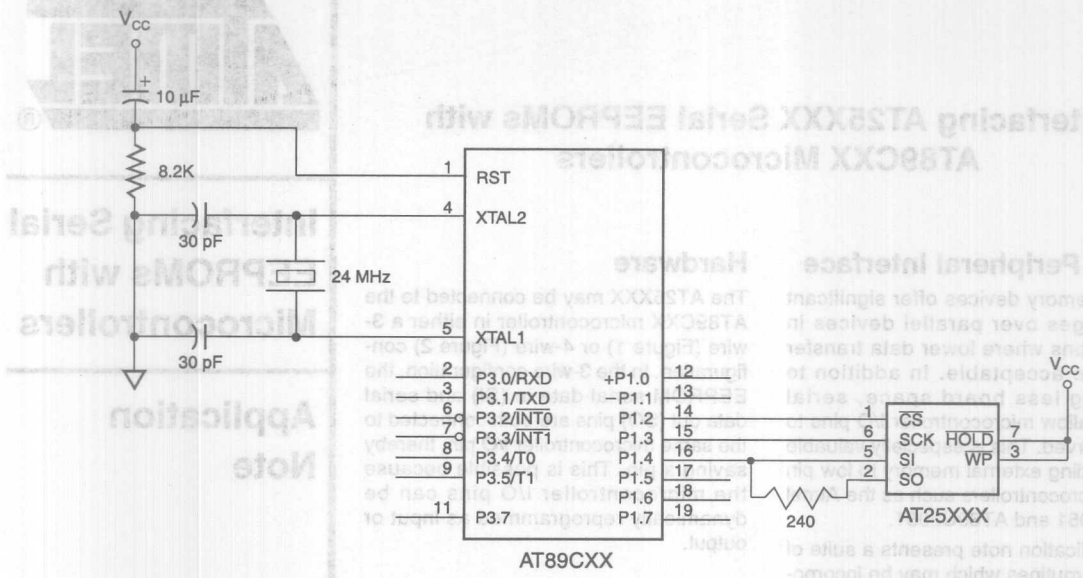
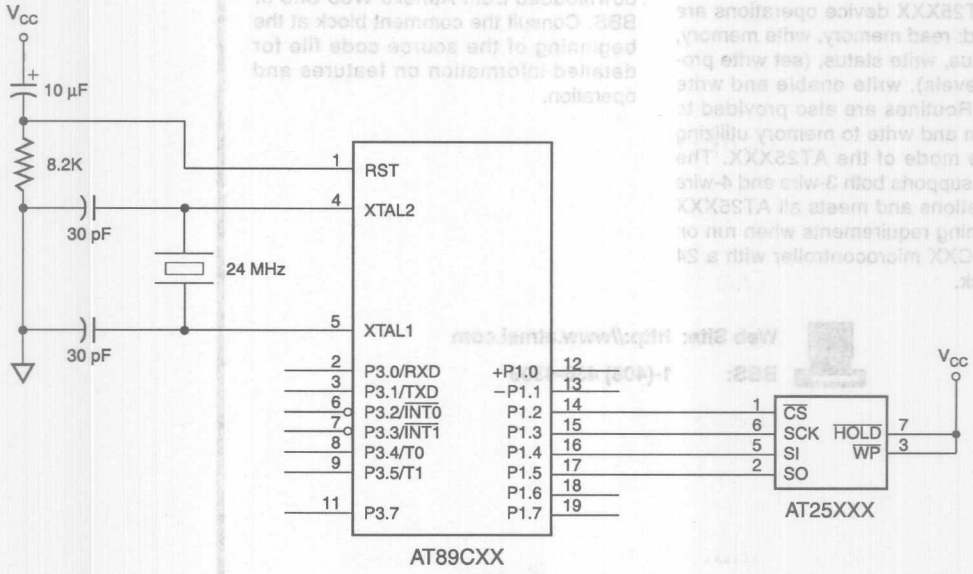


Figure 2. 4-Wire Configuration



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Package Outlines 9

Miscellaneous Information 10

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Features

- 2.7 to 3.6V Supply
  - Full Read and Write Operation
- Low Power Dissipation
  - 8 mA Active Current
  - 50 µA CMOS Standby Current
- Read Access Time - 250 ns
- Byte Write - 3 ms
- Direct Microprocessor Control
  - $\overline{\text{DATA}}$ Polling
  - READ/$\overline{\text{BUSY}}$ Open Drain Output on TSOP
- High Reliability CMOS Technology
  - Endurance: 100,000 Cycles
  - Data Retention: 10 Years
- Low Voltage CMOS Compatible Inputs and Outputs
- JEDEC Approved Byte Wide Pinout
- Commercial and Industrial Temperature Ranges

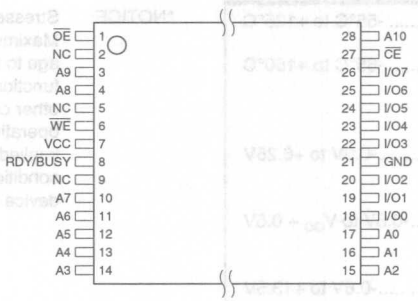
Description

The AT28BV16 is a low-power, high-performance Electrically Erasable and Programmable Read Only Memory with easy to use features. The AT28BV16 is a 16K memory organized as 2,048 words by 8 bits. The device is manufactured with Atmel's reliable nonvolatile CMOS technology. *(continued)*

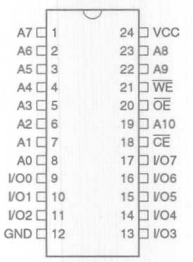
Pin Configurations

Pin Name	Function
A0 - A10	Addresses
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
RDY/$\overline{\text{BUSY}}$	Ready/$\overline{\text{Busy}}$ Output
NC	No Connect
DC	Don't Connect

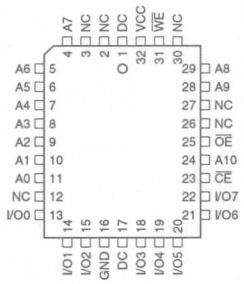
TSOP
Top View



PDIP, SOIC
Top View



PLCC
Top View



16K (2K x 8) *Battery-Voltage*™ Parallel EEPROMs

3

AT28BV16

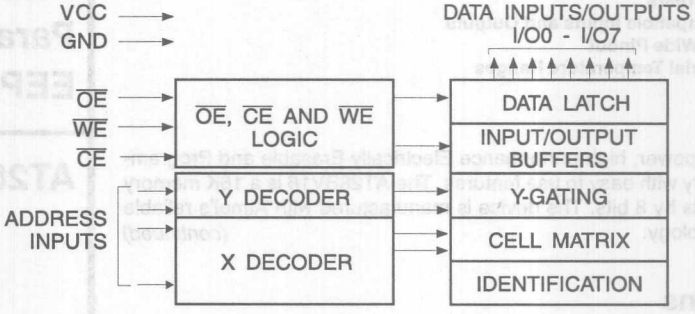
Rev. 0380B–10/98

The AT28BV16 is accessed like a static RAM for the read or write cycles without the need of external components. During a byte write, the address and data are latched internally, freeing the microprocessor address and data bus for other operations. Following the initiation of a write cycle, the device will go to a busy state and automatically clear and write the latched data using an internal control timer. The end of a write cycle can be determined by $\overline{DATA}$ polling of I/O_7. Once the end of a write cycle has been detected, a new access for a read or a write can begin.

The CMOS technology offers fast access times of 250 ns at low power dissipation. When the chip is deselected the standby current is less than 50 µA.

Atmel's 28BV16 has additional features to ensure high quality and manufacturability. The device utilizes error correction internally for extended endurance and for improved data retention characteristics. An extra 32-bytes of EEPROM are available for device identification or tracking.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V
Voltage on $\overline{OE}$ and A9 with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Device Operation

READ: The AT28BV16 is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in a high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual line control gives designers increased flexibility in preventing bus contention.

BYTE WRITE: Writing data into the AT28BV16 is similar to writing into a Static RAM. A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{OE}$ high and $\overline{CE}$ or $\overline{WE}$ low (respectively) initiates a byte write. The address location is latched on the last falling edge of $\overline{WE}$ (or $\overline{CE}$); the new data is latched on the first rising edge. Internally, the device performs a self-clear before write. Once a byte write has been started, it will automatically time itself to completion. Once a programming operation has been initiated and for the duration of t_{WC}, a read operation will effectively be a polling operation.

$\overline{DATA}$ POLLING: The AT28BV16 provides $\overline{DATA}$ POLLING to signal the completion of a write cycle. During a write cycle, an attempted read of the data being written results in the complement of that data for I/O_7 (the other outputs are indeterminate). When the write cycle is finished, true data appears on all outputs.

READY/$\overline{BUSY}$ (TSOP only): READY/$\overline{BUSY}$ is an open drain output; it is pulled low during the internal write cycle and released at the completion of the write cycle.

WRITE PROTECTION: Inadvertent writes to the device are protected against in the following ways: (a) V_{CC} sense—if V_{CC} is below 2.0V (typical) the write function is inhibited; (b) V_{CC} power on delay—once V_{CC} has reached 2.0V the device will automatically time out 5 ms (typical) before allowing a byte write; and (c) Write Inhibit—holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits byte write cycles.

DEVICE IDENTIFICATION: An extra 32-bytes of EEPROM memory are available to the user for device identification. By raising A9 to 12 ± 0.5V and using address locations 7E0H to 7FFH the additional bytes may be written to or read from in the same manner as the regular memory array.

3

DC and AC Operating Range

		AT28BV16-25	AT28BV16-30
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		2.7V to 3.6V	2.7V to 3.6V

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write[2]	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X[1]	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to AC Programming Waveforms.

DC Characteristics

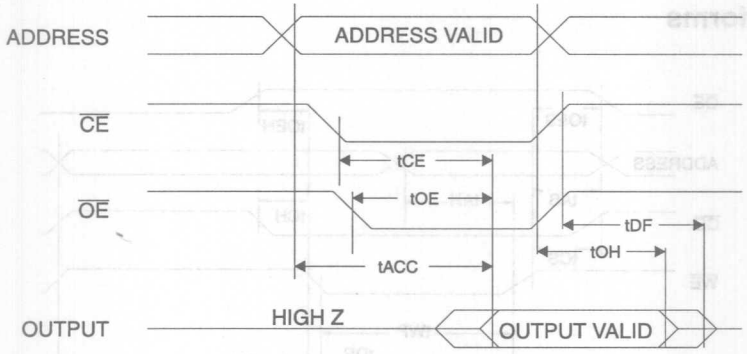
Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC} + 1.0V		5	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}		5	µA
I_{SB}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3V to V_{CC} + 1.0V		50	µA
I_{CC}	V_{CC} Active Current AC	f = 5 MHz; I_{OUT} = 0 mA; CE = V_{IL}		8	mA
V_{IL}	Input Low Voltage			0.6	V
V_{IH}	Input High Voltage		2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 1 mA		0.3	V
		I_{OL} = 2 mA for RDY/$\overline{BUSY}$		0.3	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA	2.0		V

AC Read Characteristics

Symbol	Parameter	AT28BV16-25		AT28BV16-30		Units
		Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		250		300	ns
t_{CE}[1]	$\overline{CE}$ to Output Delay		250		300	ns
t_{OE}[2]	$\overline{OE}$ to Output Delay		100		100	ns
t_{DF}[3][4]	$\overline{CE}$ or $\overline{OE}$ High to Output Float	0	55	0	55	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		ns

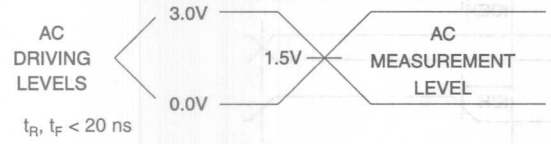
3

AC Read Waveforms[1][2][3][4]

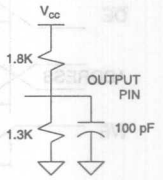


Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



Output Test Load



Pin Capacitance

f = 1 MHz, T = 25°C[1]

Symbol	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

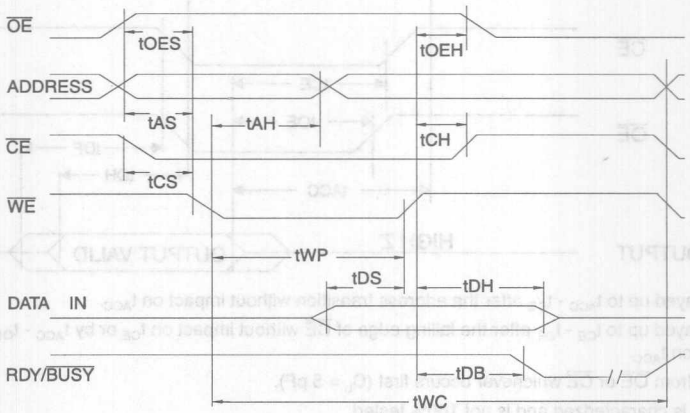
Note: 1. This parameter is characterized and is not 100% tested.

AC Write Characteristics

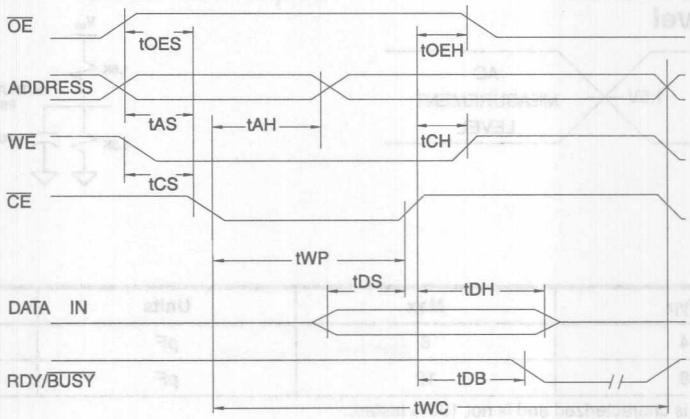
Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	10		ns
t_{AH}	Address Hold Time	100		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	150	1000	ns
t_{DS}	Data Set-up Time	100		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	10		ns
t_{CS}, t_{CH}	$\overline{CE}$ to $\overline{WE}$ and $\overline{WE}$ to $\overline{CE}$ Set-up and Hold Time	0		ns
t_{WC}	Write Cycle Time		3.0	ms
t_{DB}	Time to Device Busy		50	ns

AC Write Waveforms

$\overline{WE}$ Controlled



$\overline{CE}$ Controlled

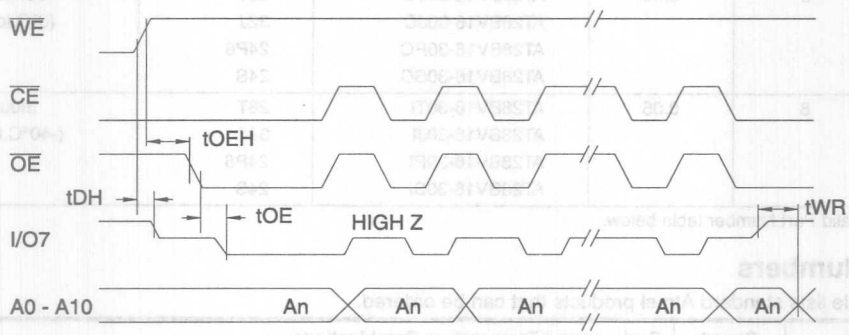


$\overline{\text{Data}}$ Polling Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay[2]				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See AC Characteristics.

$\overline{\text{Data}}$ Polling Waveforms



Ordering Information[1]

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
250	8	0.05	AT28BV16-25TC	28T	Commercial
			AT28BV16-25JC	32J	(0°C to 70°C)
			AT28BV16-25PC	24P6	
			AT28BV16-25SC	24S	
	8	0.05	AT28BV16-25TI	28T	Industrial
			AT28BV16-25JI	32J	(-40°C to 85°C)
			AT28BV16-25PI	24P6	
			AT28BV16-25SI	24S	
300	8	0.05	AT28BV16-30TC	28T	Commercial
			AT28BV16-30JC	32J	(0°C to 70°C)
			AT28BV16-30PC	24P6	
			AT28BV16-30SC	24S	
	8	0.05	AT28BV16-30TI	28T	Industrial
			AT28BV16-30JI	32J	(-40°C to 85°C)
			AT28BV16-30PI	24P6	
			AT28BV16-30SI	24S	

Note: 1. See Valid Part Number table below.

Valid Part Numbers

The following table lists standard Atmel products that can be ordered.

Device Numbers	Speed	Package and Temperature Combinations
AT28BV16	25	JC, JI, PC, PI, SC, SI, TC, TI
AT28BV16	30	JC, JI, PC, PI, SC, SI, TC, TI

Die Products

Reference Section: Parallel EEPROM Die Products

Package Type	
28T	28-Lead, Plastic Thin Small Outline Package (TSOP)
32J	32-Lead, Plastic J-Leaded Chip Carrier (PLCC)
24P6	24-Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
24S	24-Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)

Features

- Single 2.7V - 3.6V Supply
- Fast Read Access Time - 200 ns
- Automatic Page Write Operation
  - Internal Address and Data Latches for 64 Bytes
  - Internal Control Timer
- Fast Write Cycle Times
  - Page Write Cycle Time: 10 ms Maximum
  - 1- to 64-Byte Page Write Operation
- Low Power Dissipation
  - 15 mA Active Current
  - 20 µA CMOS Standby Current
- Hardware and Software Data Protection
- $\overline{\text{DATA}}$ Polling for End of Write Detection
- High Reliability CMOS Technology
  - Endurance: 10,000 Cycles
  - Data Retention: 10 Years
- JEDEC Approved Byte-Wide Pinout
- Commercial and Industrial Temperature Ranges

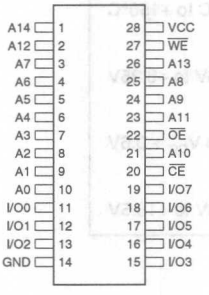
Description

The AT28BV256 is a high-performance Electrically Erasable and Programmable Read Only Memory. Its 256K of memory is organized as 32,768 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 200 ns with power dissipation of just 54 mW. When the device is deselected, the CMOS standby current is less than 200 µA. *(continued)*

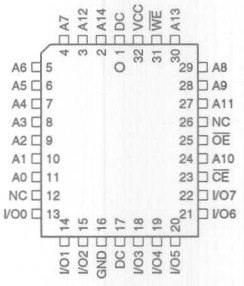
Pin Configurations

Pin Name	Function
A0 - A14	Addresses
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect
DC	Don't Connect

PDIP, SOIC
Top View

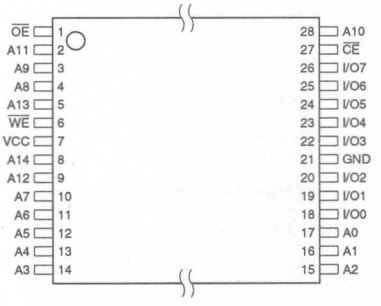


PLCC
Top View



Note: PLCC package pins 1 and 17 are DON'T CONNECT.

TSOP
Top View



256K (32K x 8) *Battery-Voltage*™ Parallel EEPROMs

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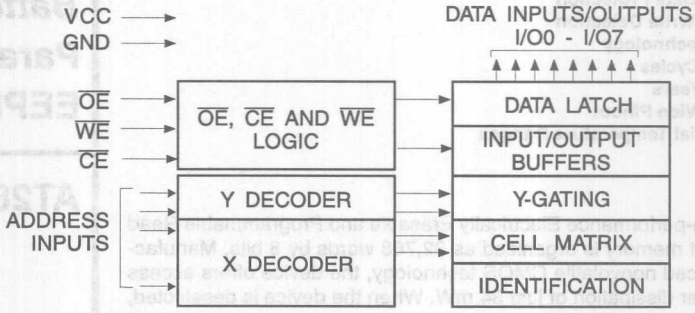
AT28BV256

Rev. 0273F–10/98

The AT28BV256 is accessed like a Static RAM for the read or write cycle without the need for external components. The device contains a 64-byte page register to allow writing of up to 64 bytes simultaneously. During a write cycle, the addresses and 1 to 64 bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by $\overline{DATA}$ polling of I/O7. Once the end of a write cycle has been detected a new access for a read or write can begin.

Atmel's 28BV256 has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and improved data retention characteristics. An optional software data protection mechanism is available to guard against inadvertent writes. The device also includes an extra 64 bytes of EEPROM for device identification or tracking.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V
Voltage on $\overline{OE}$ and A9 with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Device Operation

READ: The AT28BV256 is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state when either $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention in their system.

BYTE WRITE: A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high initiates a write cycle. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Once a byte write has been started it will automatically time itself to completion. Once a programming operation has been initiated and for the duration of t_{WC}, a read operation will effectively be a polling operation.

PAGE WRITE: The page write operation of the AT28BV256 allows 1 to 64 bytes of data to be written into the device during a single internal programming period. A page write operation is initiated in the same manner as a byte write; the first byte written can then be followed by 1 to 63 additional bytes. Each successive byte must be written within 150 µs (t_{BLC}) of the previous byte. If the t_{BLC} limit is exceeded the AT28BV256 will cease accepting data and commence the internal programming operation. All bytes during a page write operation must reside on the same page as defined by the state of the A6 - A14 inputs. For each $\overline{WE}$ high to low transition during the page write operation, A6 - A14 must be the same.

The A0 to A5 inputs are used to specify which bytes within the page are to be written. The bytes may be loaded in any order and may be altered within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

$\overline{DATA}$ POLLING: The AT28BV256 features $\overline{DATA}$ Polling to indicate the end of a write cycle. During a byte or page write cycle an attempted read of the last byte written will result in the complement of the written data to be presented on I/O7. Once the write cycle has been completed, true data is valid on all outputs, and the next write cycle may begin. $\overline{DATA}$ Polling may begin at anytime during the write cycle.

TOGGLE BIT: In addition to $\overline{DATA}$ Polling the AT28BV256 provides another method for determining the end of a write cycle. During the write operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the write has completed, I/O6 will stop toggling and valid data will be read. Reading the toggle bit may begin at any time during the write cycle.

DATA PROTECTION: If precautions are not taken, inadvertent writes may occur during transitions of the host system power supply. Atmel has incorporated both hardware and software features that will protect the memory against inadvertent writes.

HARDWARE PROTECTION: Hardware features protect against inadvertent writes to the AT28BV256 in the following ways: (a) V_{CC} power-on delay—once V_{CC} has reached 1.8V (typical) the device will automatically time out 10 ms (typical) before allowing a write; (b) write inhibit—holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits write cycles; and (c) noise filter—pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a write cycle.

SOFTWARE DATA PROTECTION: A software-controlled data protection feature has been implemented on the AT28BV256. Software data protection (SDP) helps prevent inadvertent writes from corrupting the data in the device. SDP can prevent inadvertent writes during power-up and power-down as well as any other potential periods of system instability.

The AT28BV256 can only be written using the software data protection feature. A series of three write commands to specific addresses with specific data must be presented to the device before writing in the byte or page mode. The same three write commands must begin each write operation. All software write commands must obey the page mode write timing specifications. The data in the 3-byte command sequence is not written to the device; the address in the command sequence can be utilized just like any other location in the device.

Any attempt to write to the device without the 3-byte sequence will start the internal write timers. No data will be written to the device; however, for the duration of t_{WC}, read operations will effectively be polling operations.

DEVICE IDENTIFICATION: An extra 64 bytes of EEPROM memory are available to the user for device identification. By raising A9 to 12V ± 0.5V and using address locations 7FC0H to 7FFFH the additional bytes may be written to or read from in the same manner as the regular memory array.

DC and AC Operating Range

		AT28BV256-20	AT28BV256-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		2.7V - 3.6V	2.7V - 3.6V

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write[2]	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X[1]	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z
Chip Erase	V_{IL}	V_H[3]	V_{IL}	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to AC Programming Waveforms.
3. $V_H = 12.0V \pm 0.5V$.

DC Characteristics

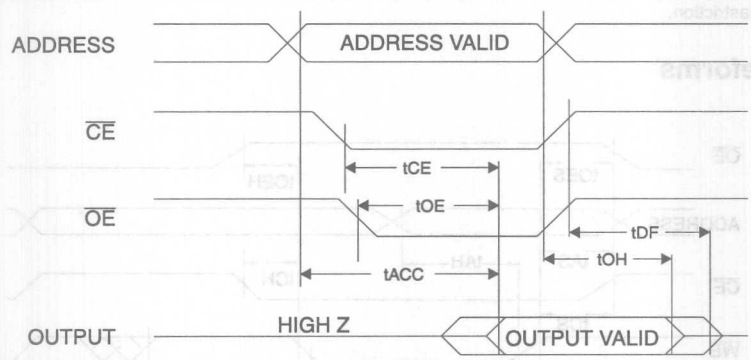
Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	$V_{IN} = 0V$ to $V_{CC} + 1V$			10	µA
I_{LO}	Output Leakage Current	$V_{I/O} = 0V$ to V_{CC}			10	µA
I_{SB}	V_{CC} Standby Current CMOS	$\overline{CE} = V_{CC} - 0.3V$ to $V_{CC} + 1V$	Com.		20	µA
			Ind.		50	µA
I_{CC}	V_{CC} Active Current	f = 5 MHz; I_{OUT} = 0 mA			15	mA
V_{IL}	Input Low Voltage				0.6	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	$I_{OL} = 1.6$ mA			0.3	V
V_{OH}	Output High Voltage	$I_{OH} = -100$ µA		2.0		V

AC Read Characteristics

Symbol	Parameter	AT28BV256-20		AT28BV256-25		Units
		Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		200		250	ns
t_{CE}[1]	$\overline{CE}$ to Output Delay		200		250	ns
t_{OE}[2]	$\overline{OE}$ to Output Delay	0	80	0	100	ns
t_{DF}[3][4]	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	55	0	60	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		ns

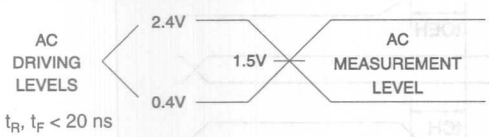
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AC Read Waveforms[1][2][3][4]

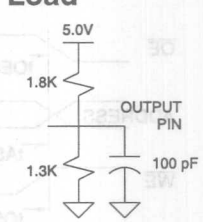


Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



Output Test Load



Pin Capacitance

f = 1 MHz, T = 25°C[1]

Symbol	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

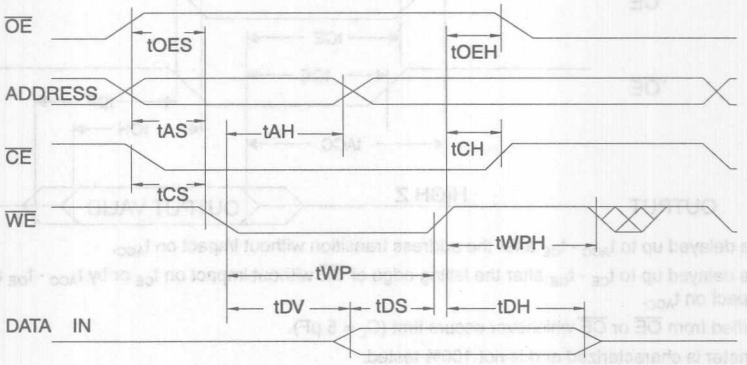
AC Write Characteristics

Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	200		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	0		ns
t_{DV}	Time to Data Valid	NR(1)		

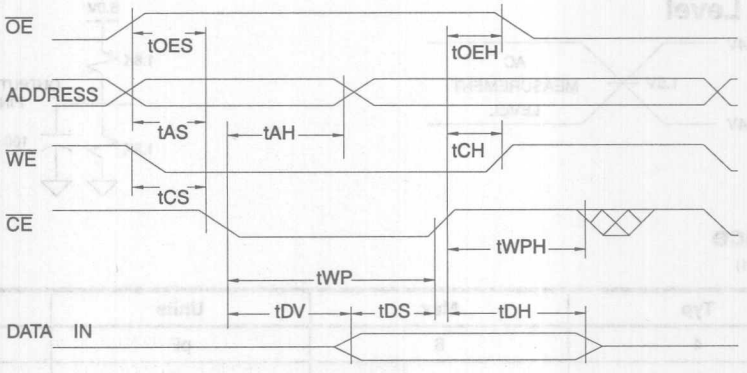
Note: 1. NR = No Restriction.

AC Write Waveforms

$\overline{WE}$ Controlled



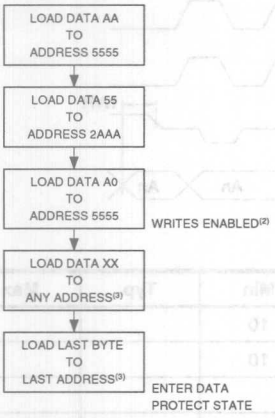
$\overline{CE}$ Controlled



Page Mode Characteristics

Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time		10	ms
t_{AS}	Address Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}	Data Hold Time	0		ns
t_{WP}	Write Pulse Width	200		ns
t_{BLC}	Byte Load Cycle Time		150	µs
t_{WPH}	Write Pulse Width High	100		ns

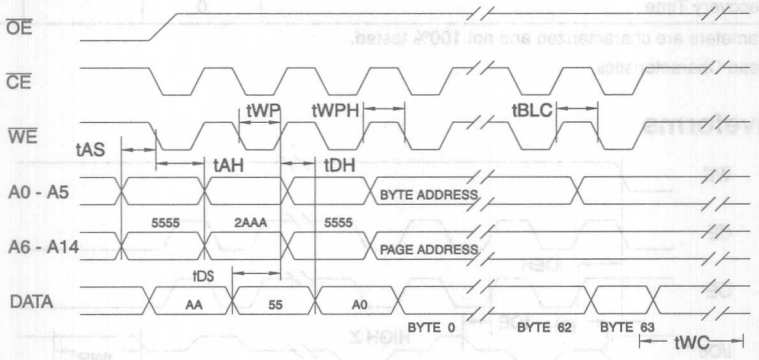
Programming Algorithm



Notes for software program code:

1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Data protect state will be re-activated at the end of program cycle.
3. 1 to 64 bytes of data are loaded.

Software Protected Program Cycle Waveforms(1)(2)(3)



Notes: 1. A0 - A14 must conform to the addressing sequence for the first three bytes as shown above.

2. A6 through A14 must specify the same page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$) after the software code has been entered.

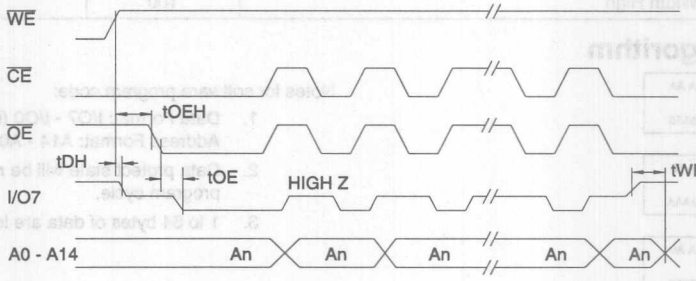
3. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

$\overline{\text{Data}}$ Polling Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	0			ns
t_{OEH}	$\overline{OE}$ Hold Time	0			ns
t_{OE}	$\overline{OE}$ to Output Delay[2]				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See AC Read Characteristics.

$\overline{\text{Data}}$ Polling Waveforms

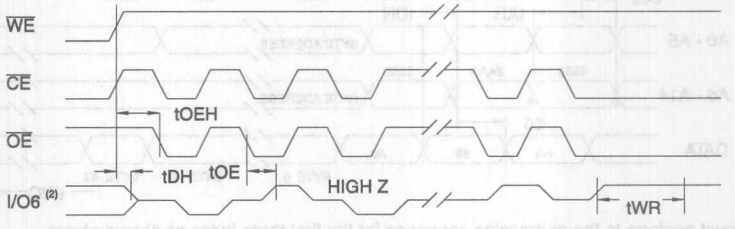


Toggle Bit Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay[2]				ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

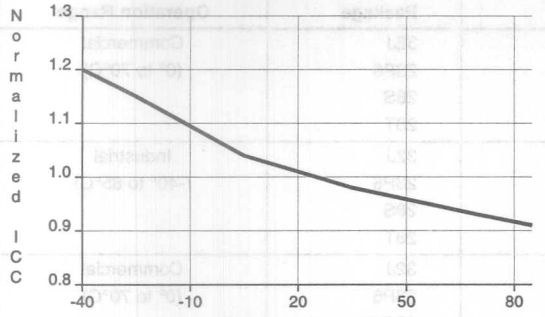
Notes: 1. These parameters are characterized and not 100% tested.
2. See AC Read Characteristics.

Toggle Bit Waveforms

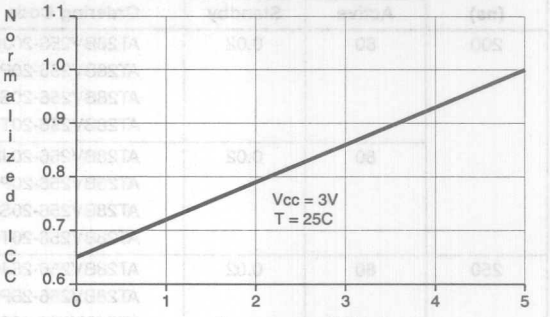


Notes: 1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

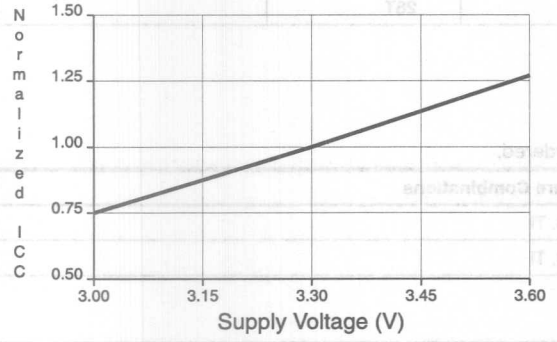
NORMALIZED SUPPLY CURRENT vs. TEMPERATURE



NORMALIZED SUPPLY CURRENT vs. ADDRESS FREQUENCY



NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



3

Ordering Information[1]

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
200	80	0.02	AT28BV256-20JC	32J	Commercial
			AT28BV256-20PC	28P6	(0° to 70°C)
			AT28BV256-20SC	28S	
			AT28BV256-20TC	28T	
	80	0.02	AT28BV256-20JI	32J	Industrial
			AT28BV256-20PI	28P6	(-40° to 85°C)
			AT28BV256-20SI	28S	
			AT28BV256-20TI	28T	
250	80	0.02	AT28BV256-25JC	32J	Commercial
			AT28BV256-25PC	28P6	(0° to 70°C)
			AT28BV256-20SC	28S	
			AT28BV256-25TC	28T	
	80	0.02	AT28BV256-25JI	32J	Industrial
			AT28BV256-25PI	28P6	(-40° to 85°C)
			AT28BV256-20SI	28S	
			AT28BV256-25TI	28T	

Note: 1. See Valid Part Numbers table below.

Valid Part Numbers

The following table lists standard Atmel products that can be ordered.

Device Numbers	Speed	Package and Temperature Combinations
AT28BV256	20	JC, JI, PC, PI, SC, SI, TC, TI
AT28BV256	25	JC, JI, PC, PI, SC, SI, TC, TI

Die Products

Reference Section: Parallel EEPROM Die Products

Package Type	
32J	32-Lead, Plastic J-Leaded Chip Carrier (PLCC)
28P6	28-Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
28S	28-Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
28T	28-Lead, Plastic Thin Small Outline Package (TSOP)

Features

- 2.7V to 3.6V Supply
  - Full Read and Write Operation
- Low Power Dissipation
  - 8 mA Active Current
  - 50 µA CMOS Standby Current
- Read Access Time - 300 ns
- Byte Write - 3 ms
- Direct Microprocessor Control
  - $\overline{\text{DATA}}$ Polling
  - READY/$\overline{\text{BUSY}}$ Open Drain Output
- High Reliability CMOS Technology
  - Endurance: 100,000 Cycles
  - Data Retention: 10 Years
- JEDEC Approved Byte-Wide Pinout
- Commercial and Industrial Temperature Ranges

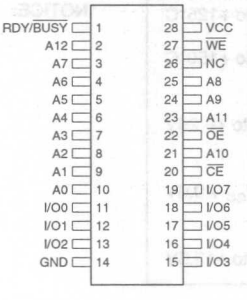
Description

The AT28BV64 is a low-voltage, low-power Electrically Erasable and Programmable Read Only Memory specifically designed for battery powered applications. Its 64K of memory is organized 8,192 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 200 ns with power dissipation less than 30 mW. When the device is deselected the standby current is less than 50 µA. *(continued)*

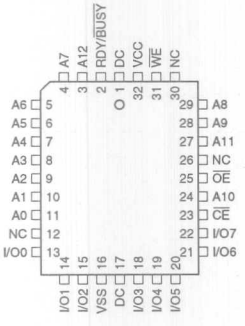
Pin Configurations

Pin Name	Function
A0 - A12	Addresses
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
RDY/$\overline{\text{BUSY}}$	Ready/Busy Output
NC	No Connect
DC	Don't Connect

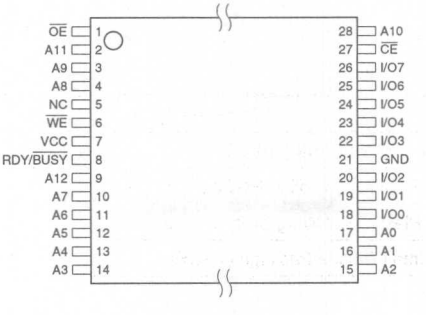
PDIP, SOIC
Top View



PLCC
Top View



TSOP
Top View



64K (8K x 8) *Battery-Voltage*™ Parallel EEPROMs

AT28BV64

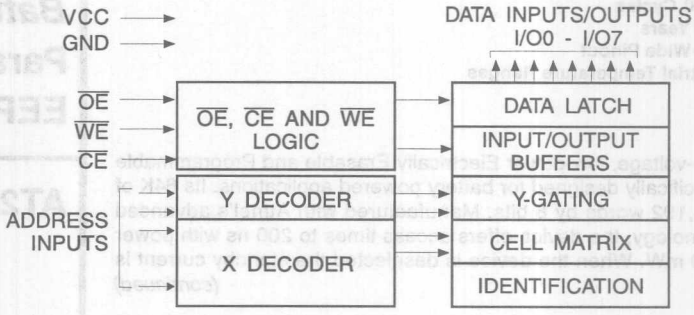
3

Rev. 0493A–10/98

The AT28BV64 is accessed like a Static RAM for the read or write cycles without the need for external components. During a byte write, the address and data are latched internally, freeing the microprocessor address and data bus for other operations. Following the initiation of a write cycle, the device will go to a busy state and automatically clear and write the latched data using an internal control timer. The device includes two methods for detecting the end of a write cycle, level detection of RDY/$\overline{BUSY}$ and $\overline{DATA}$ polling of I/O_7. Once the end of a write cycle has been detected, a new access for a read or write can begin.

Atmel's 28BV64 has additional features to ensure high quality and manufacturability. The device utilizes error correction internally for extended endurance and for improved data retention characteristics. An extra 32-bytes of EEPROM are available for device identification or tracking.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V
Voltage on $\overline{OE}$ and A9 with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Device Operation

READ: The AT28BV64 is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in a high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual line control gives designers increased flexibility in preventing bus contention.

BYTE WRITE: Writing data into the AT28BV64 is similar to writing into a Static RAM. A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{OE}$ high and $\overline{CE}$ or $\overline{WE}$ low (respectively) initiates a byte write. The address location is latched on the falling edge of $\overline{WE}$ (or $\overline{CE}$); the new data is latched on the rising edge. Internally, the device performs a self-clear before write. Once a byte write has been started, it will automatically time itself to completion. Once a programming operation has been initiated and for the duration of t_{WC}, a read operation will effectively be a polling operation.

READY/$\overline{BUSY}$: Pin 1 is an open drain READY/$\overline{BUSY}$ output that can be used to detect the end of a write cycle. RDY/$\overline{BUSY}$ is actively pulled low during the write cycle and is released at the completion of the write. The open drain connection allows for OR-tying of several devices to the same RDY/$\overline{BUSY}$ line.

$\overline{DATA}$ POLLING: The AT28BV64 provides $\overline{DATA}$ POLLING to signal the completion of a write cycle. During a write cycle, an attempted read of the data being written results in the complement of that data for I/O_7 (the other outputs are indeterminate). When the write cycle is finished, true data appears on all outputs.

WRITE PROTECTION: Inadvertent writes to the device are protected against in the following ways: (a) V_{CC} sense—if V_{CC} is below 1.8V (typical) the write function is inhibited; (b) V_{CC} power on delay—once V_{CC} has reached 2.0V the device will automatically time out 10 ms (typical) before allowing a byte write; and (c) Write Inhibit—holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits byte write cycles.

3

DC and AC Operating Range

		AT28BV64-30
Operating Temperature (Case)	Com.	0°C - 70°C
	Ind.	-40°C - 85°C
V_{CC} Power Supply		2.7V to 3.6V

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write[2]	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X[1]	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to AC Programming Waveforms.

DC Characteristics

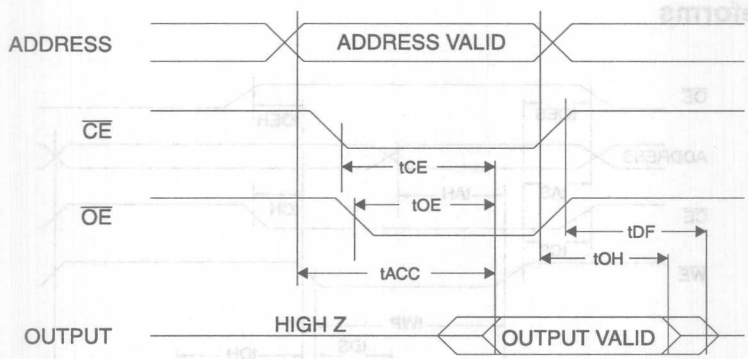
Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC} + 1.0V		5	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}		5	µA
I_{SB}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3V to V_{CC} + 1.0V		50	µA
I_{CC}	V_{CC} Active Current AC	f = 5 MHz; I_{OUT} = 0 mA; CE = V_{IL}		8	mA
V_{IL}	Input Low Voltage			0.6	V
V_{IH}	Input High Voltage		2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 1 mA		0.3	V
		I_{OL} = 2 mA for RDY/$\overline{BUSY}$		0.3	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA	2.0		V

AC Read Characteristics

Symbol	Parameter	AT28BV64-30		Units
		Min	Max	
t_{ACC}	Address to Output Delay		300	ns
t_{CE}[1]	$\overline{CE}$ to Output Delay		300	ns
t_{OE}[2]	$\overline{OE}$ to Output Delay	0	150	ns
t_{DF}[3][4]	$\overline{CE}$ or $\overline{OE}$ High to Output Float	0	60	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		ns

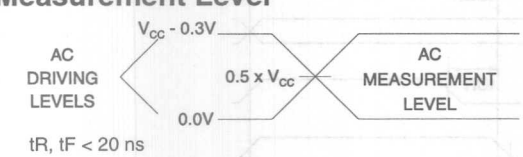
3

AC Read Waveforms[1][2][3][4]



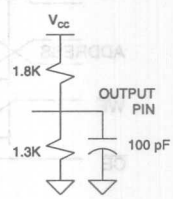
Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



tR, tF < 20 ns

Output Test Load



Pin Capacitance

f = 1 MHz, T = 25°C[1]

Symbol	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

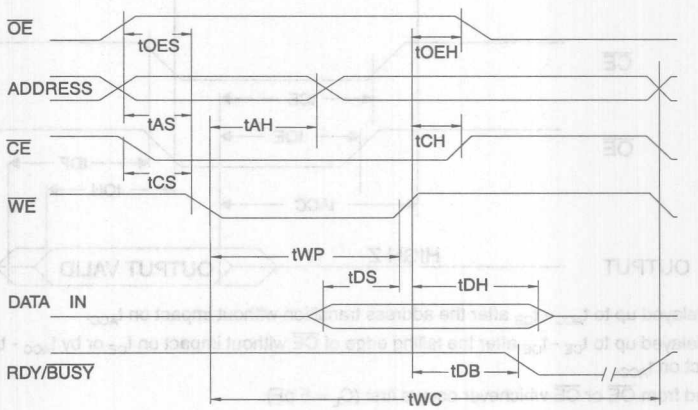
Note: 1. This parameter is characterized and is not 100% tested.

AC Write Characteristics

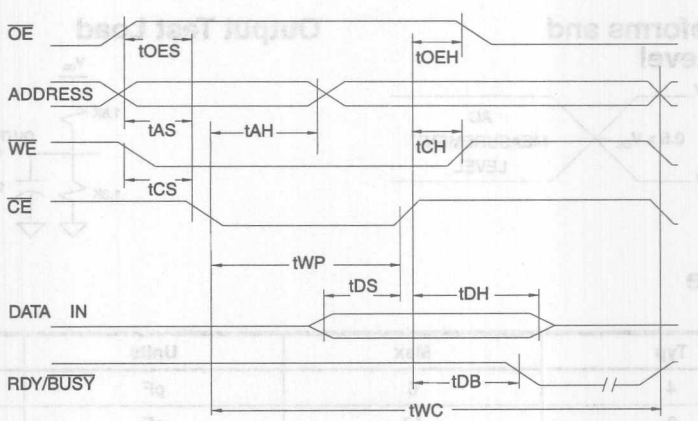
Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	10		ns
t_{AH}	Address Hold Time	100		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	150	1000	ns
t_{DS}	Data Set-up Time	100		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	10		ns
t_{DB}	Time to Device Busy		50	ns
t_{WC}	Write Cycle Time		3	ms

AC Write Waveforms

$\overline{WE}$ Controlled



$\overline{CE}$ Controlled

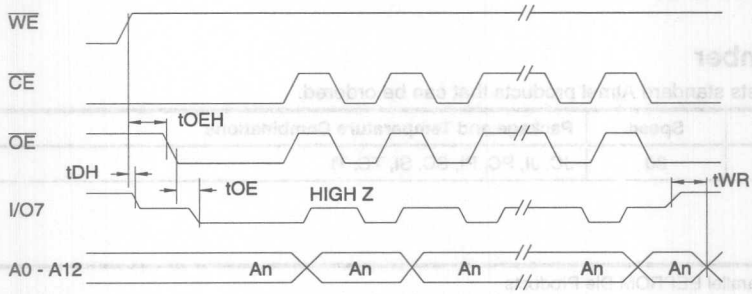


$\overline{\text{Data}}$ Polling Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay[2]				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See AC Characteristics.

$\overline{\text{Data}}$ Polling Waveforms



Ordering Information[1]

t_{ACC} (ns)	I_{CC} (mA)		Operating Voltage	Ordering Code	Package	Operation Range
	Active	Standby				
300	8	0.05	2.7V to 3.6V	AT28BV64-30JC	32J	Commercial (0°C to 70°C)
				AT28BV64-30PC	28P6	
				AT28BV64-30SC	28S	
				AT28BV64-30SC	28T	
	8	0.05	2.7V to 3.6V	AT28BV64-30JI	32J	Industrial (-40°C to 85°C)
				AT28BV64-30PI	28P6	
				AT28BV64-30SI	28S	
				AT28BV64-30TI	28T	

Note: 1. See Valid Part Number table below.

Valid Part Number

The following table lists standard Atmel products that can be ordered.

Device Numbers	Speed	Package and Temperature Combinations
AT28BV64	30	JC, JI, PC, PI, SC, SI, TC, TI

Die Products

Reference Section: Parallel EEPROM Die Products

Package Type	
32J	32-Lead, Plastic J-Leaded Chip Carrier (PLCC)
28P6	28-Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
28S	28-Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
28T	28-Lead, Plastic Thin Small Outline Package (TSOP)

Features

- Single 3.3V ± 10% Supply
- 3-Volt Only Read and Write Operation
- Hardware and Software Data Protection
- Low Power Dissipation
  - 15 mA Active Current
  - 20 µA CMOS Standby Current
- Fast Read Access Time - 200 ns
- Automatic Page Write Operation
  - Internal Address and Data Latches for 64 Bytes
  - Internal Control Timer
- Fast Write Cycle Times
  - Page Write Cycle Time: 10 ms Maximum
  - 1 to 64 Byte Page Write Operation
- $\overline{\text{DATA}}$ Polling for End of Write Detection
- High Reliability CMOS Technology
  - Endurance: 100,000 Cycles
  - Data Retention: 10 Years
- JEDEC Approved Byte-Wide Pinout
- Commercial and Industrial Temperature Ranges

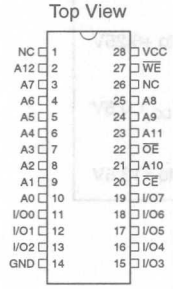
Description

The AT28BV64B is a high-performance electrically erasable programmable read only memory (EEPROM). Its 64K of memory is organized as 8,192 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 200 ns with power dissipation of just 54 mW. When the device is deselected, the CMOS standby current is less than 20 µA. *(continued)*

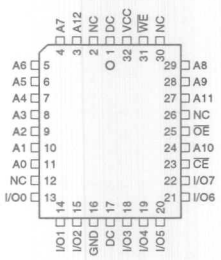
Pin Configurations

Pin Name	Function
A0 - A12	Addresses
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect
DC	Don't Connect

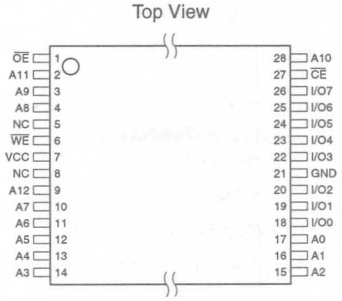
PDIP, SOIC
Top View



PLCC
Top View



TSOP
Top View



Note: PLCC package pins 1 and 17 are DON'T CONNECT.

64K (8K x 8) Low-Voltage Parallel EEPROMs with Page Write and Software Data Protection

AT28BV64B

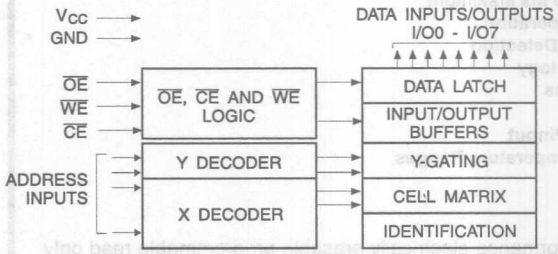
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Rev. 0299D–05/98

The AT28BV64B is accessed like a static RAM for the read or write cycle without the need for external components. The device contains a 64 byte page register to allow writing of up to 64 bytes simultaneously. During a write cycle, the addresses and 1 to 64 bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by $\overline{DATA}$ polling of I/O7. Once the end of a write cycle has been detected a new access for a read or write can begin.

Atmel's 28LV64B has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and improved data retention characteristics. A software data protection mechanism guards against inadvertent writes. The device also includes an extra 64 bytes of EEPROM for device identification or tracking.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V
Voltage on $\overline{OE}$ and A9 with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Device Operation

READ: The AT28BV64B is accessed like a static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state when either $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention in their systems.

BYTE WRITE: A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high initiates a write cycle. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Once a byte write has been started, it will automatically time itself to completion. Once a programming operation has been initiated and for the duration of t_{WC}, a read operation will effectively be a polling operation.

PAGE WRITE: The page write operation of the AT28BV64B allows 1 to 64 bytes of data to be written into the device during a single internal programming period. A page write operation is initiated in the same manner as a byte write; the first byte written can then be followed by 1 to 63 additional bytes. Each successive byte must be written within 100 µs (t_{BLC}) of the previous byte. If the t_{BLC} limit is exceeded, the AT28BV64B will cease accepting data and commence the internal programming operation. All bytes during a page write operation must reside on the same page as defined by the state of the A6 to A12 inputs. For each $\overline{WE}$ high to low transition during the page write operation, A6 to A12 must be the same.

The A0 to A5 inputs specify which bytes within the page are to be written. The bytes may be loaded in any order and may be altered within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

$\overline{DATA}$ POLLING: The AT28BV64B features $\overline{DATA}$ Polling to indicate the end of a write cycle. During a byte or page write cycle an attempted read of the last byte written will result in the complement of the written data to be presented on I/O7. Once the write cycle has been completed, true data is valid on all outputs, and the next write cycle may begin. $\overline{DATA}$ Polling may begin at anytime during the write cycle.

TOGGLE BIT: In addition to $\overline{DATA}$ Polling, the AT28BV64B provides another method for determining the end of a write cycle. During the write operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the write has completed, I/O6 will stop toggling and valid data will be read. Reading the toggle bit may begin at any time during the write cycle.

DATA PROTECTION: If precautions are not taken, inadvertent writes may occur during transitions of the host system power supply. Atmel has incorporated both hardware and software features that will protect the memory against inadvertent writes.

HARDWARE PROTECTION: Hardware features protect against inadvertent writes to the AT28BV64B in the following ways: (a) V_{CC} power-on delay—once V_{CC} has reached 1.8V (typical) the device will automatically time out 10 ms (typical) before allowing a write; (b) write inhibit—holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits write cycles; and (c) noise filter—pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a write cycle.

SOFTWARE DATA PROTECTION: A software-controlled data protection feature has been implemented on the AT28BV64B. Software data protection (SDP) helps prevent inadvertent writes from corrupting the data in the device. SDP can prevent inadvertent writes during power-up and power-down as well as any other potential periods of system instability.

The AT28BV64B can only be written using the software data protection feature. A series of three write commands to specific addresses with specific data must be presented to the device before writing in the byte or page mode. The same three write commands must begin each write operation. All software write commands must obey the page mode write timing specifications. The data in the 3-byte command sequence is not written to the device; the addresses in the command sequence can be utilized just like any other location in the device.

Any attempt to write to the device without the 3-byte sequence will start the internal write timers. No data will be written to the device; however, for the duration of t_{WC}, read operations will effectively be polling operations.

DEVICE IDENTIFICATION: An extra 64 bytes of EEPROM memory are available to the user for device identification. By raising A9 to 12V ± 0.5V and using address locations 7FC0H to 7FFFH, the additional bytes may be written to or read from in the same manner as the regular memory array.

DC and AC Operating Range

		AT28BV64B-20	AT28BV64B-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		3.3V ± 10%	3.3V ± 10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write[2]	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X[1]	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z
Chip Erase	V_{IL}	V_H[3]	V_{IL}	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to AC Programming Waveforms.
3. $V_H = 12.0V \pm 0.5V$.

DC Characteristics

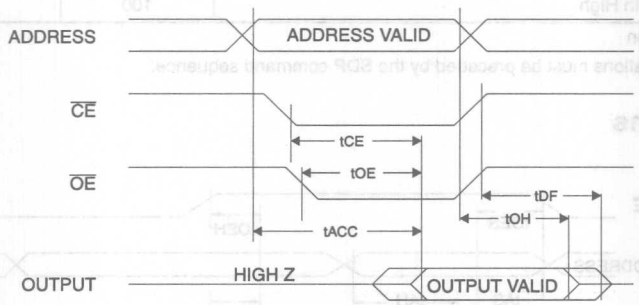
Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	$V_{IN} = 0V$ to $V_{CC} + 1V$			10	µA
I_{LO}	Output Leakage Current	$V_{I/O} = 0V$ to V_{CC}			10	µA
I_{SB}	V_{CC} Standby Current CMOS	$\overline{CE} = V_{CC} - 0.3V$ to $V_{CC} + 1V$	Com.		20	µA
			Ind.		50	µA
I_{CC}	V_{CC} Active Current	f = 5 MHz; I_{OUT} = 0 mA			15	mA
V_{IL}	Input Low Voltage				0.6	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA			0.45	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA		2.0		V

AC Read Characteristics

Symbol	Parameter	AT28BV64B-20		AT28BV64B-25		Units
		Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		200		250	ns
t_{CE}[1]	$\overline{CE}$ to Output Delay		200		250	ns
t_{OE}[2]	$\overline{OE}$ to Output Delay	0	80	0	100	ns
t_{DF}[3][4]	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	55	0	60	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		ns

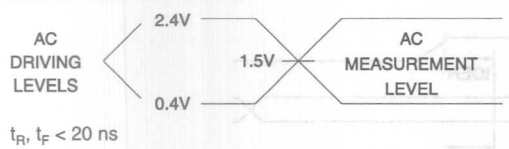
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AC Read Waveforms[1][2][3][4]



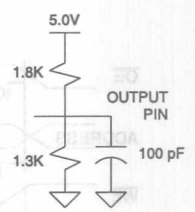
Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 20 ns

Output Test Load



Pin Capacitance

f = 1 MHz, T = 25°C[1]

Symbol	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

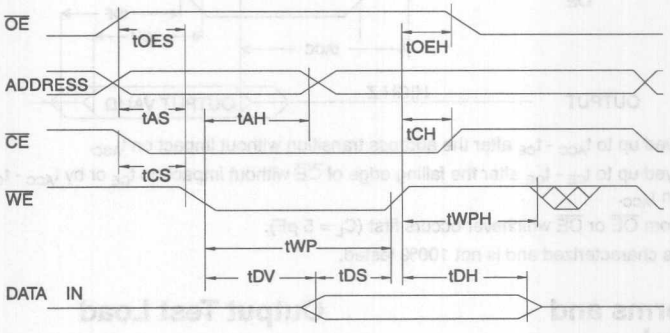
AC Write Characteristics

Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	0		ns
t_{AH}	Address Hold Time	100		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	200		ns
t_{DS}	Data Set-up Time	100		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	0		ns
t_{DV}	Time to Data Valid	NR[1]		
t_{WPH}	Write Pulse Width High	100		ns

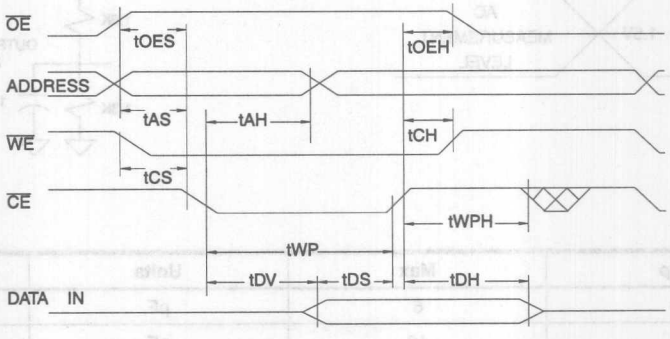
Notes: 1. NR = No Restriction
2. All byte write operations must be preceded by the SDP command sequence.

AC Write Waveforms

$\overline{WE}$ Controlled



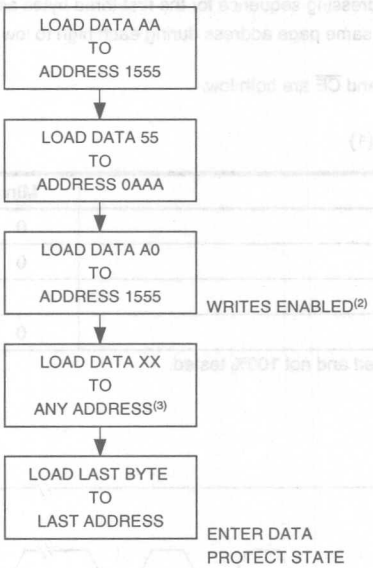
$\overline{CE}$ Controlled



Page Mode Characteristics

Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time		10	ms
t_{AS}	Address Set-up Time	0		ns
t_{AH}	Address Hold Time	100		ns
t_{DS}	Data Set-up Time	100		ns
t_{DH}	Data Hold Time	0		ns
t_{WP}	Write Pulse Width	200		ns
t_{BLC}	Byte Load Cycle Time		100	µs
t_{WPH}	Write Pulse Width High	100		ns

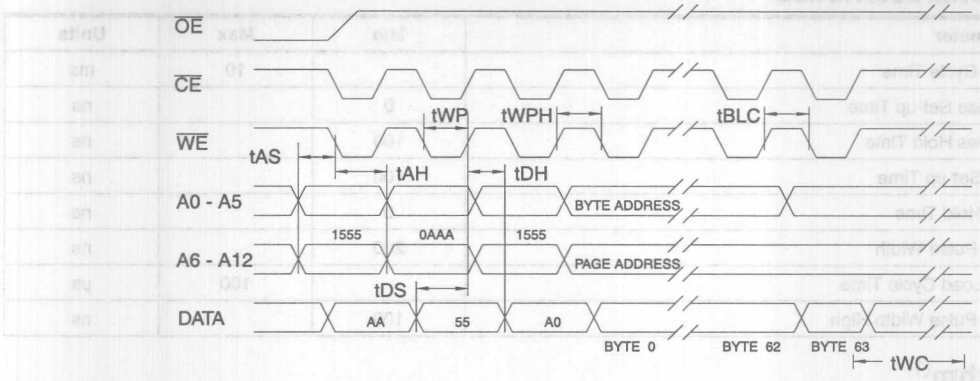
Write Algorithm(1)



Notes for software program code:

1. Data Format: I/O7 - I/O0 (Hex); Address Format: A12 - A0 (Hex).
2. Data protect state will be re-activated at the end of the write cycle.
3. 1 to 64 bytes of data are loaded.

Software Data Protection Write Cycle Waveforms[1][2][3]



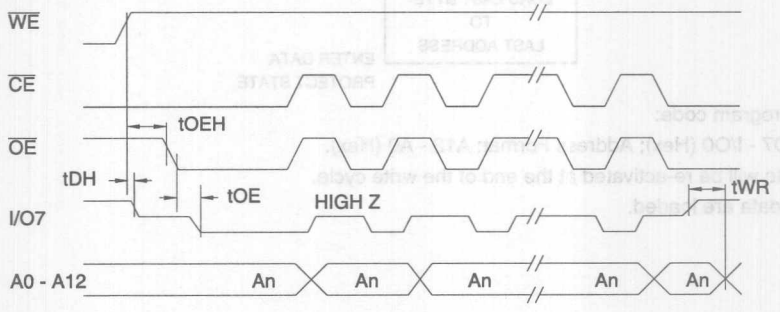
Notes: 1. A0 - A12 must conform to the addressing sequence for the first three bytes as shown above.
2. A6 through A12 must specify the same page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$) after the software code has been entered.
3. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

Data Polling Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	0			ns
t_{OEH}	$\overline{OE}$ Hold Time	0			ns
t_{OE}	$\overline{OE}$ to Output Delay[2]				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See AC Read Characteristics.

Data Polling Waveforms

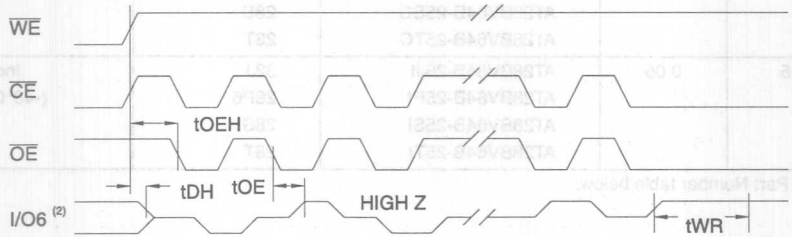


Toggle Bit Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay[2]				ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See AC Read Characteristics.

Toggle Bit Waveforms



Notes: 1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used, but the address should not vary.

Ordering Information[1]

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
200	15	0.05	AT28BV64B-20JC	32J	Commercial (0°C to 70°C)
			AT28BV64B-20PC	28P6	
			AT28BV64B-20SC	28S	
			AT28BV64B-20TC	28T	
	15	0.05	AT28BV64B-20JI	32J	Industrial (-40°C to 85°C)
			AT28BV64B-20PI	28P6	
			AT28BV64B-20SI	28S	
			AT28BV64B-20TI	28T	
250	15	0.05	AT28BV64B-25JC	32J	Commercial (0°C to 70°C)
			AT28BV64B-25PC	28P6	
			AT28BV64B-25SC	28S	
			AT28BV64B-25TC	28T	
	15	0.05	AT28BV64B-25JI	32J	Industrial (-40°C to 85°C)
			AT28BV64B-25PI	28P6	
			AT28BV64B-25SI	28S	
			AT28BV64B-25TI	28T	

Note: 1. See Valid Part Number table below.

Valid Part Numbers

The following table lists standard Atmel products that can be ordered.

Device Numbers	Speed	Package and Temperature Combinations
AT28BV64B	20	JC, JI, PC, PI, SC, SI, TC, TI
AT28BV64B	25	JC, JI, PC, PI, SC, SI, TC, TI

Package Type	
32J	32-Lead, Plastic J-Leaded Chip Carrier (PLCC)
28P6	28-Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
28S	28-Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
28T	28-Lead, Plastic Thin Small Outline Package (TSOP)

Features

- Single 3.3V ± 10% Supply
- Fast Read Access Time - 200 ns
- Automatic Page Write Operation
  - Internal Address and Data Latches for 128 Bytes
  - Internal Control Timer
- Fast Write Cycle Time
  - Page Write Cycle Time - 10 ms Maximum
  - 1 to 128-Byte Page Write Operation
- Low Power Dissipation
  - 15 mA Active Current
  - 20 µA CMOS Standby Current
- Hardware and Software Data Protection
- $\overline{\text{DATA}}$ Polling for End of Write Detection
- High Reliability CMOS Technology
  - Endurance: 100,000K Cycles
  - Data Retention: 10 Years
- JEDEC Approved Byte-Wide Pinout
- Commercial and Industrial Temperature Ranges

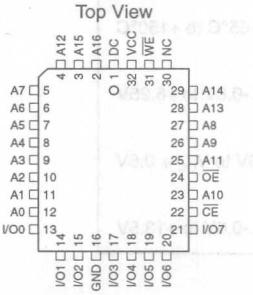
Description

The AT28LV010 is a high-performance 3-volt only Electrically Erasable and Programmable Read Only Memory. Its 1 megabit of memory is organized as 131,072 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 200 ns with power dissipation of just 54 mW. When the device is deselected, the CMOS standby current is less than 20 µA. *(continued)*

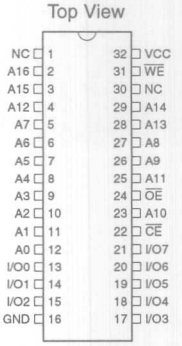
Pin Configurations

Pin Name	Function
A0 - A16	Addresses
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect
DC	Don't Connect

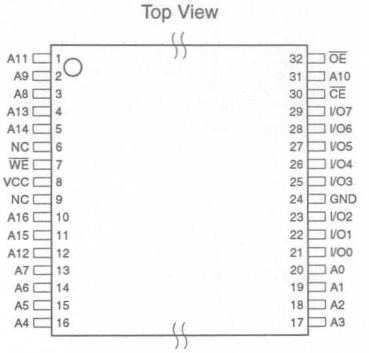
PLCC
Top View



PDIP
Top View



TSOP
Top View



1-Megabit (128K x 8) Low Voltage Paged Parallel EEPROMs

AT28LV010

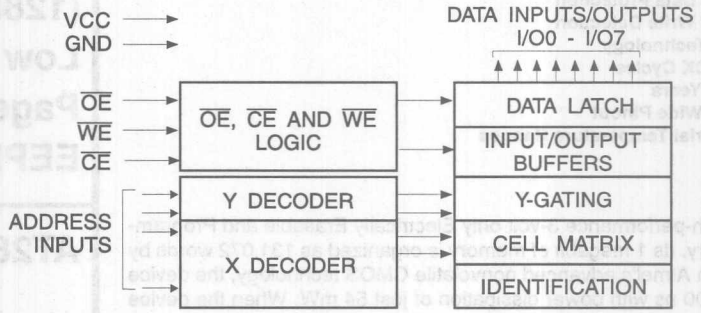
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Rev. 0395B–10/98

The AT28LV010 is accessed like a Static RAM for the read or write cycle without the need for external components. The device contains a 128-byte page register to allow writing of up to 128 bytes simultaneously. During a write cycle, the address and 1 to 128 bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by $\overline{\text{DATA}}$ polling of I/O7. Once the end of a write cycle has been detected a new access for a read or write can begin.

Atmel's 28LV010 has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and improved data retention characteristics. Software data protection is implemented to guard against inadvertent writes. The device also includes an extra 128 bytes of EEPROM for device identification or tracking.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V
Voltage on $\overline{\text{OE}}$ and A9 with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Device Operation

READ: The AT28LV010 is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state when either $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention in their system.

WRITE: The write operation of the AT28LV010 allows 1 to 128 bytes of data to be written into the device during a single internal programming period. Each write operation must be preceded by the software data protection (SDP) command sequence. This sequence is a series of three unique write command operations that enable the internal write circuitry. The command sequence and the data to be written must conform to the software protected write cycle timing. Addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs last and data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs first. Each successive byte must be written within 150 µs (t_{BLC}) of the previous byte. If the t_{BLC} limit is exceeded the AT28LV010 will cease accepting data and commence the internal programming operation. If more than one data byte is to be written during a single programming operation, they must reside on the same page as defined by the state of the A7 - A16 inputs. For each $\overline{WE}$ high to low transition during the page write operation, A7 - A16 must be the same.

The A0 to A6 inputs are used to specify which bytes within the page are to be written. The bytes may be loaded in any order and may be altered within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

$\overline{DATA}$ POLLING: The AT28LV010 features $\overline{DATA}$ Polling to indicate the end of a write cycle. During a byte or page write cycle an attempted read of the last byte written will result in the complement of the written data to be presented on I/O7. Once the write cycle has been completed, true data is valid on all outputs, and the next write cycle may begin. $\overline{DATA}$ Polling may begin at anytime during the write cycle.

TOGGLE BIT: In addition to $\overline{DATA}$ Polling the AT28LV010 provides another method for determining the end of a write cycle. During the write operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the write has completed, I/O6 will stop toggling and valid data will be read. Reading the toggle bit may begin at any time during the write cycle.

DATA PROTECTION: If precautions are not taken, inadvertent writes may occur during transitions of the host system power supply. Atmel has incorporated both hardware and software features that will protect the memory against inadvertent writes.

HARDWARE PROTECTION: Hardware features protect against inadvertent writes to the AT28LV010 in the following ways: (a) V_{CC} power-on delay—once V_{CC} has reached 2.0V (typical) the device will automatically time out 5 ms (typical) before allowing a write; (b) write inhibit—holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits write cycles; and (c) noise filter—pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a write cycle.

SOFTWARE DATA PROTECTION: The AT28LV010 incorporates the industry standard software data protection (SDP) function. Unlike standard 5-volt only EEPROM's, the AT28LV010 has SDP enabled at all times. Therefore, all write operations must be preceded by the SDP command sequence.

The data in the 3-byte command sequence is not written to the device; the addresses in the command sequence can be utilized just like any other location in the device. Any attempt to write to the device without the 3-byte sequence will start the internal timers. No data will be written to the device. However, for the duration of t_{WC}, read operations will effectively be polling operations.

DC and AC Operating Range

		AT28LV010-20	AT28LV010-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		3.3V ± 5%	3.3V ± 10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write[2]	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X[1]	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to AC Programming Waveforms.

DC Characteristics

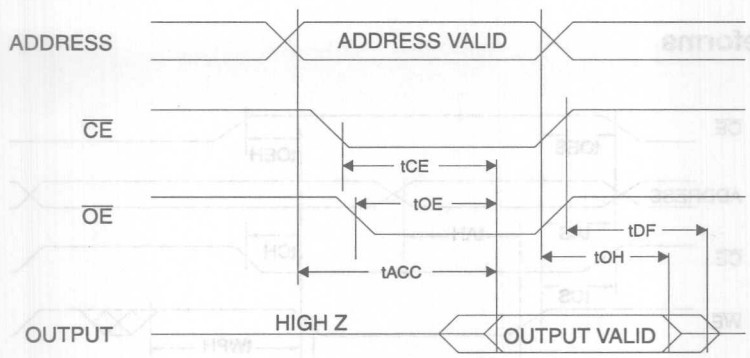
Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}			1	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}			1	µA
I_{SB}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3V to V_{CC} + 1V	Com.		20	µA
			Ind.		50	µA
I_{CC}	V_{CC} Active Current	f = 5 MHz; I_{OUT} = 0 mA; V_{CC} = 3.6V			15	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA; V_{CC} = 3.0V			0.45	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA; V_{CC} = 3.0V		2.4		V

AC Read Characteristics

Symbol	Parameter	AT28LV010-20		AT28LV010-25		Units
		Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		200		250	ns
t_{CE}[1]	$\overline{CE}$ to Output Delay		200		250	ns
t_{OE}[2]	$\overline{OE}$ to Output Delay	0	80	0	100	ns
t_{DF}[3][4]	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	55	0	60	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		ns

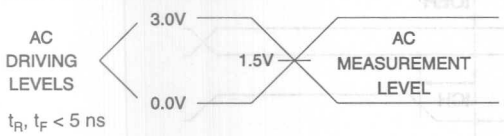
3

AC Read Waveforms[1][2][3][4]

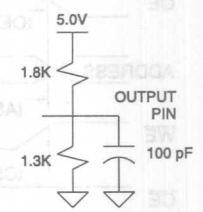


Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



Output Test Load



Pin Capacitance

f = 1 MHz, T = 25°C[1]

Symbol	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

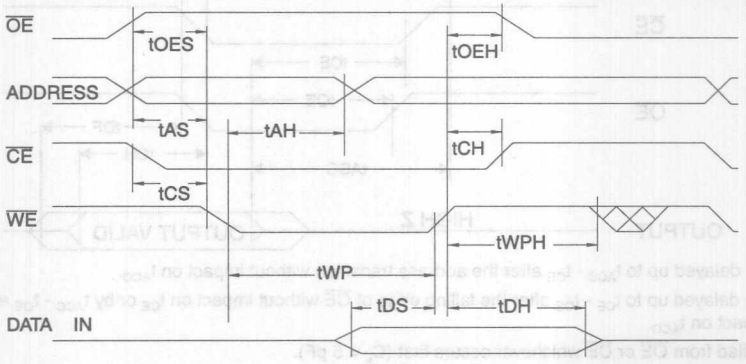
AC Write Characteristics[1]

Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	0		ns
t_{AH}	Address Hold Time	100		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	200		ns
t_{DS}	Data Set-up Time	100		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	10		ns

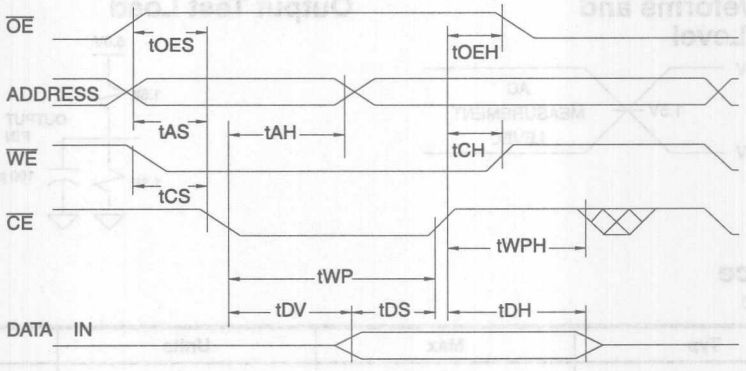
Note: 1. All write operations must be preceded by the SDP command sequence.

AC Write Waveforms

$\overline{WE}$ Controlled



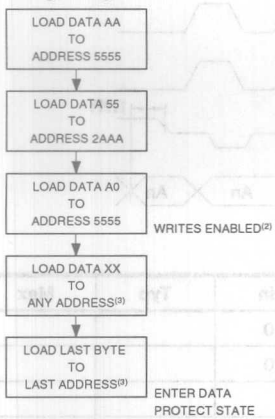
$\overline{CE}$ Controlled



Software Protected Write Characteristics

Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time		10	ms
t_{AS}	Address Set-up Time	0		ns
t_{AH}	Address Hold Time	100		ns
t_{DS}	Data Set-up Time	100		ns
t_{DH}	Data Hold Time	10		ns
t_{WP}	Write Pulse Width	200		ns
t_{BLC}	Byte Load Cycle Time		150	µs
t_{WPH}	Write Pulse Width High	100		ns

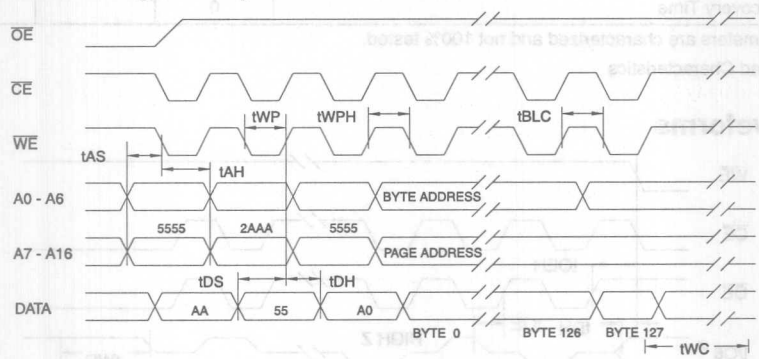
Programming Algorithm



Notes:

1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Data protect state will be re-activated at the end of program cycle.
3. 1 to 128 bytes of data are loaded.

Software Protected Program Cycle Waveforms(1)(2)(3)



Notes:

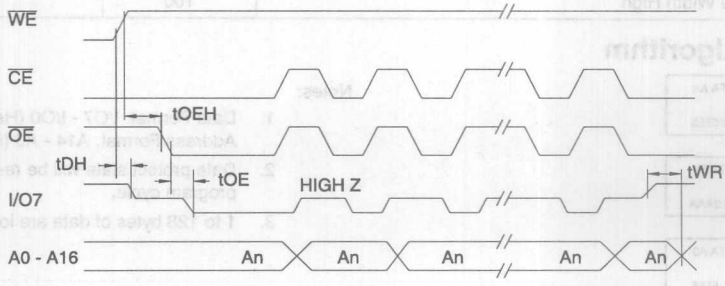
1. A0 - A14 must conform to the addressing sequence for the first three bytes as shown above.
2. After the command sequence has been issued and a page write operation follows, the page address inputs (A7 - A16) must be the same for each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
3. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

$\overline{\text{Data}}$ Polling Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay[2]				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See AC Read Characteristics

$\overline{\text{Data}}$ Polling Waveforms

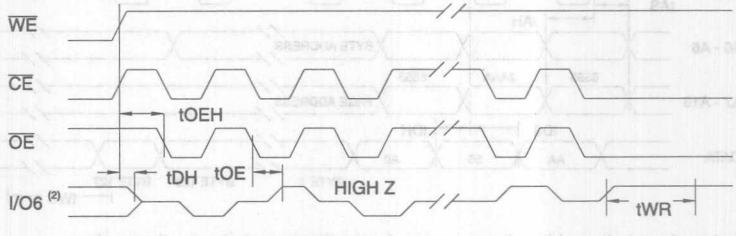


Toggle Bit Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay[2]				ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See AC Read Characteristics

Toggle Bit Waveforms



Notes: 1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

Ordering Information[1]

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
200	15	0.02	AT28LV010-20JC AT28LV010-20PC AT28LV010-20TC	32J 32P6 32T	Commercial (0° to 70°C)
	15	0.02	AT28LV010-20JI AT28LV010-20PI AT28LV010-20TI	32J 32P6 32T	Industrial (-40° to 85°C)
250	15	0.02	AT28LV010-25JC AT28LV010-25PC AT28LV010-25TC	32J 32P6 32T	Commercial (0° to 70°C)
	15	0.02	AT28LV010-25JI AT28LV010-25PI AT28LV010-25TI	32J 32P6 32T	Industrial (-40° to 85°C)

Note: 1. See Valid Part Numbers table below.

3

Valid Part Numbers

The following table lists standard Atmel products that can be ordered.

Device Numbers	Speed	Package and Temperature Combinations
AT28LV010	20	JC, JI, PC, PI, TC, TI
AT28LV010	25	JC, JI, PC, PI, TC, TI

Die Products

Reference Section: Parallel EEPROM Die Products

Package Type	
32J	32-Lead, Plastic J-Leaded Chip Carrier (PLCC)
32P6	32-Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
32T	32-Lead, Plastic Thin Small Outline Package (TSOP)

Ordering Information[1]

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
200	15	0.02	AT28LV010-20JC AT28LV010-20PC AT28LV010-20TC	32J 32P6 32T	Commercial (0° to 70°C)
	15	0.02	AT28LV010-20JI AT28LV010-20PI AT28LV010-20TI	32J 32P6 32T	Industrial (-40° to 85°C)
250	15	0.02	AT28LV010-25JC AT28LV010-25PC AT28LV010-25TC	32J 32P6 32T	Commercial (0° to 70°C)
	15	0.02	AT28LV010-25JI AT28LV010-25PI AT28LV010-25TI	32J 32P6 32T	Industrial (-40° to 85°C)

Note: 1. See Valid Part Numbers table below.

Valid Part Numbers

The following table lists standard Atmel products that can be ordered.

Device Numbers	Speed	Package and Temperature Combinations
AT28LV010	20	JC, JI, PC, PI, TC, TI
AT28LV010	25	JC, JI, PC, PI, TC, TI

Die Products

Reference Section: Parallel EEPROM Die Products

Package Type	
32J	32-Lead, Plastic J-Leaded Chip Carrier (PLCC)
32P6	32-Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
32T	32-Lead, Plastic Thin Small Outline Package (TSOP)

Features

- Fast Read Access Time - 150 ns
- Fast Byte Write - 200 µs or 1 ms
- Self-Timed Byte Write Cycle
  - Internal Address and Data Latches
  - Internal Control Timer
  - Automatic Clear Before Write
- Direct Microprocessor Control
  - $\overline{\text{DATA}}$ POLLING
- Low Power
  - 30 mA Active Current
  - 100 µA CMOS Standby Current
- High Reliability
  - Endurance: 10^4 or 10^5 Cycles
  - Data Retention: 10 Years
- 5V ± 10% Supply
- CMOS & TTL Compatible Inputs and Outputs
- JEDEC Approved Byte Wide Pinout
- Commercial and Industrial Temperature Ranges

Description

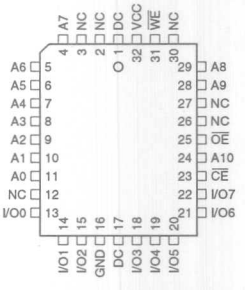
The AT28C16 is a low-power, high-performance Electrically Erasable and Programmable Read Only Memory with easy to use features. The AT28C16 is a 16K memory organized as 2,048 words by 8 bits. The device is manufactured with Atmel's reliable nonvolatile CMOS technology.

(continued)

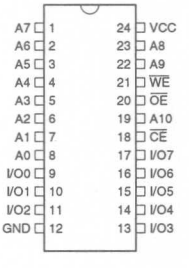
Pin Configurations

Pin Name	Function
A0 - A10	Addresses
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect
DC	Don't Connect

PLCC
Top View



PDIP, SOIC
Top View



Note: PLCC package pins 1 and 17 are DON'T CONNECT.

16K (2K x 8) Parallel EEPROMs

AT28C16

3

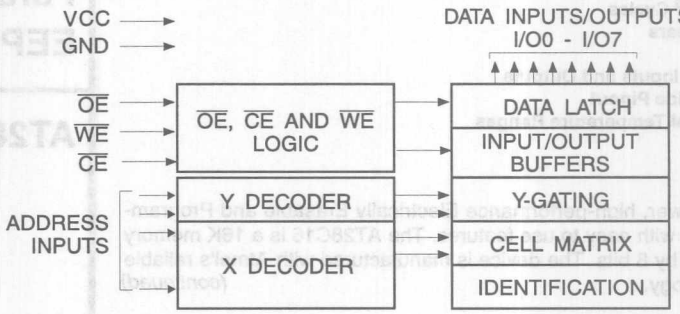
Rev. 0540B–10/98

The AT28C16 is accessed like a static RAM for the read or write cycles without the need of external components. During a byte write, the address and data are latched internally, freeing the microprocessor address and data bus for other operations. Following the initiation of a write cycle, the device will go to a busy state and automatically clear and write the latched data using an internal control timer. The end of a write cycle can be determined by $\overline{\text{DATA}}$ POLLING of I/O_7. Once the end of a write cycle has been detected, a new access for a read or a write can begin.

The CMOS technology offers fast access times of 150 ns at low power dissipation. When the chip is deselected the standby current is less than 100 µA.

Atmel's 28C16 has additional features to ensure high quality and manufacturability. The device utilizes error correction internally for extended endurance and for improved data retention characteristics. An extra 32 bytes of EEPROM are available for device identification or tracking.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V
Voltage on $\overline{\text{OE}}$ and A9 with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Device Operation

READ: The AT28C16 is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in a high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual line control gives designers increased flexibility in preventing bus contention.

BYTE WRITE: Writing data into the AT28C16 is similar to writing into a Static RAM. A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{OE}$ high and $\overline{CE}$ or $\overline{WE}$ low (respectively) initiates a byte write. The address location is latched on the last falling edge of $\overline{WE}$ (or $\overline{CE}$); the new data is latched on the first rising edge. Internally, the device performs a self-clear before write. Once a byte write has been started, it will automatically time itself to completion. Once a programming operation has been initiated and for the duration of t_{WC}, a read operation will effectively be a polling operation.

FAST BYTE WRITE: The AT28C16E offers a byte write time of 200 µs maximum. This feature allows the entire device to be rewritten in 0.4 seconds.

$\overline{\text{DATA}}$ POLLING: The AT28C16 provides $\overline{DATA}$ POLLING to signal the completion of a write cycle. During a write cycle, an attempted read of the data being written results in the complement of that data for I/O_7 (the other outputs are indeterminate). When the write cycle is finished, true data appears on all outputs.

WRITE PROTECTION: Inadvertent writes to the device are protected against in the following ways: (a) V_{CC} sense—if V_{CC} is below 3.8V (typical) the write function is inhibited; (b) V_{CC} power on delay—once V_{CC} has reached 3.8V the device will automatically time out 5 ms (typical) before allowing a byte write; and (c) write inhibit—holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits byte write cycles.

CHIP CLEAR: The contents of the entire memory of the AT28C16 may be set to the high state by the CHIP CLEAR operation. By setting $\overline{CE}$ low and $\overline{OE}$ to 12 volts, the chip is cleared when a 10 msec low pulse is applied to $\overline{WE}$.

DEVICE IDENTIFICATION: An extra 32 bytes of EEPROM memory are available to the user for device identification. By raising A9 to 12 ± 0.5V and using address locations 7E0H to 7FFH the additional bytes may be written to or read from in the same manner as the regular memory array.

3

DC and AC Operating Range

		AT28C16-15
Operating Temperature (Case)	Com.	0°C - 70°C
	Ind.	-40°C - 85°C
V_{CC} Power Supply		5V ± 10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write[2]	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X[1]	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z
Chip Erase	V_{IL}	V_H[3]	V_{IL}	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to AC Programming Waveforms.
3. $V_H = 12.0V \pm 0.5V$

DC Characteristics

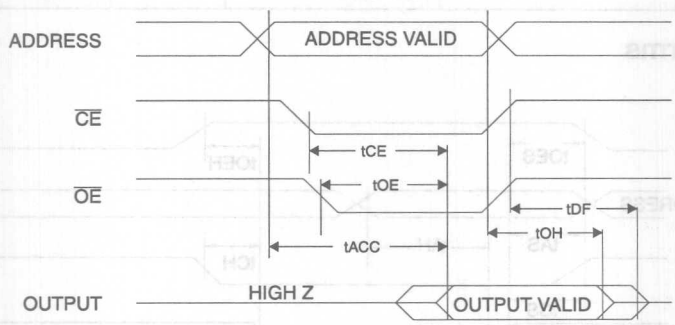
Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	$V_{IN} = 0V$ to $V_{CC} + 1V$			10	µA
I_{LO}	Output Leakage Current	$V_{I/O} = 0V$ to V_{CC}			10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE} = V_{CC} - 0.3V$ to $V_{CC} + 1.0V$			100	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE} = 2.0V$ to $V_{CC} + 1.0V$	Com.		2	mA
			Ind.		3	mA
I_{CC}	V_{CC} Active Current AC	f = 5 MHz; $I_{OUT} = 0$ mA $\overline{CE} = V_{IL}$	Com.		30	mA
			Ind.		45	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1$ mA			.4	V
V_{OH}	Output High Voltage	$I_{OH} = -400$ µA		2.4		V

AC Read Characteristics

Symbol	Parameter	AT28C16-15 Min	AT28C16-15 Max	Units
t_{ACC}	Address to Output Delay		150	ns
t_{CE}[1]	$\overline{CE}$ to Output Delay		150	ns
t_{OE}[2]	$\overline{OE}$ to Output Delay	10	70	ns
t_{DF}[3][4]	$\overline{CE}$ or $\overline{OE}$ High to Output Float	0	50	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		ns

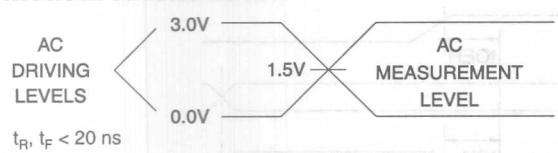
3

AC Read Waveforms[1][2][3][4]



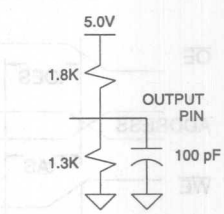
Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 20 ns

Output Test Load



Pin Capacitance

f = 1 MHz, T = 25°C[1]

Symbol	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

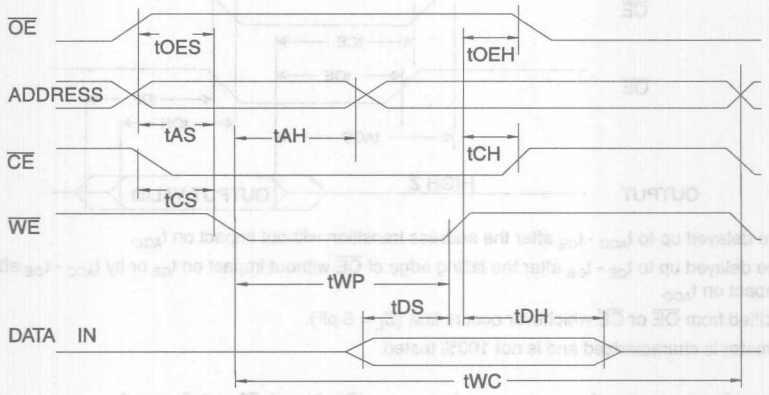
Note: 1. This parameter is characterized and is not 100% tested.

AC Write Characteristics

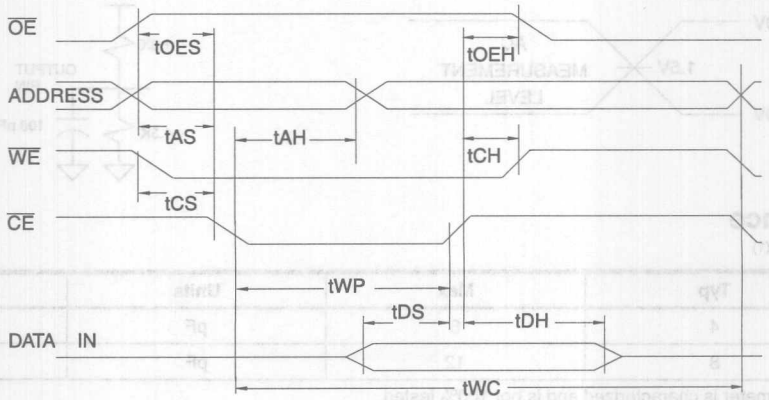
Symbol	Parameter		Min	Typ	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time		10			ns
t_{AH}	Address Hold Time		50			ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)		100		1000	ns
t_{DS}	Data Set-up Time		50			ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time		10			ns
t_{CS}, t_{CH}	$\overline{CE}$ to $\overline{WE}$ and $\overline{WE}$ to $\overline{CE}$ Set-up and Hold Time		0			ns
t_{WC}	Write Cycle Time	AT28C16		0.5	1.0	ms
		AT28C16E		100	200	µs

AC Write Waveforms

$\overline{WE}$ Controlled



$\overline{CE}$ Controlled

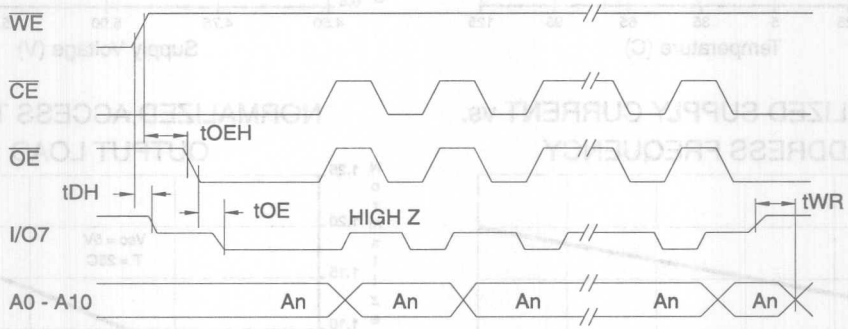


$\overline{\text{Data}}$ Polling Characteristics[1]

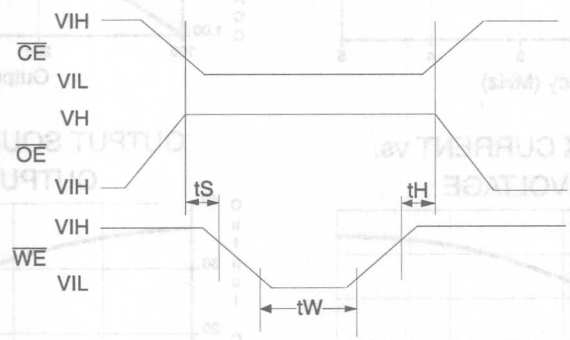
Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay[2]				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See AC Characteristics.

$\overline{\text{Data}}$ Polling Waveforms

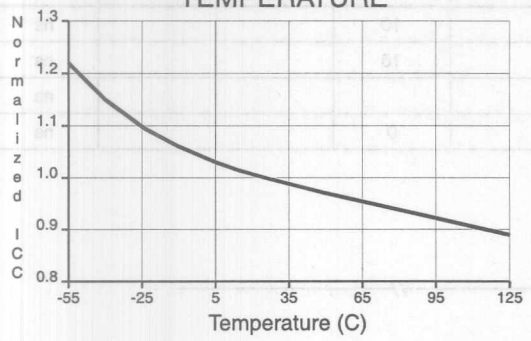


Chip Erase Waveforms

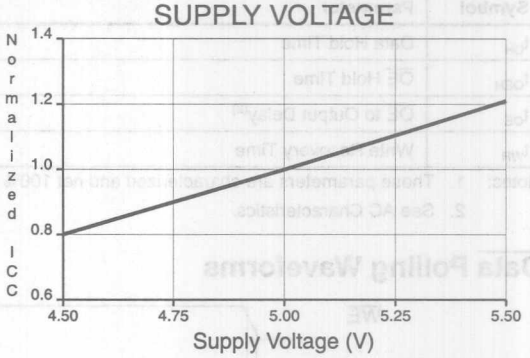


$t_S = t_H = 1$ µsec (min.)
$t_W = 10$ msec (min.)
$V_H = 12.0V \pm 0.5V$

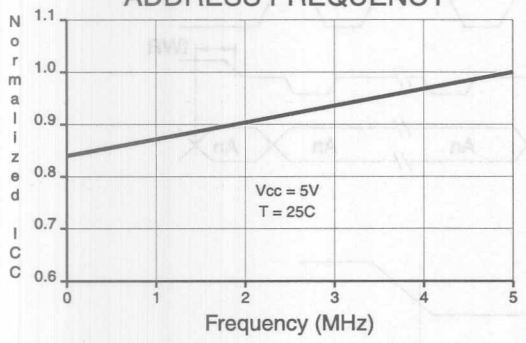
NORMALIZED SUPPLY CURRENT vs. TEMPERATURE



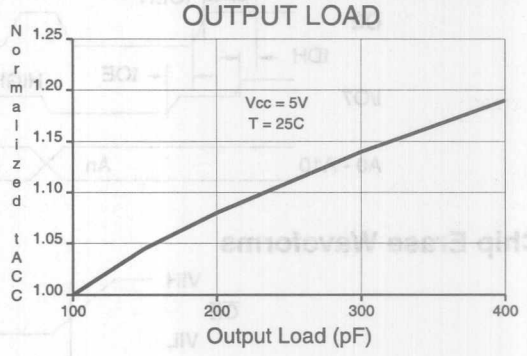
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



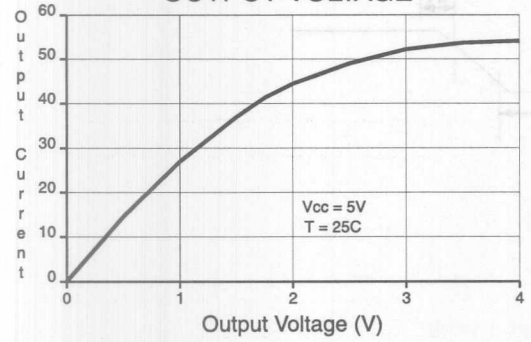
NORMALIZED SUPPLY CURRENT vs. ADDRESS FREQUENCY



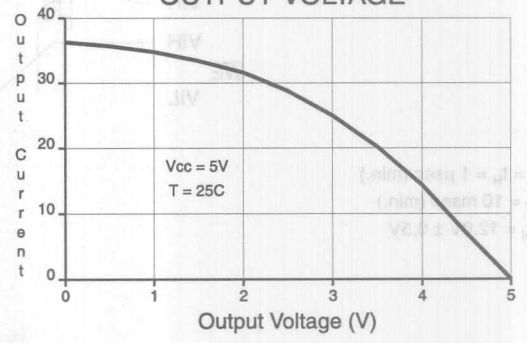
NORMALIZED ACCESS TIME vs. OUTPUT LOAD



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



Ordering Information[1]

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
150	30	0.1	AT28C16(E)-15JC AT28C16(E)-15PC AT28C16(E)-15SC	32J 24P6 24S	Commercial (0°C to 70°C)
	45	0.1	AT28C16(E)-15JI AT28C16(E)-15PI AT28C16(E)-15SI	32J 24P6 24S	Industrial (-40°C to 85°C)

Notes:
1. See Valid Part Numbers table below.
2. The 28C16 200 ns and 250 ns speed selections have been removed from valid selections table and are replaced by the faster 150 ns T_{AA} offering.
3. The 28C16 ceramic package offerings have been removed. New designs should utilize the 28C256 ceramic offerings.

3

Valid Part Numbers

The following table lists standard Atmel products that can be ordered.

Device Numbers	Speed	Package and Temperature Combinations
AT28C16	15	JC, JI, PC, PI, SC, SI
AT28C16E	15	JC, JI, PC, PI, SC, SI
AT28C16	-	W

Die Products

Reference Section: Parallel EEPROM Die Products

Package Type	
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
24P6	24 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
24S	24 Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
W	Die
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 1 ms
E	High Endurance Option: Endurance = 100K Write Cycles; Write Time = 200 µs

Ordering Information[1]

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
150	30	0.1	AT28C16(E)-15JC	32J	Commercial
			AT28C16(E)-15PC	24P6	(0°C to 70°C)
			AT28C16(E)-15SC	24S	
	40	0.1	AT28C16(E)-15JI	32J	Industrial
			AT28C16(E)-15PI	24P6	(-40°C to 85°C)
			AT28C16(E)-15SI	24S	

Notes: 1. See Valid Part Numbers table below.

2. The 28C16 200 ns and 250 ns speed selections have been removed from valid selections table and are replaced by the faster 150 ns T_{ACC} offering.

3. The 28C16 ceramic package offerings have been removed. New designs should utilize the 28C256 ceramic offerings.

Valid Part Numbers

The following table lists standard Atmel products that can be ordered.

Device Numbers	Speed	Package and Temperature Combinations
AT28C16	15	JC, JI, PC, PI, SC, SI
AT28C16E	15	JC, JI, PC, PI, SC, SI
AT28C16	-	W

Die Products

Reference Section: Parallel EEPROM Die Products

Package Type	
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
24P6	24 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
24S	24 Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
W	Die
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 1 ms
E	High Endurance Option: Endurance = 100K Write Cycles; Write Time = 200 µs

Features

- Ideal Rewritable Attribute Memory
- Simple Write Operation
  - Self-Timed Byte Writes
  - On-chip Address and Data Latch for SRAM-like Write Operation
  - Fast Write Cycle Time - 1 ms
  - 5-Volt Only Nonvolatile Writes
- End of Write Detection
  - RDY/$\overline{\text{BUSY}}$ Output
  - $\overline{\text{DATA}}$ Polling
- High Reliability
  - Endurance: 100,000 Write Cycles
  - Data Retention: 10 Years Minimum
- Single 5-Volt Supply for Read and Write
- Very Low Power
  - 30 mA Active Current
  - 100 µA Standby Current

16K (2K x 8) PCMCIA Nonvolatile Attribute Memory

AT28C16-T

3

Description

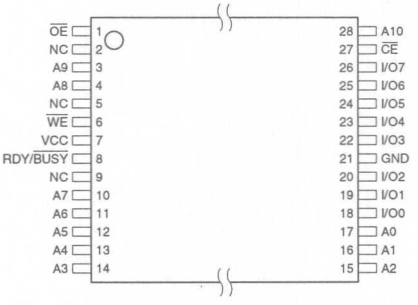
The AT28C16-T is the ideal nonvolatile attribute memory: it is a low power, 5-volt only byte writable nonvolatile memory (EEPROM). Standby current is typically less than 100 µA. The AT28C16-T is written like a Static RAM, eliminating complex programming algorithms. The fast write cycle times of 1 ms, allow quick card reconfiguration in-system. Data retention is specified as 10 years minimum, precluding the necessity for batteries. Three access times have been specified to allow for varying layers of buffering between the memory and the PCMCIA interface.

The AT28C16-T is accessed like a Static RAM for read and write operations. During a byte write, the address and data are latched internally. Following the initiation of a write cycle, the device will go to a busy state and automatically write the latched data using an internal control timer. The device provides two methods for detecting the end of a write cycle; the RDY/$\overline{\text{BUSY}}$ output and $\overline{\text{DATA}}$ POLLING of I/O_7.

Pin Configurations

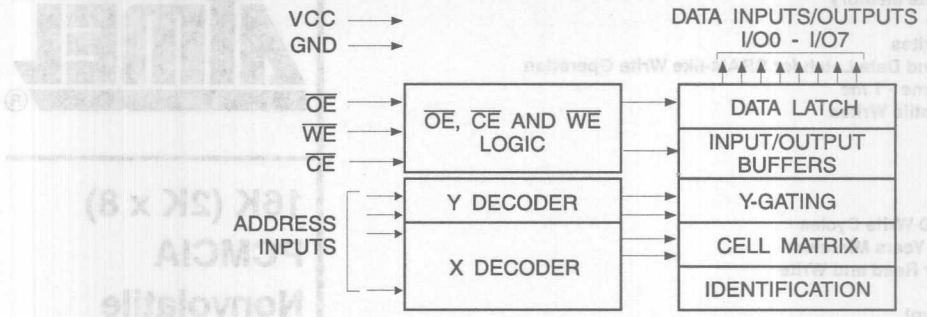
Pin Name	Function
A0 - A10	Addresses
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
RDY/$\overline{\text{BUSY}}$	Ready/Busy Output
NC	No Connect

TSOP
Top View



Rev. 0258C–10/98

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +125°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V
Voltage on $\overline{OE}$ and A9 with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Device Operation

READ: The AT28C16-T is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in a high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers increased flexibility in preventing bus contention.

BYTE WRITE: Writing data into the AT28C16-T is similar to writing into a Static RAM. A low pulse on $\overline{WE}$ or $\overline{CE}$ input with $\overline{OE}$ high and $\overline{CE}$ or $\overline{WE}$ low (respectively) initiates a byte write. The address is latched on the falling edge of $\overline{WE}$ or $\overline{CE}$ (whichever occurs last) and the data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$ (whichever occurs first). Once a byte write is started it will automatically time itself to completion. For the AT28C16-T the write cycle time is 1 ms maximum. Once a programming operation has been initiated and for the duration of t_{WC}, a read operation will effectively be a polling operation.

READY/$\overline{BUSY}$: Pin 1 is an open drain READY/$\overline{BUSY}$ output that indicates the current status of the self-timed internal write cycle. READY/$\overline{BUSY}$ is actively pulled low during the write cycle and is released at the completion of the write. The open drain output allows OR-tying of several devices to a common interrupt input.

$\overline{DATA}$ POLLING: The AT28C16-T also provides $\overline{DATA}$ polling to signal the completion of a write cycle. During a write cycle, an attempted read of the data being written results in the complement of that data for I/O_7 (the other outputs are indeterminate). When the write cycle is finished, true data appears on all outputs.

WRITE PROTECTION: Inadvertent writes to the device are protected against in the following ways: (a) V_{CC} sense—if V_{CC} is below 3.8V (typical) the write function is inhibited; (b) V_{CC} power on delay—once V_{CC} has reached 3.8V the device will automatically time out 5 ms (typical) before allowing a byte write; and (c) write inhibit—holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits byte write cycles.

CHIP CLEAR: The contents of the entire memory of the AT28C16-T may be set to the high state by the Chip Clear operation. By setting $\overline{CE}$ low and $\overline{OE}$ to 12V, the chip is cleared when a 10 ms low pulse is applied to $\overline{WE}$.

DEVICE IDENTIFICATION: An extra 32 bytes of EEPROM memory are available to the user for device identification. By raising A9 to 12V (± 0.5V) and using address locations 7E0H to 7FFH the additional bytes may be written to or read from in the same manner as the regular memory array.

DC and AC Operating Range

		AT28C16-15T
Operating Temperature (Case)	Com.	0°C - 70°C
	Ind.	-40°C - 85°C
V_{CC} Power Supply		5V ± 10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write[2]	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X[1]	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z
Chip Erase	V_{IL}	V_H[3]	V_{IL}	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to AC Programming Waveforms.
3. V_H = 12.0V ± 0.5V.

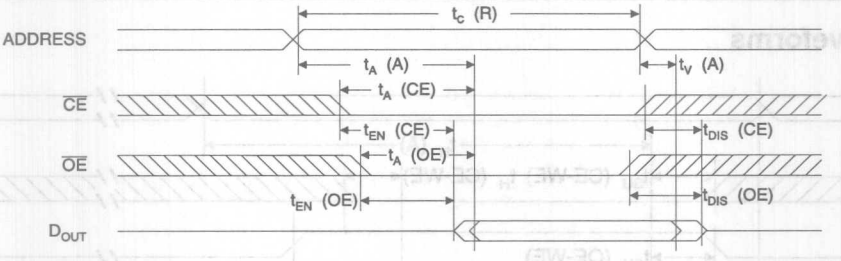
DC Characteristics

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC} + 1V			10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}			10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3V to V_{CC} + 1.0V			100	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V to V_{CC} + 1.0V	Com.		2	mA
			Ind.		3	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz; I_{OUT} = 0 mA	Com.		30	mA
			Ind.		45	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA		2.4		V

AC Read Characteristics

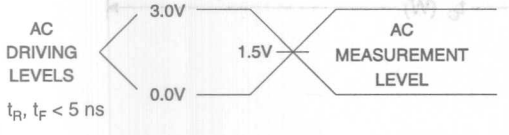
PCMCIA Symbol	Atmel Symbol	Parameter	AT28C16-15T		Units
			Min	Max	
t_C (R)	t_{RC}	Read Cycle Time	150		ns
t_A (A)	t_{ACC}	Address Access Time		150	ns
t_A (CE)	t_{CE}[1]	$\overline{CE}$ Access Time		150	ns
t_A (OE)	t_{OE}[2]	$\overline{OE}$ Access Time	0	75	ns
t_{EN} (CE)	t_{LZ}[4]	Output Enable Time From $\overline{CE}$	0		ns
t_{EN} (OE)	t_{OLZ}[4]	Output Enable Time From $\overline{OE}$	0		ns
t_V (A)	t_{OH}	Output Hold Time	0		ns
t_{DIS} (CE)	t_{DF}[3][4]	Output Disable Time From $\overline{CE}$	0	50	ns
t_{DIS} (OE)	t_{DF}[3][4]	Output Disable Time From $\overline{OE}$	0	50	ns

AC Read Waveforms[1][2][3][4]

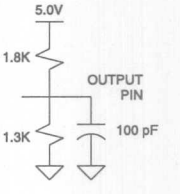


Notes:
1. $\overline{CE}$ may be delayed up to t_{ACC} - t_{CE} after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE} or by t_{ACC} - t_{OE} after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



Output Test Load



Pin Capacitance

f = 1 MHz, T = 25°C[1]

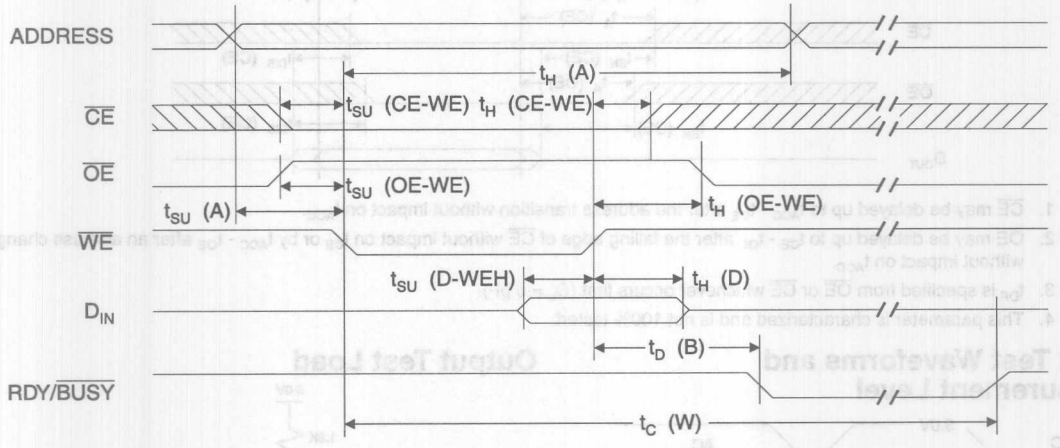
Symbol	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

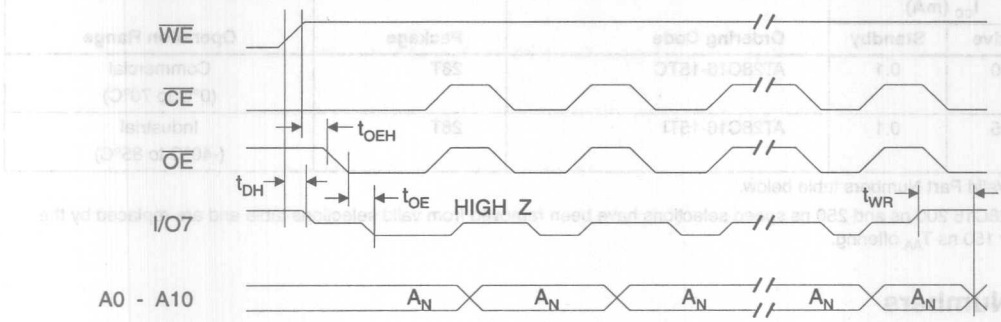
AC Write Characteristics

PCMCIA Symbol	Atmel Symbol	Parameter	Min	Max	Units
t_{SU} (A)	t_{AS}	Address Setup Time	10		ns
t_{SU} (OE-WE)	t_{OES}	Output Disable Time To $\overline{WE}$	10		ns
t_{SU} (CE-WE)	t_{CS}	Chip Enable Time To $\overline{WE}$	0		ns
t_W (WE)	t_{WP}	Write Enable Pulse Width	100	1000	ns
t_{SU} (D-WEH)	t_{DS}	Data Setup To $\overline{WE}$ High	50		ns
t_H (A)	t_{AH}	Address Hold Time From $\overline{WE}$	50		ns
t_H (D)	t_{DH}	Data Hold Time From $\overline{WE}$ High	10		ns
t_H (OE-WE)	t_{OEH}	Output Enable Hold Time From $\overline{WE}$ High	10		ns
t_H (CE-WE)	t_{CH}	Chip Enable Hold Time From $\overline{WE}$ High	0		ns
t_D (B)	t_{DB}	Delay From $\overline{WE}$ High To $\overline{BUSY}$ Asserted		50	ns
t_C (W)	t_{WC}	Write Cycle Time		1	ms

AC Write Waveforms

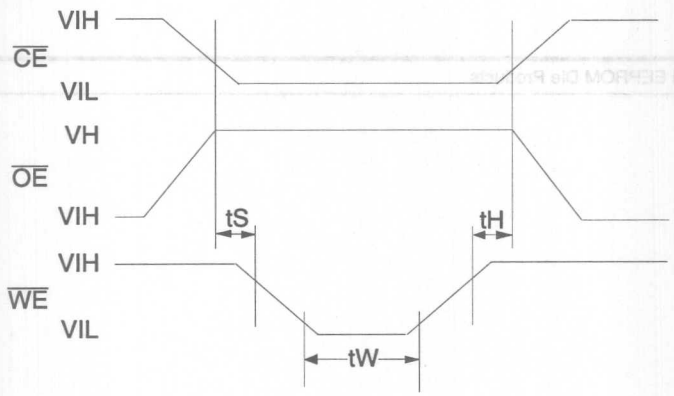


$\overline{\text{Data}}$ Polling Waveforms



Note: 1. Data Polling AC Timing Characteristics are the same as the AC Read Characteristics.

Chip Erase Waveforms



$t_S = t_H = 1\ \mu sec$ (min.)
$t_W = 10$ msec (min.)
$V_H = 12.0 \pm 0.5V$

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
150	30	0.1	AT28C16-15TC	28T	Commercial (0°C to 70°C)
	45	0.1	AT28C16-15TI	28T	Industrial (-40°C to 85°C)

Notes: 1. See Valid Part Numbers table below.

2. The 28C16 200 ns and 250 ns speed selections have been removed from valid selections table and are replaced by the faster 150 ns T_{AA} offering.

Valid Part Numbers

The following table lists standard Atmel products that can be ordered.

Device Numbers	Speed	Package and Temperature Combinations
AT28C16	15	TC, TI

Die Products

Reference Section: Parallel EEPROM Die Products

Package Type	
28T	28-Lead, Plastic Thin Small Outline Package (TSOP)

Features

- Fast Read Access Time - 150 ns
- Fast Byte Write - 200 µs or 1 ms
- Self-Timed Byte Write Cycle
  - Internal Address and Data Latches
  - Internal Control Timer
  - Automatic Clear Before Write
- Direct Microprocessor Control
  - $\overline{\text{DATA}}$ POLLING
  - READY/$\overline{\text{BUSY}}$ Open Drain Output
- Low Power
  - 30 mA Active Current
  - 100 µa CMOS Standby Current
- High Reliability
  - Endurance: 10^4 or 10^5 Cycles
  - Data Retention: 10 Years
- 5V ± 10% Supply
- CMOS & TTL Compatible Inputs and Outputs
- JEDEC Approved Byte Wide Pinout
- Commercial and Industrial Temperature Ranges

Description

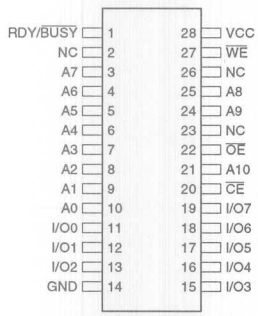
The AT28C17 is a low-power, high-performance Electrically Erasable and Programmable Read Only Memory with easy to use features. The AT28C17 is a 16K memory organized as 2,048 words by 8 bits. The device is manufactured with Atmel's reliable nonvolatile CMOS technology.

(continued)

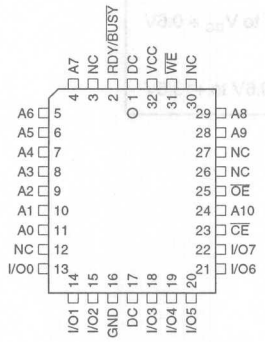
Pin Configurations

Pin Name	Function
A0 - A10	Addresses
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
RDY/$\overline{\text{BUSY}}$	Ready/Busy Output
NC	No Connect
DC	Don't Connect

PDIP, SOIC
Top View



PLCC
Top View



Note: PLCC package pins 1 and 17 are DON'T CONNECT.

16K (2K x 8) Parallel EEPROMs

AT28C17

3

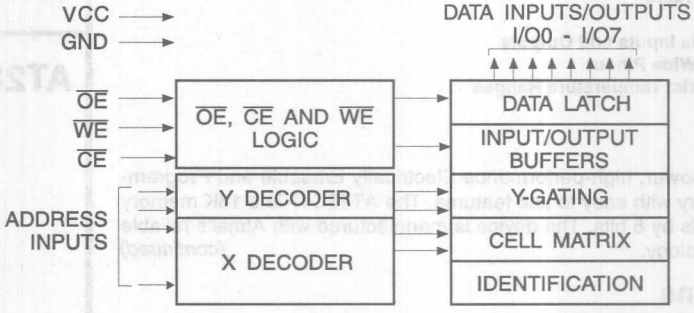
Rev. 0541B–10/98

The AT28C17 is accessed like a static RAM for the read or write cycles without the need of external components. During a byte write, the address and data are latched internally, freeing the microprocessor address and data bus for other operations. Following the initiation of a write cycle, the device will go to a busy state and automatically clear and write the latched data using an internal control timer. The device includes two methods for detecting the end of a write cycle, level detection of RDY/$\overline{BUSY}$ and $\overline{DATA}$ POLLING of I/O_7. Once the end of a write cycle has been detected, a new access for a read or a write can begin.

The CMOS technology offers fast access times of 150 ns at low power dissipation. When the chip is deselected the standby current is less than 100 µA.

Atmel's 28C17 has additional features to ensure high quality and manufacturability. The device utilizes error correction internally for extended endurance and for improved data retention characteristics. An extra 32 bytes of EEPROM are available for device identification or tracking.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V
Voltage on $\overline{OE}$ and A9 with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Device Operation

READ: The AT28C17 is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in a high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual line control gives designers increased flexibility in preventing bus contention.

BYTE WRITE: Writing data into the AT28C17 is similar to writing into a Static RAM. A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{OE}$ high and $\overline{CE}$ or $\overline{WE}$ low (respectively) initiates a byte write. The address location is latched on the last falling edge of $\overline{WE}$ (or $\overline{CE}$); the new data is latched on the first rising edge. Internally, the device performs a self-clear before write. Once a byte write has been started, it will automatically time itself to completion. Once a programming operation has been initiated and for the duration of t_{WC}, a read operation will effectively be a polling operation.

FAST BYTE WRITE: The AT28C17E offers a byte write time of 200 µs maximum. This feature allows the entire device to be rewritten in 0.4 seconds.

READY/$\overline{BUSY}$: Pin 1 is an open drain READY/$\overline{BUSY}$ output that can be used to detect the end of a write cycle. RDY/$\overline{BUSY}$ is actively pulled low during the write cycle and is released at the completion of the write. The open drain connection allows for OR-tying of several devices to the same RDY/$\overline{BUSY}$ line.

$\overline{DATA}$ POLLING: The AT28C17 provides $\overline{DATA}$ POLLING to signal the completion of a write cycle. During a write cycle, an attempted read of the data being written results in the complement of that data for I/O_7 (the other outputs are indeterminate). When the write cycle is finished, true data appears on all outputs.

WRITE PROTECTION: Inadvertent writes to the device are protected against in the following ways: (a) V_{CC} sense—if V_{CC} is below 3.8V (typical) the write function is inhibited; (b) V_{CC} power on delay once V_{CC} has reached 3.8V the device will automatically time out 5 ms (typical) before allowing a byte write; and (c) write inhibit—holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits byte write cycles.

CHIP CLEAR: The contents of the entire memory of the AT28C17 may be set to the high state by the CHIP CLEAR operation. By setting $\overline{CE}$ low and $\overline{OE}$ to 12 volts, the chip is cleared when a 10 msec low pulse is applied to $\overline{WE}$.

DEVICE IDENTIFICATION: An extra 32 bytes of EEPROM memory are available to the user for device identification. By raising A9 to 12 ± 0.5V and using address locations 7E0H to 7FFH the additional bytes may be written to or read from in the same manner as the regular memory array.

DC and AC Operating Range

		AT28C17-15
Operating Temperature (Case)	Com.	0°C - 70°C
	Ind.	-40°C - 85°C
V_{CC} Power Supply		5V ± 10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write(2)	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X(1)	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z
Chip Erase	V_{IL}	V_H(3)	V_{IL}	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to AC Programming Waveforms.
3. $V_H = 12.0V \pm 0.5V$.

DC Characteristics

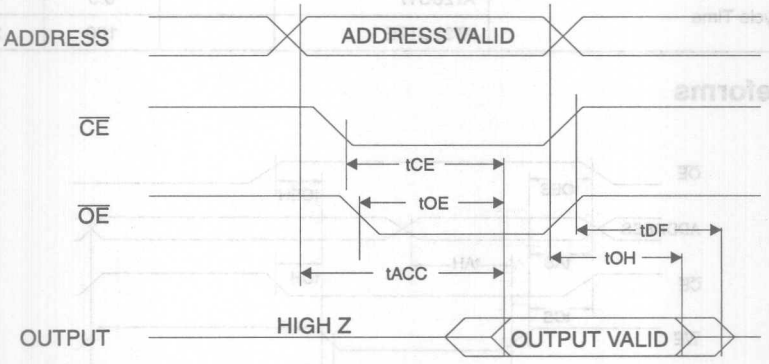
Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	$V_{IN} = 0V$ to $V_{CC} + 1V$			10	µA
I_{LO}	Output Leakage Current	$V_{I/O} = 0V$ to V_{CC}			10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE} = V_{CC} - 0.3V$ to $V_{CC} + 1.0V$			100	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE} = 2.0V$ to $V_{CC} + 1.0V$	Com.		2	mA
			Ind.		3	mA
I_{CC}	V_{CC} Active Current AC	f = 5 MHz; $I_{OUT} = 0$ mA $\overline{CE} = V_{IL}$	Com.		30	mA
			Ind.		45	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1$ mA = 4.0 for RDY/$\overline{BUSY}$			.4	V
V_{OH}	Output High Voltage	$I_{OH} = -400$ µA		2.4		V

AC Read Characteristics

Symbol	Parameter	AT28C17-15		Units
		Min	Max	
t_{ACC}	Address to Output Delay		150	ns
t_{CE}[1]	$\overline{CE}$ to Output Delay		150	ns
t_{OE}[2]	$\overline{OE}$ to Output Delay	10	70	ns
t_{DF}[3][4]	$\overline{CE}$ or $\overline{OE}$ High to Output Float	0	50	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		ns

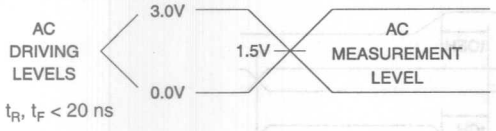
3

AC Read Waveforms[1][2][3][4]

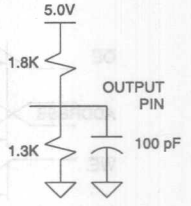


Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



Output Test Load



Pin Capacitance

f = 1 MHz, T = 25°C[1]

Symbol	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

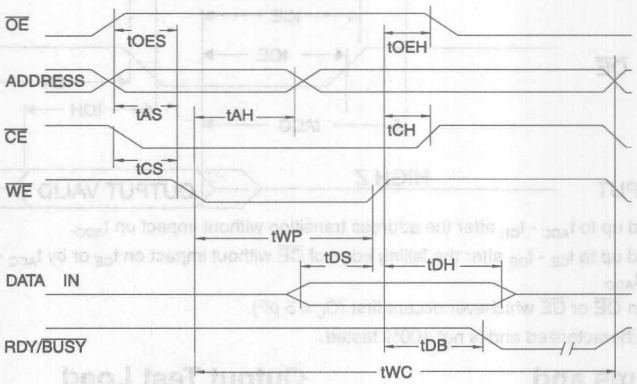
Note: 1. This parameter is characterized and is not 100% tested.

AC Write Characteristics

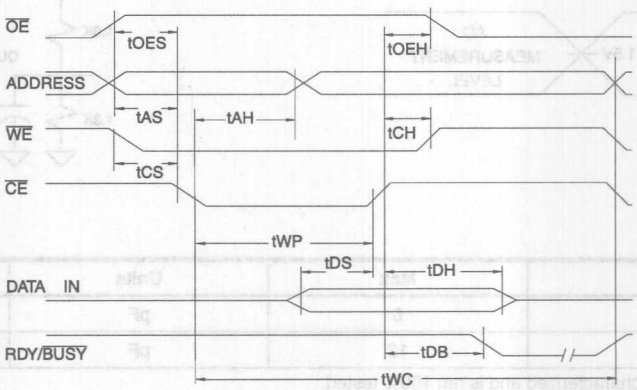
Symbol	Parameter		Min	Typ	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time		10			ns
t_{AH}	Address Hold Time		50			ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)		100		1000	ns
t_{DS}	Data Set-up Time		50			ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time		10			ns
t_{CS}, t_{CH}	$\overline{CE}$ to $\overline{WE}$ and $\overline{WE}$ to $\overline{CE}$ Set-up and Hold Time		0			ns
t_{DB}	Time to Device Busy				50	ns
t_{WC}	Write Cycle Time	AT28C17		0.5	1.0	ms
		AT28C17E		100	200	µs

AC Write Waveforms

$\overline{WE}$ Controlled



$\overline{CE}$ Controlled

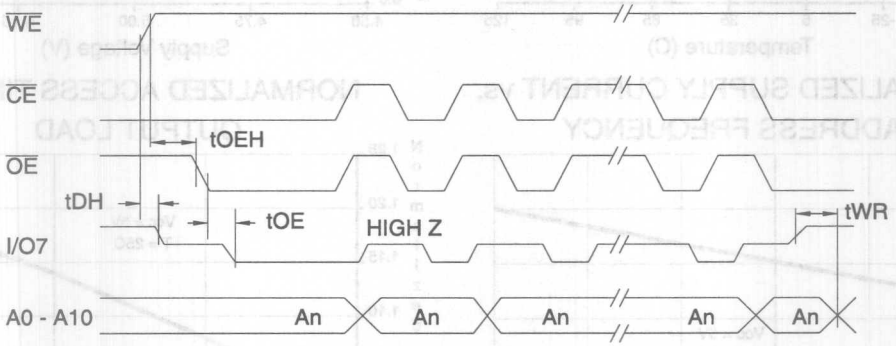


$\overline{\text{Data}}$ Polling Characteristics[1]

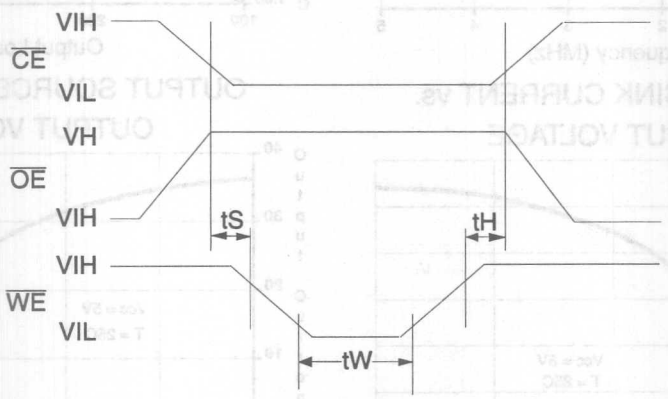
Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay[2]				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See AC Read Characteristics.

$\overline{\text{Data}}$ Polling Waveforms

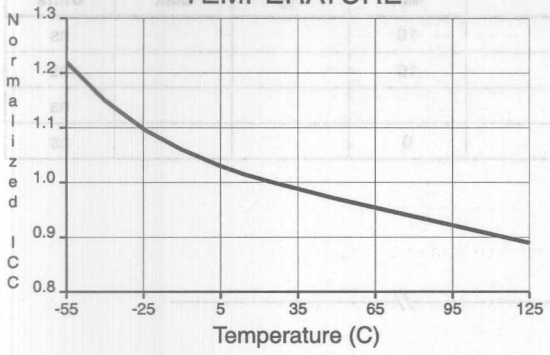


Chip Erase Waveforms

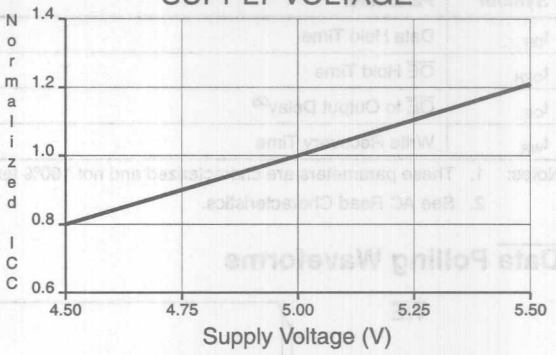


$t_S = t_H = 1$ µsec (min.)
$t_W = 10$ msec (min.)
$V_H = 12.0 \pm 0.5V$

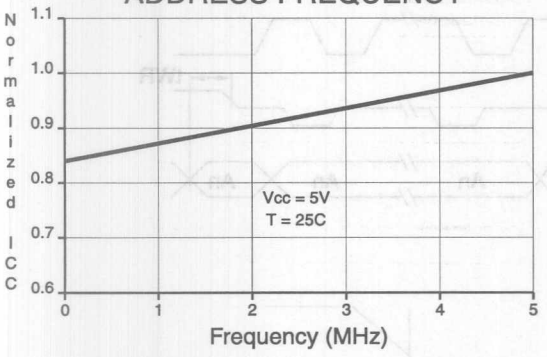
NORMALIZED SUPPLY CURRENT vs. TEMPERATURE



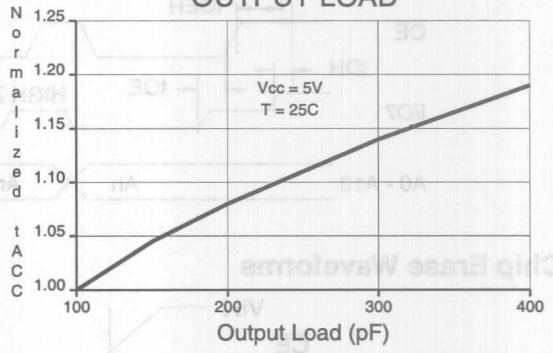
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



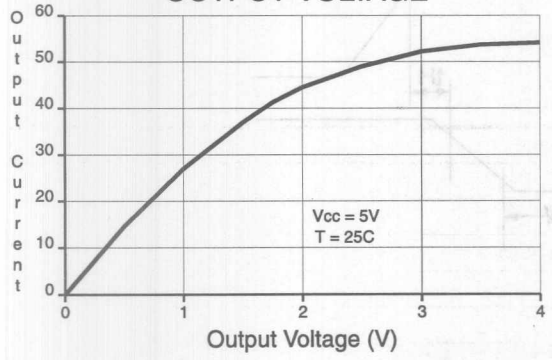
NORMALIZED SUPPLY CURRENT vs. ADDRESS FREQUENCY



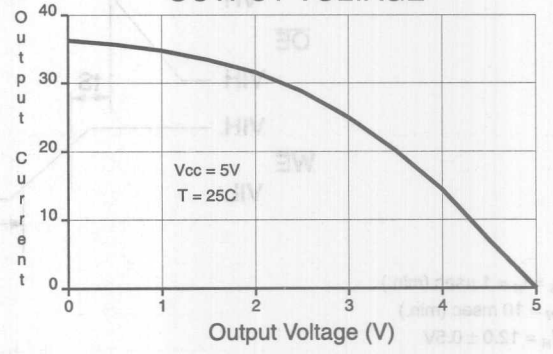
NORMALIZED ACCESS TIME vs. OUTPUT LOAD



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



Ordering Information[1]

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
150	30	0.1	AT28C17(E)-15JC AT28C17(E)-15PC AT28C17(E)-15SC	32J 28P6 28S	Commercial (0°C to 70°C)
	45	0.1	AT28C17(E)-15JI AT28C17(E)-15PI AT28C17(E)-15SI	32J 28P6 28S	Industrial (-40°C to 85°C)

Notes:
1. See Valid Part Numbers table below.
2. The 28C17 200 ns and 250 ns speed selections have been removed from valid selections table and are replaced by the faster 150 ns T_{AA} offering.
3. The 28C17 ceramic and LCC package offerings have been removed. New designs should utilize the 28C256 ceramic offerings.

3

Valid Part Numbers

The following table lists standard Atmel products that can be ordered.

Device Numbers	Speed	Package and Temperature Combinations
AT28C17	15	JC, JI, PC, PI, SC, SI
AT28C17E	15	JC, JI, PC, PI, SC, SI
AT28C17	-	W

Die Products

Reference Section: Parallel EEPROM Die Products

Package Type	
32J	32-Lead, Plastic J-Leaded Chip Carrier (PLCC)
28P6	28-Lead, 0.600" Wide, Plastic Dull Inline Package (PDIP)
28S	28-Lead, 0.300" Wide, Plastic Gull Wing, Small Outline (SOIC)
W	Die
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 1 ms
E	High Endurance Option: Endurance = 100K Write Cycles; Write Time = 200 µs

Ordering Information[1]

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
150	30	0.1	AT28C17(E)-15JC AT28C17(E)-15PC AT28C17(E)-15SC	32J 28P6 28S	Commercial (0°C to 70°C)
	40	0.1	AT28C17(E)-15JI AT28C17(E)-15PI AT28C17(E)-15SI	32J 28P6 28S	Industrial (-40°C to 85°C)

Notes: 1. See Valid Part Numbers table below.

2. The 28C17 200 ns and 250 ns speed selections have been removed from valid selections table and are replaced by the faster 120 ns T_{AA} offering.

3. The 28C17 ceramic and LCC packages offerings have been removed. New designs should utilize the 28C256 ceramic offerings.

Valid Part Numbers

The following table lists standard Atmel products that can be ordered.

Device Numbers	Speed	Package and Temperature Combinations
AT28C17	15	JC, JI, PC, PI, SC, SI
AT28C17E	15	JC, JI, PC, PI, SC, SI
AT28C17	-	W

Die Products

Reference Section: Parallel EEPROM Die Products

Package Type	
32J	32-Lead, Plastic J-Leaded Chip Carrier (PLCC)
28P6	28-Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
28S	28-Lead, 0.300" Wide, Plastic Gull Wing, Small Outline (SOIC)
W	Die

Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 1 ms
E	High Endurance Option: Endurance = 100K Write Cycles; Write Time = 200 µs

Features

- Fast Read Access Time - 120 ns
- Fast Byte Write - 200 µs or 1 ms
- Self-Timed Byte Write Cycle
  - Internal Address and Data Latches
  - Internal Control Timer
  - Automatic Clear Before Write
- Direct Microprocessor Control
  - READY/$\overline{\text{BUSY}}$ Open Drain Output
  - $\overline{\text{DATA}}$ Polling
- Low Power
  - 30 mA Active Current
  - 100 µA CMOS Standby Current
- High Reliability
  - Endurance: 10^4 or 10^5 Cycles
  - Data Retention: 10 Years
- 5V ± 10% Supply
- CMOS and TTL Compatible Inputs and Outputs
- JEDEC Approved Byte-Wide Pinout
- Commercial and Industrial Temperature Ranges

Description

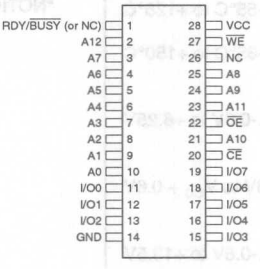
The AT28C64 is a low-power, high-performance 8,192 words by 8-bit nonvolatile Electrically Erasable and Programmable Read Only Memory with popular, easy to use features. The device is manufactured with Atmel's reliable nonvolatile technology.

(continued)

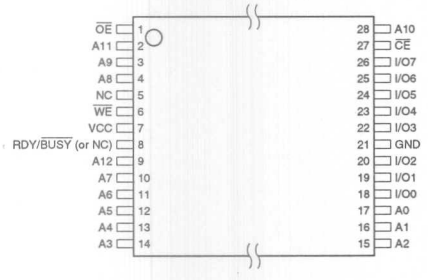
Pin Configurations

Pin Name	Function
A0 - A12	Addresses
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
RDY/$\overline{\text{BUSY}}$	Ready/$\overline{\text{Busy}}$ Output
NC	No Connect
DC	Don't Connect

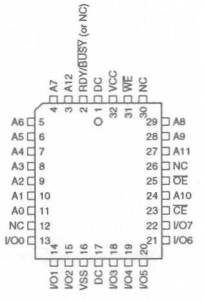
PDIP, SOIC
Top View



TSOP
Top View



LCC, PLCC
Top View



Note: PLCC package pins 1 and 17 are DON'T CONNECT.

64K (8K x 8) Parallel EEPROMs

3

AT28C64
AT28C64X

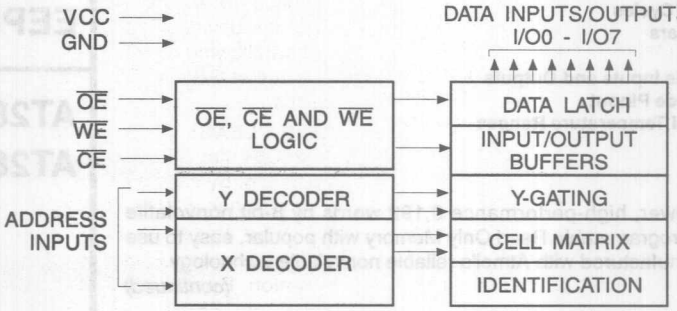
Rev. 0001G–10/98

The AT28C64 is accessed like a Static RAM for the read or write cycles without the need for external components. During a byte write, the address and data are latched internally, freeing the microprocessor address and data bus for other operations. Following the initiation of a write cycle, the device will go to a busy state and automatically clear and write the latched data using an internal control timer. The device includes two methods for detecting the end of a write cycle, level detection of RDY/$\overline{BUSY}$ (unless pin 1 is N.C.) and $\overline{DATA}$ POLLING of I/O_7. Once the end of a write cycle has been detected, a new access for a read or write can begin.

The CMOS technology offers fast access times of 120 ns at low power dissipation. When the chip is deselected the standby current is less than 100 µA.

Atmel's 28C64 has additional features to ensure high quality and manufacturability. The device utilizes error correction internally for extended endurance and for improved data retention characteristics. An extra 32 bytes of EEPROM are available for device identification or tracking.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V
Voltage on $\overline{OE}$ and A9 with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Device Operation

READ: The AT28C64 is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in a high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual line control gives designers increased flexibility in preventing bus contention.

BYTE WRITE: Writing data into the AT28C64 is similar to writing into a Static RAM. A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{OE}$ high and $\overline{CE}$ or $\overline{WE}$ low (respectively) initiates a byte write. The address location is latched on the falling edge of $\overline{WE}$ (or $\overline{CE}$); the new data is latched on the rising edge. Internally, the device performs a self-clear before write. Once a byte write has been started, it will automatically time itself to completion. Once a programming operation has been initiated and for the duration of t_{WC}, a read operation will effectively be a polling operation.

FAST BYTE WRITE: The AT28C64E offers a byte write time of 200 µs maximum. This feature allows the entire device to be rewritten in 1.6 seconds.

READY/$\overline{BUSY}$: Pin 1 is an open drain RDY/$\overline{BUSY}$ output that can be used to detect the end of a write cycle. RDY/$\overline{BUSY}$ is actively pulled low during the write cycle and is released at the completion of the write. The open drain connection allows for OR-tying of several devices to the same RDY/$\overline{BUSY}$ line. The RDY/$\overline{BUSY}$ pin is not connected for the AT28C64X.

$\overline{DATA}$ POLLING: The AT28C64 provides $\overline{DATA}$ POLLING to signal the completion of a write cycle. During a write cycle, an attempted read of the data being written results in the complement of that data for I/O_7 (the other outputs are indeterminate). When the write cycle is finished, true data appears on all outputs.

WRITE PROTECTION: Inadvertent writes to the device are protected against in the following ways: (a) V_{CC} sense—if V_{CC} is below 3.8V (typical) the write function is inhibited; (b) V_{CC} power on delay—once V_{CC} has reached 3.8V the device will automatically time out 5 ms (typical) before allowing a byte write; and (c) write inhibit—holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits byte write cycles.

CHIP CLEAR: The contents of the entire memory of the AT28C64 may be set to the high state by the CHIP CLEAR operation. By setting $\overline{CE}$ low and $\overline{OE}$ to 12 volts, the chip is cleared when a 10 msec low pulse is applied to $\overline{WE}$.

DEVICE IDENTIFICATION: An extra 32 bytes of EEPROM memory are available to the user for device identification. By raising A9 to 12 ± 0.5V and using address locations 1FE0H to 1FFFH the additional bytes may be written to or read from in the same manner as the regular memory array.

3

DC and AC Operating Range

		AT28C64-12	AT28C64-15	AT28C64-20	AT28C64-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write[2]	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X[1]	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z
Chip Erase	V_{IL}	V_H[3]	V_{IL}	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to AC Programming Waveforms.
3. $V_H = 12.0V \pm 0.5V$.

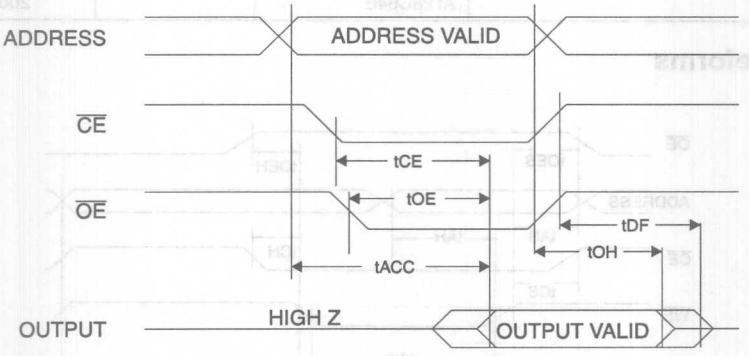
DC Characteristics

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	$V_{IN} = 0V$ to $V_{CC} + 1V$			10	µA
I_{LO}	Output Leakage Current	$V_{I/O} = 0V$ to V_{CC}			10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE} = V_{CC} - 0.3V$ to $V_{CC} + 1.0V$			100	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE} = 2.0V$ to $V_{CC} + 1.0V$	Com.		2	mA
			Ind.		3	mA
I_{CC}	V_{CC} Active Current AC	f = 5 MHz; $I_{OUT} = 0$ mA $\overline{CE} = V_{IL}$	Com.		30	mA
			Ind.		45	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1$ mA $= 4.0$ mA for RDY/$\overline{BUSY}$			0.45	V
V_{OH}	Output High Voltage	$I_{OH} = -400$ µA		2.4		V

AC Read Characteristics

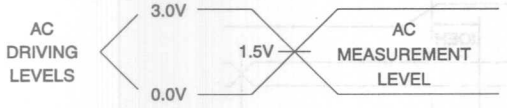
Symbol	Parameter	AT28C64-12		AT28C64-15		AT28C64-20		AT28C64-25		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		120		150		200		250	ns
t_{CE}[1]	$\overline{CE}$ to Output Delay		120		150		200		250	ns
t_{OE}[2]	$\overline{OE}$ to Output Delay	10	60	10	70	10	80	10	100	ns
t_{DF}[3][4]	$\overline{CE}$ or $\overline{OE}$ High to Output Float	0	45	0	50	0	55	0	60	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		0		ns

AC Read Waveforms[1][2][3][4]



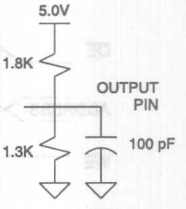
Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 20 ns

Output Test Load



Pin Capacitance

f = 1 MHz, T = 25°C[1]

Symbol	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

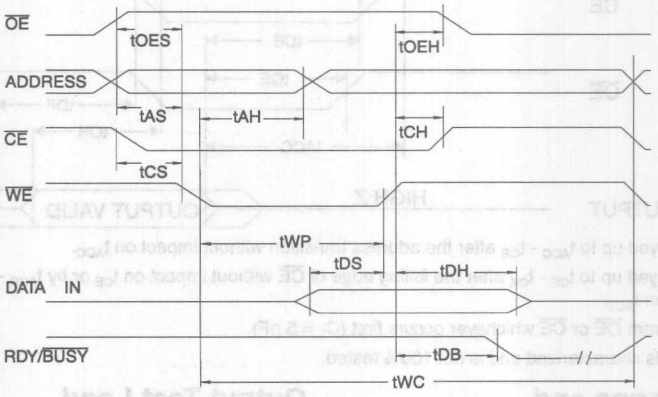
Note: 1. This parameter is characterized and is not 100% tested.

AC Write Characteristics

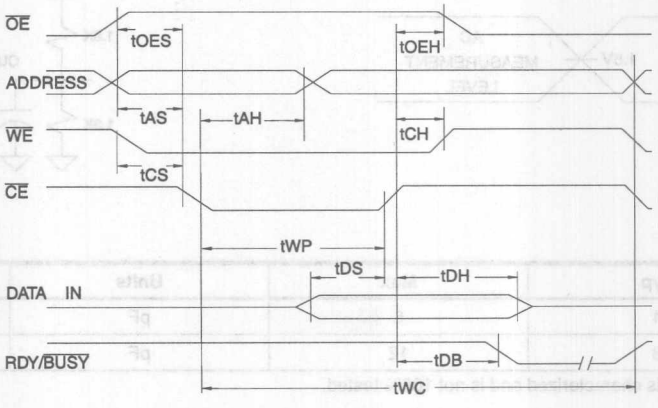
Symbol	Parameter		Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time		10		ns
t_{AH}	Address Hold Time		50		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)		100	1000	ns
t_{DS}	Data Set-up Time		50		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time		10		ns
t_{CS}, t_{CH}	$\overline{CE}$ to $\overline{WE}$ and $\overline{WE}$ to $\overline{CE}$ Set-up and Hold Time		0		ns
t_{DB}	Time to Device Busy			50	ns
t_{WC}	Write Cycle Time	AT28C64		1.0	ms
		AT28C64E		200	µs

AC Write Waveforms

$\overline{WE}$ Controlled



$\overline{CE}$ Controlled

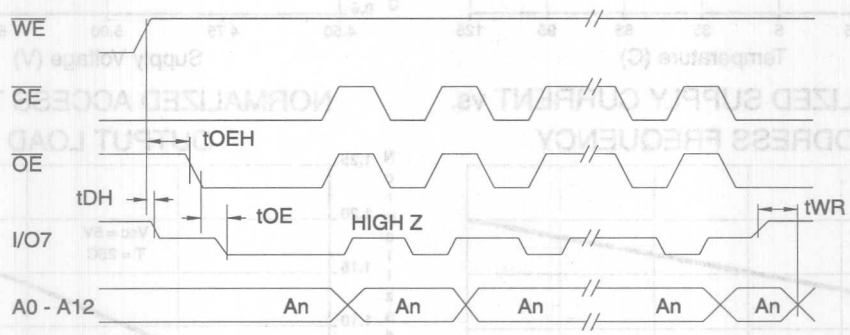


$\overline{\text{Data}}$ Polling Characteristics[1]

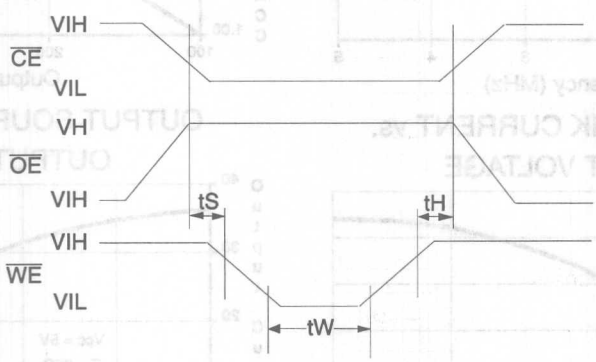
Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay[2]				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See AC Read Characteristics.

$\overline{\text{Data}}$ Polling Waveforms

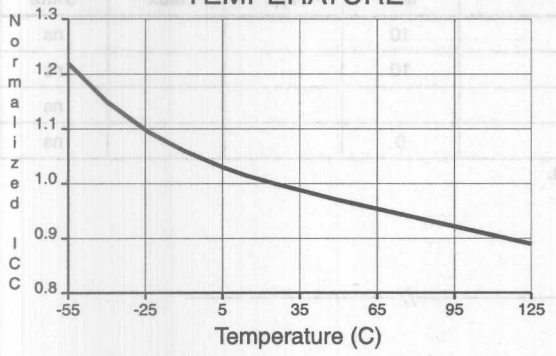


Chip Erase Waveforms

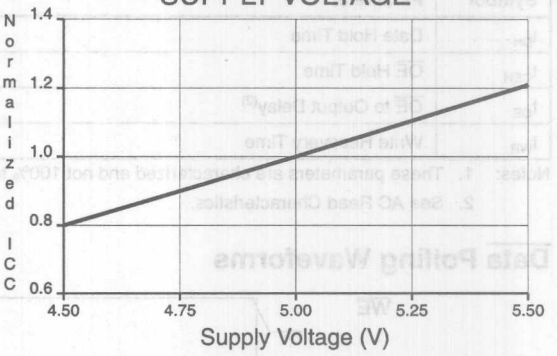


$t_S = t_H = 1$ µsec (min.)
$t_W = 10$ msec (min.)
$V_H = 12.0 \pm 0.5$V

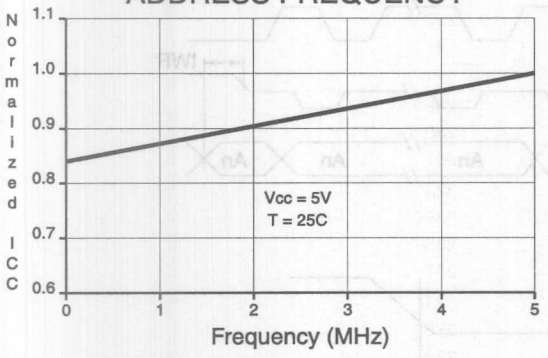
NORMALIZED SUPPLY CURRENT vs. TEMPERATURE



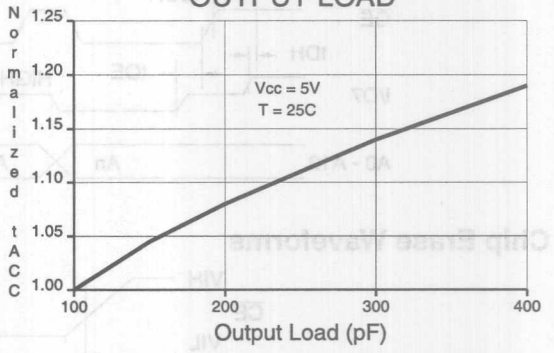
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



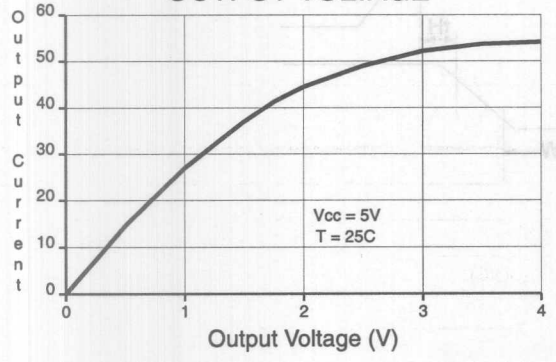
NORMALIZED SUPPLY CURRENT vs. ADDRESS FREQUENCY



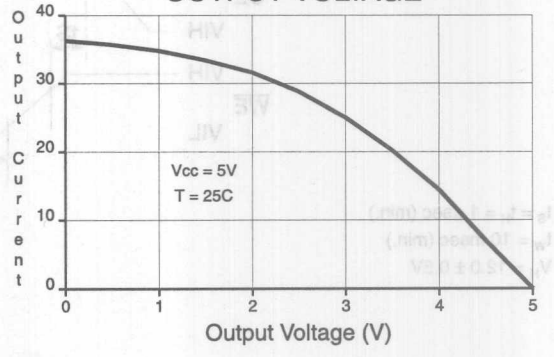
NORMALIZED ACCESS TIME vs. OUTPUT LOAD



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



AT28C64 Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
120	30	0.1	AT28C64(E)-12JC AT28C64(E)-12PC AT28C64(E)-12SC AT28C64(E)-12TC	32J 28P6 28S 28T	Commercial (0°C to 70°C)
	45	0.1	AT28C64(E)-12JI AT28C64(E)-12PI AT28C64(E)-12SI AT28C64(E)-12TI	32J 28P6 28S 28T	Industrial (-40°C to 85°C)
150	30	0.1	AT28C64(E)-15JC AT28C64(E)-15PC AT28C64(E)-15SC AT28C64(E)-15TC	32J 28P6 28S 28T	Commercial (0°C to 70°C)
	45	0.1	AT28C64(E)-15JI AT28C64(E)-15PI AT28C64(E)-15SI AT28C64(E)-15TI	32J 28P6 28S 28T	Industrial (-40°C to 85°C)
200	30	0.1	AT28C64(E)-20JC AT28C64(E)-20PC AT28C64(E)-20SC AT28C64(E)-20TC	32J 28P6 28S 28T	Commercial (0°C to 70°C)
	45	0.1	AT28C64(E)-20JI AT28C64(E)-20PI AT28C64(E)-20SI AT28C64(E)-20TI	32J 28P6 28S 28T	Industrial (-40°C to 85°C)
250	30	0.1	AT28C64(E)-25JC AT28C64(E)-25PC AT28C64(E)-25SC AT28C64(E)-25TC	32J 28P6 28S 28T	Commercial (0°C to 70°C)
	45	0.1	AT28C64(E)-25JI AT28C64(E)-25PI AT28C64(E)-25SI AT28C64(E)-25TI	32J 28P6 28S 28T	Industrial (-40°C to 85°C)

Package Type	
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
28P6	28 Lead, 0.600" Wide, Plastic Dull Inline Package (PDIP)
28S	28 Lead, 0.300" Wide, Plastic Gull Wing, Small Outline (SOIC)
28T	28 Lead, Plastic Thin Small Outline Package (TSOP)
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 1 ms
E	High Endurance Option: Endurance = 100K Write Cycles; Write Time = 200 µs

AT28C64X Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
150	30	0.1	AT28C64X-15JC AT28C64X-15PC AT28C64X-15SC AT28C64X-15TC	32J 28P6 28S 28T	Commercial (0°C to 70°C)
	45	0.1	AT28C64X-15JI AT28C64X-15PI AT28C64X-15SI AT28C64X-15TI	32J 28P6 28S 28T	Industrial (-40°C to 85°C)
200	30	0.1	AT28C64X-20JC AT28C64X-20PC AT28C64X-20SC AT28C64X-20TC	32J 28P6 28S 28T	Commercial (0°C to 70°C)
	45	0.1	AT28C64X-20JI AT28C64X-20PI AT28C64X-20SI AT28C64X-20TI	32J 28P6 28S 28T	Industrial (-40°C to 85°C)
250	30	0.1	AT28C64X-25JC AT28C64X-25PC AT28C64X-25SC AT28C64X-25TC	32J 28P6 28S 28T	Commercial (0°C to 70°C)
	45	0.1	AT28C64X-25JI AT28C64X-25PI AT28C64X-25SI AT28C64X-25TI	32J 28P6 28S 28T	Industrial (-40°C to 85°C)

Valid Part Numbers

The following table lists standard Atmel products that can be ordered.

Device Numbers	Speed	Package and Temperature Combinations
AT28C64 X	12	JC, JI, PC, PI, SC, SI, TC, TI
AT28C64 X	15	JC, JI, PC, PI, SC, SI, TC, TI
AT28C64 X	20	JC, JI, PC, PI, SC, SI, TC, TI
AT28C64 X	25	JC, JI, PC, PI, SC, SI, TC, TI

Die Products

Reference Section: Parallel EEPROM Die Products

Package Type	
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
28P6	28 Lead, 0.600" Wide, Plastic Dull Inline Package (PDIP)
28S	28 Lead, 0.300" Wide, Plastic Gull Wing, Small Outline (SOIC)
28T	28 Lead, Plastic Thin Small Outline Package (TSOP)

Features

- Fast Read Access Time - 150 ns
- Automatic Page Write Operation
  - Internal Address and Data Latches for 64 Bytes
- Fast Write Cycle Times
  - Page Write Cycle Time: 10 ms Maximum
  - 1 to 64-Byte Page Write Operation
- Low Power Dissipation
  - 40 mA Active Current
  - 100 µA CMOS Standby Current
- Hardware and Software Data Protection
- $\overline{\text{DATA}}$ Polling and Toggle Bit for End of Write Detection
- High Reliability CMOS Technology
  - Endurance: 100,000 Cycles
  - Data Retention: 10 Years
- Single 5V ± 10% Supply
- CMOS and TTL Compatible Inputs and Outputs
- JEDEC Approved Byte-Wide Pinout
- Commercial and Industrial Temperature Ranges

Description

The AT28C64B is a high-performance electrically erasable and programmable read only memory (EEPROM). Its 64K of memory is organized as 8,192 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 150 ns with power dissipation of just 220 mW. When the device is deselected, the CMOS standby current is less than 100 µA. *(continued)*

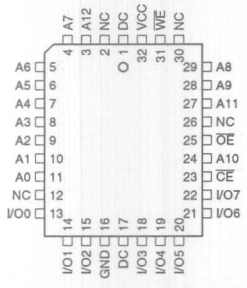
Pin Configurations

Pin Name	Function
A0 - A12	Addresses
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect
DC	Don't Connect

PDIP, SOIC
Top View

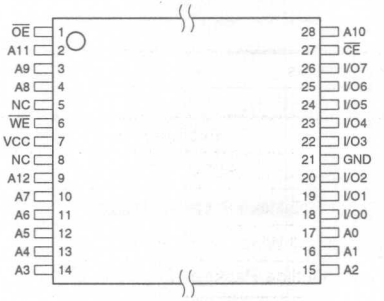


PLCC
Top View



Note: PLCC package pins 1 and 17 are DON'T CONNECT.

TSOP
Top View



64K (8K x 8) Parallel EEPROMs with Page Write and Software Data Protection

AT28C64B

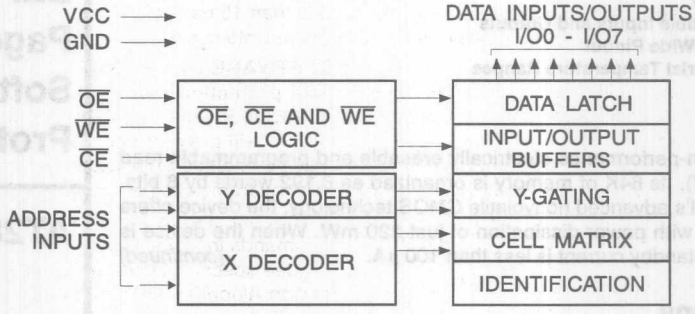
3

Rev. 0270F–10/98

The AT28C64B is accessed like a Static RAM for the read or write cycle without the need for external components. The device contains a 64-byte page register to allow writing of up to 64 bytes simultaneously. During a write cycle, the addresses and 1 to 64 bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by $\overline{\text{DATA}}$ POLLING of I/O_7. Once the end of a write cycle has been detected, a new access for a read or write can begin.

Atmel's AT28C64B has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and improved data retention characteristics. An optional software data protection mechanism is available to guard against inadvertent writes. The device also includes an extra 64 bytes of EEPROM for device identification or tracking.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V
Voltage on $\overline{\text{OE}}$ and A9 with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Device Operation

READ: The AT28C64B is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high-impedance state when either $\overline{CE}$ or $\overline{OE}$ is high. This dual line control gives designers flexibility in preventing bus contention in their systems.

BYTE WRITE: A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high initiates a write cycle. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Once a byte write has been started, it will automatically time itself to completion. Once a programming operation has been initiated and for the duration of t_{WC}, a read operation will effectively be a polling operation.

PAGE WRITE: The page write operation of the AT28C64B allows 1 to 64 bytes of data to be written into the device during a single internal programming period. A page write operation is initiated in the same manner as a byte write; after the first byte is written, it can then be followed by 1 to 63 additional bytes. Each successive byte must be loaded within 150 µs (t_{BLC}) of the previous byte. If the t_{BLC} limit is exceeded, the AT28C64B will cease accepting data and commence the internal programming operation. All bytes during a page write operation must reside on the same page as defined by the state of the A6 to A12 inputs. For each $\overline{WE}$ high to low transition during the page write operation, A6 to A12 must be the same.

The A0 to A5 inputs specify which bytes within the page are to be written. The bytes may be loaded in any order and may be altered within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

$\overline{DATA}$ POLLING: The AT28C64B features $\overline{DATA}$ Polling to indicate the end of a write cycle. During a byte or page write cycle an attempted read of the last byte written will result in the complement of the written data to be presented on I/O_7. Once the write cycle has been completed, true data is valid on all outputs, and the next write cycle may begin. $\overline{DATA}$ Polling may begin at any time during the write cycle.

TOGGLE BIT: In addition to $\overline{DATA}$ Polling, the AT28C64B provides another method for determining the end of a write cycle. During the write operation, successive attempts to read data from the device will result in I/O_6 toggling between one and zero. Once the write has completed, I/O_6 will stop toggling, and valid data will be read. Toggle bit reading may begin at any time during the write cycle.

DATA PROTECTION: If precautions are not taken, inadvertent writes may occur during transitions of the host system power supply. Atmel has incorporated both hardware and software features that will protect the memory against inadvertent writes.

HARDWARE DATA PROTECTION: Hardware features protect against inadvertent writes to the AT28C64B in the following ways: (a) V_{CC} sense—if V_{CC} is below 3.8V (typical), the write function is inhibited; (b) V_{CC} power-on delay—once V_{CC} has reached 3.8V, the device will automatically time out 5 ms (typical) before allowing a write; (c) write inhibit—holding any one of $\overline{OE}$ low, $\overline{CE}$ high, or $\overline{WE}$ high inhibits write cycles; and (d) noise filter—pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a write cycle.

SOFTWARE DATA PROTECTION: A software controlled data protection feature has been implemented on the AT28C64B. When enabled, the software data protection (SDP), will prevent inadvertent writes. The SDP feature may be enabled or disabled by the user; the AT28C64B is shipped from Atmel with SDP disabled.

SDP is enabled by the user issuing a series of three write commands in which three specific bytes of data are written to three specific addresses (refer to the *Software Data Protection Algorithm* diagram in this data sheet). After writing the 3-byte command sequence and waiting t_{WC}, the entire AT28C64B will be protected against inadvertent writes. It should be noted that even after SDP is enabled, the user may still perform a byte or page write to the AT28C64B by preceding the data to be written by the same 3-byte command sequence used to enable SDP.

Once set, SDP remains active unless the disable command sequence is issued. Power transitions do not disable SDP, and SDP protects the AT28C64B during power-up and power-down conditions. All command sequences must conform to the page write timing specifications. The data in the enable and disable command sequences is not actually written into the device; their addresses may still be written with user data in either a byte or page write operation.

After setting SDP, any attempt to write to the device without the 3-byte command sequence will start the internal write timers. No data will be written to the device. However, for the duration of t_{WC}, read operations will effectively be polling operations.

DEVICE IDENTIFICATION: An extra 64 bytes of EEPROM memory are available to the user for device identification. By raising A9 to 12V ± 0.5V and using address locations 1FC0H to 1FFFH, the additional bytes may be written to or read from in the same manner as the regular memory array.

DC and AC Operating Range

		AT28C64B-15	AT28C64B-20	AT28C64B-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		5V ± 10%	5V ± 10%	5V ± 10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write[2]	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X[1]	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z
Chip Erase	V_{IL}	V_H[3]	V_{IL}	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to the *AC Write Waveforms* diagrams in this data sheet.
3. $V_H = 12.0V \pm 0.5V$.

DC Characteristics

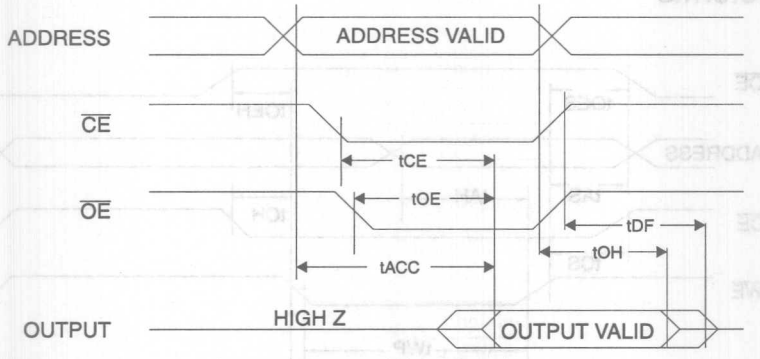
Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	$V_{IN} = 0V$ to $V_{CC} + 1V$			10	µA
I_{LO}	Output Leakage Current	$V_{I/O} = 0V$ to V_{CC}			10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE} = V_{CC} - 0.3V$ to $V_{CC} + 1V$	Com., Ind.		100	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE} = 2.0V$ to $V_{CC} + 1V$			2	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz; $I_{OUT} = 0$ mA			40	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1$ mA			0.40	V
V_{OH}	Output High Voltage	$I_{OH} = -400$ µA		2.4		V

AC Read Characteristics

Symbol	Parameter	AT28C64B-15		AT28C64B-20		AT28C64B-25		Units
		Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		150		200		250	ns
t_{CE}[1]	$\overline{CE}$ to Output Delay		150		200		250	ns
t_{OE}[2]	$\overline{OE}$ to Output Delay	0	70	0	80	0	100	ns
t_{DF}[3][4]	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	50	0	55	0	60	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		ns

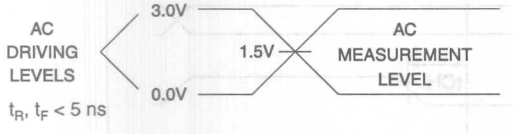
3

AC Read Waveforms[1][2][3][4]

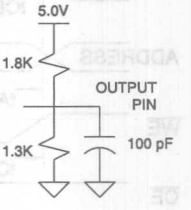


Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



Output Test Load



Pin Capacitance

f = 1 MHz, T = 25°C[1]

Symbol	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

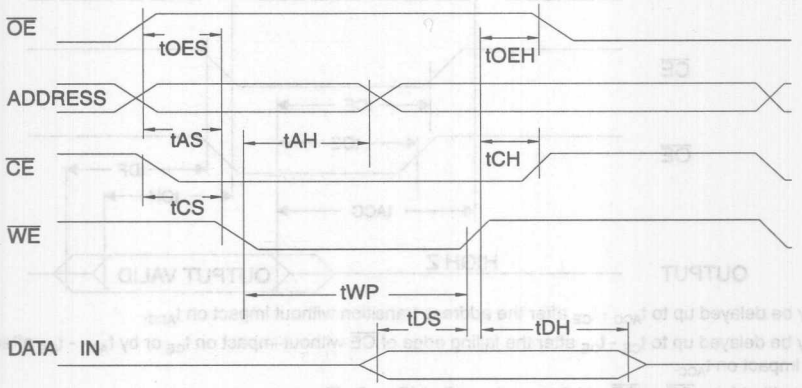
Note: 1. This parameter is characterized and is not 100% tested.

AC Write Characteristics

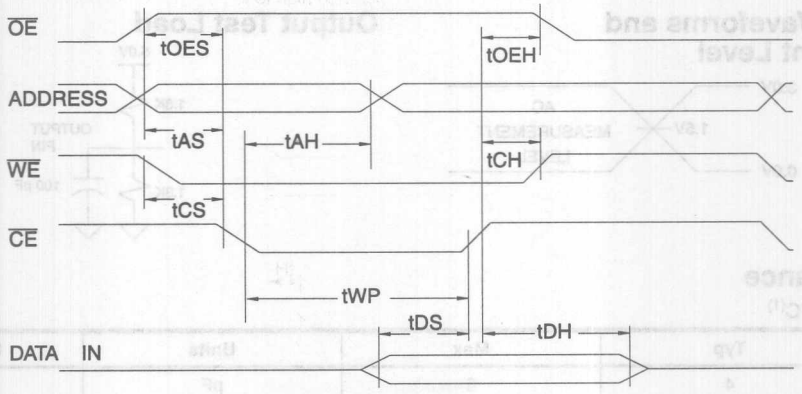
Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	100		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	0		ns

AC Write Waveforms

$\overline{WE}$ Controlled



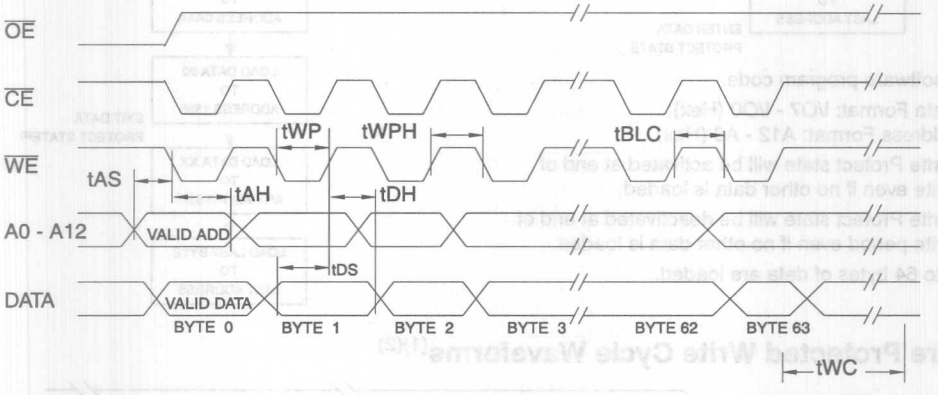
$\overline{CE}$ Controlled



Page Mode Characteristics

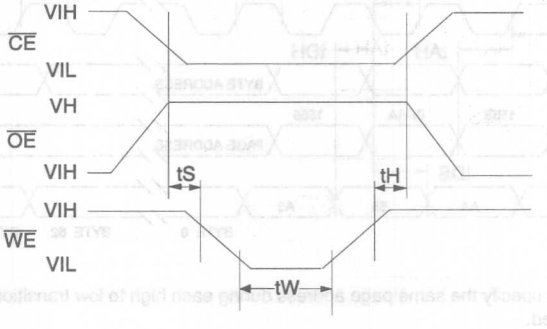
Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time		10	ms
t_{WC}	Write Cycle Time (28C64B SL184)	0	3	ms
t_{AS}	Address Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}	Data Hold Time	0		ns
t_{WP}	Write Pulse Width	100		ns
t_{BLC}	Byte Load Cycle Time		150	µs
t_{WPH}	Write Pulse Width High	50		ns

Page Mode Write Waveforms(1)(2)



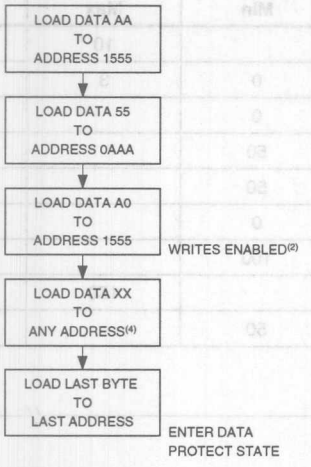
Notes: 1. A6 through A12 must specify the same page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
2. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

Chip Erase Waveforms

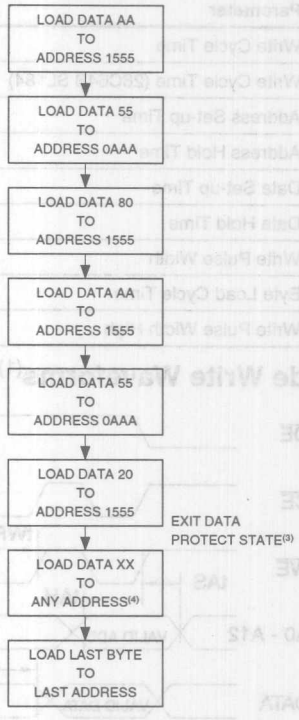


$t_S = t_H = 1$ µsec (min.)
$t_W = 10$ msec (min.)
$V_H = 12.0 \pm 0.5V$

Software Data Protection Enable Algorithm[1]



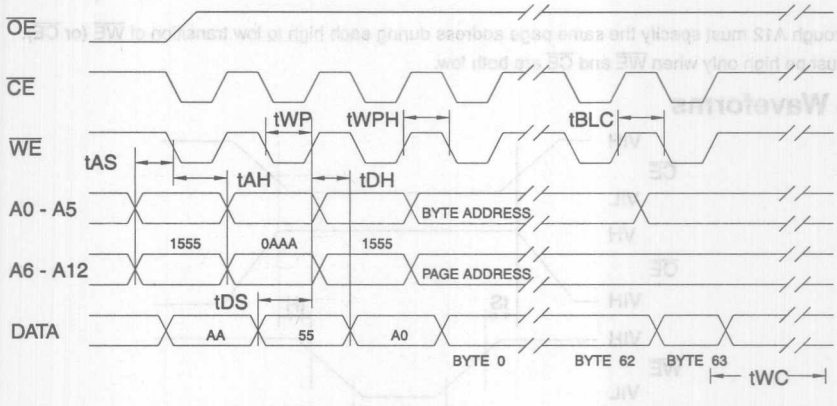
Software Data Protection Disable Algorithm[1]



Notes for software program code:

1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A12 - A0 (Hex).
2. Write Protect state will be activated at end of write even if no other data is loaded.
3. Write Protect state will be deactivated at end of write period even if no other data is loaded.
4. 1 to 64 bytes of data are loaded.

Software Protected Write Cycle Waveforms[1][2]



Notes: 1. A6 through A12 must specify the same page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$) after the software code has been entered.

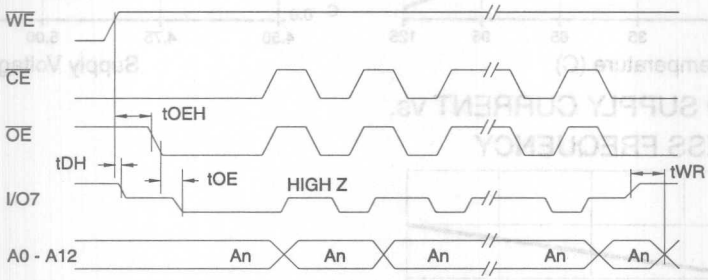
2. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

$\overline{\text{Data}}$ Polling Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	0			ns
t_{OEH}	$\overline{OE}$ Hold Time	0			ns
t_{OE}	$\overline{OE}$ to Output Delay[2]				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See AC Read Characteristics.

$\overline{\text{Data}}$ Polling Waveforms

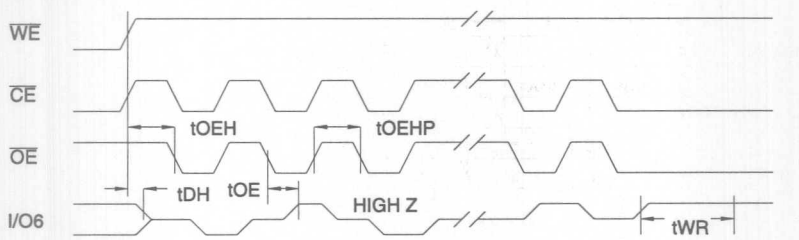


Toggle Bit Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay[2]				ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

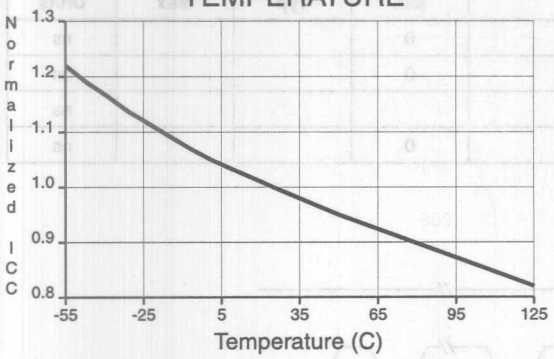
Notes: 1. These parameters are characterized and not 100% tested.
2. See AC Read Characteristics.

Toggle Bit Waveforms[1][2][3]

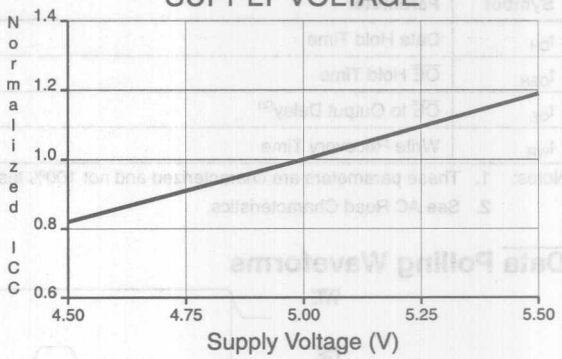


Notes: 1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

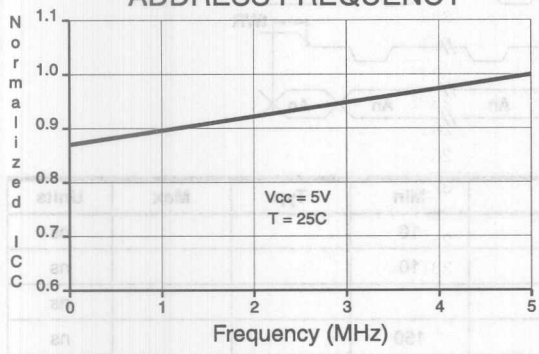
NORMALIZED SUPPLY CURRENT vs. TEMPERATURE



NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



NORMALIZED SUPPLY CURRENT vs. ADDRESS FREQUENCY



Ordering Information[1]

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
150	40	0.1	AT28C64B-15JC AT28C64B-15PC AT28C64B-15SC AT28C64B-15TC	32J 28P6 28S 28T	Commercial (0°C to 70°C)
			AT28C64B-15JI AT28C64B-15PI AT28C64B-15SI AT28C64B-15TI	32J 28P6 28S 28T	Industrial (-40°C to 85°C)
200	40	0.1	AT28C64B-20JC AT28C64B-20PC AT28C64B-20SC AT28C64B-20TC	32J 28P6 28S 28T	Commercial (0°C to 70°C)
			AT28C64B-20JI AT28C64B-20PI AT28C64B-20SI AT28C64B-20TI	32J 28P6 28S 28T	Industrial (-40°C to 85°C)
250	40	0.1	AT28C64B-25JC AT28C64B-25PC AT28C64B-25SC AT28C64B-25TC	32J 28P6 28S 28T	Commercial (0°C to 70°C)
			AT28C64B-25JI AT28C64B-25PI AT28C64B-25SI AT28C64B-25TI	32J 28P6 28S 28T	Industrial (-40°C to 85°C)

Note: 1. See Valid Part Numbers table below.

Valid Part Numbers

The following table lists standard Atmel products that can be ordered.

Device Numbers	Speed	Package and Temperature Combinations
AT28C64B	15	JC, JI, PC, PI, SC, SI, TC, TI
AT28C64B	20	JC, JI, PC, PI, SC, SI, TC, TI
AT28C64B	25	JC, JI, PC, PI, SC, SI, TC, TI
AT28C64B	-	W

Die Products

Reference Section: Parallel EEPROM Die Products

Package Type	
32J	32-Lead, Plastic J-Leaded Chip Carrier (PLCC)
28P6	28-Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
28S	28-Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
28T	28-Lead, Plastic Thin Small Outline Package (TSOP)
W	Die

Ordering Information[1]

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
150	40	0.1	AT28C64B-15JC	32J	Commercial
			AT28C64B-15PC	28P6	(0°C to 70°C)
			AT28C64B-15SC	28S	
			AT28C64B-15TC	28T	
			AT28C64B-15JI	32J	Industrial
			AT28C64B-15PI	28P6	(-40°C to 85°C)
			AT28C64B-15SI	28S	
			AT28C64B-15TI	28T	
200	40	0.1	AT28C64B-20JC	32J	Commercial
			AT28C64B-20PC	28P6	(0°C to 70°C)
			AT28C64B-20SC	28S	
			AT28C64B-20TC	28T	
			AT28C64B-20JI	32J	Industrial
			AT28C64B-20PI	28P6	(-40°C to 85°C)
			AT28C64B-20SI	28S	
			AT28C64B-20TI	28T	
250	40	0.1	AT28C64B-25JC	32J	Commercial
			AT28C64B-25PC	28P6	(0°C to 70°C)
			AT28C64B-25SC	28S	
			AT28C64B-25TC	28T	
			AT28C64B-25JI	32J	Industrial
			AT28C64B-25PI	28P6	(-40°C to 85°C)
			AT28C64B-25SI	28S	
			AT28C64B-25TI	28T	

Note: 1. See Valid Part Numbers table below.

Valid Part Numbers

The following table lists standard Atmel products that can be ordered.

Device Numbers	Speed	Package and Temperature Combinations
AT28C64B	-15	JC, JI, PC, PI, SC, SI, TC, TI
AT28C64B	-20	JC, JI, PC, PI, SC, SI, TC, TI
AT28C64B	-25	JC, JI, PC, PI, SC, SI, TC, TI
AT28C64B	-	W

Die Products

Reference Section: Parallel EEPROM Die Products

	Package Type
32J	32-Lead, Plastic J-Leaded Chip Carrier (PLCC)
28P6	28-Lead, 0.600" Wide, Plastic Dual In-line Package (PDIP)
28S	28-Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
28T	28-Lead, Plastic Thin Small Outline Package (TSOP)
W	Die

Features

- Fast Read Access Time - 150 ns
- Automatic Page Write Operation
  - Internal Address and Data Latches for 64 Bytes
  - Internal Control Timer
- Fast Write Cycle Times
  - Page Write Cycle Time: 3 ms or 10 ms Maximum
  - 1 to 64-Byte Page Write Operation
- Low Power Dissipation
  - 50 mA Active Current
  - 200 µA CMOS Standby Current
- Hardware and Software Data Protection
- $\overline{\text{DATA}}$ Polling for End of Write Detection
- High Reliability CMOS Technology
  - Endurance: 10^4 or 10^5 Cycles
  - Data Retention: 10 Years
- Single 5V ± 10% Supply
- CMOS and TTL Compatible Inputs and Outputs
- JEDEC Approved Byte-Wide Pinout
- Full Military, Commercial, and Industrial Temperature Ranges

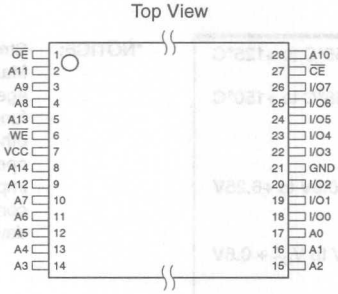
Description

The AT28C256 is a high-performance Electrically Erasable and Programmable Read Only Memory. Its 256K of memory is organized as 32,768 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 150 ns with power dissipation of just 440 mW. When the device is deselected, the CMOS standby current is less than 200 µA. *(continued)*

Pin Configurations

Pin Name	Function
A0 - A14	Addresses
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect
DC	Don't Connect

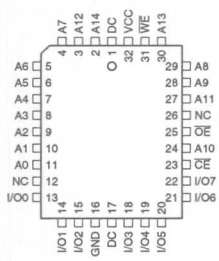
TSOP
Top View



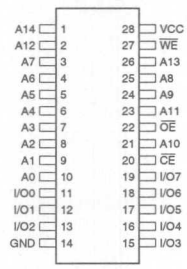
PGA
Top View

4 A6	3 A7	1 A14	27 $\overline{\text{WE}}$	26 A13
5 A5	2 A12	28 VCC	24 A9	25 A8
7 A3	6 A4		22 $\overline{\text{OE}}$	23 A11
9 A1	8 A2		20 $\overline{\text{CE}}$	21 A10
11 I/O0	10 A0	14 GND	16 I/O4	19 I/O7
12 I/O1	13 I/O2	15 I/O3	17 I/O5	18 I/O6

LCC, PLCC
Top View



CERDIP, PDIP, FLATPACK, SOIC — Top View



Note: PLCC package pins 1 and 17 are DON'T CONNECT.

256K (32K x 8) Paged Parallel EEPROMs

3

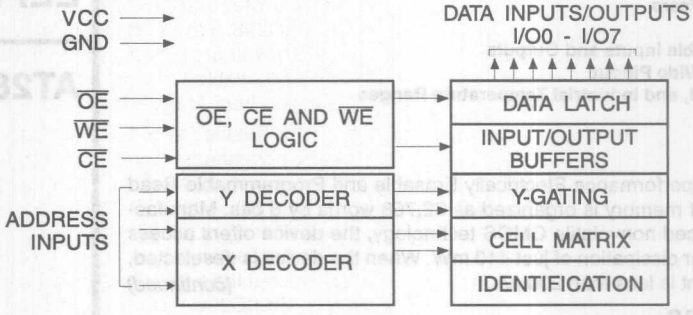
AT28C256

Rev. 0006G–10/98

The AT28C256 is accessed like a Static RAM for the read or write cycle without the need for external components. The device contains a 64-byte page register to allow writing of up to 64 bytes simultaneously. During a write cycle, the addresses and 1 to 64 bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by $\overline{\text{DATA}}$ POLLING of I/O_7. Once the end of a write cycle has been detected a new access for a read or write can begin.

Atmel's 28C256 has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and improved data retention characteristics. An optional software data protection mechanism is available to guard against inadvertent writes. The device also includes an extra 64 bytes of EEPROM for device identification or tracking.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V
Voltage on $\overline{\text{OE}}$ and A9 with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Device Operation

READ: The AT28C256 is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state when either $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention in their system.

BYTE WRITE: A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high initiates a write cycle. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Once a byte write has been started it will automatically time itself to completion. Once a programming operation has been initiated and for the duration of t_{WC}, a read operation will effectively be a polling operation.

PAGE WRITE: The page write operation of the AT28C256 allows 1 to 64 bytes of data to be written into the device during a single internal programming period. A page write operation is initiated in the same manner as a byte write; the first byte written can then be followed by 1 to 63 additional bytes. Each successive byte must be written within 150 µs (t_{BLC}) of the previous byte. If the t_{BLC} limit is exceeded the AT28C256 will cease accepting data and commence the internal programming operation. All bytes during a page write operation must reside on the same page as defined by the state of the A6 - A14 inputs. For each $\overline{WE}$ high to low transition during the page write operation, A6 - A14 must be the same.

The A0 to A5 inputs are used to specify which bytes within the page are to be written. The bytes may be loaded in any order and may be altered within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

$\overline{DATA}$ POLLING: The AT28C256 features $\overline{DATA}$ Polling to indicate the end of a write cycle. During a byte or page write cycle an attempted read of the last byte written will result in the complement of the written data to be presented on I/O_7. Once the write cycle has been completed, true data is valid on all outputs, and the next write cycle may begin. $\overline{DATA}$ Polling may begin at anytime during the write cycle.

TOGGLE BIT: In addition to $\overline{DATA}$ Polling the AT28C256 provides another method for determining the end of a write cycle. During the write operation, successive attempts to read data from the device will result in I/O_6 toggling between one and zero. Once the write has completed, I/O_6 will stop toggling and valid data will be read. Reading the toggle bit may begin at any time during the write cycle.

DATA PROTECTION: If precautions are not taken, inadvertent writes may occur during transitions of the host system power supply. Atmel has incorporated both hardware and software features that will protect the memory against inadvertent writes.

HARDWARE PROTECTION: Hardware features protect against inadvertent writes to the AT28C256 in the following ways: (a) V_{CC} sense—if V_{CC} is below 3.8V (typical) the write function is inhibited; (b) V_{CC} power-on delay—once V_{CC} has reached 3.8V the device will automatically time out 5 ms (typical) before allowing a write; (c) write inhibit—holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits write cycles; and (d) noise filter—pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a write cycle.

SOFTWARE DATA PROTECTION: A software controlled data protection feature has been implemented on the AT28C256. When enabled, the software data protection (SDP), will prevent inadvertent writes. The SDP feature may be enabled or disabled by the user; the AT28C256 is shipped from Atmel with SDP disabled.

SDP is enabled by the host system issuing a series of three write commands; three specific bytes of data are written to three specific addresses (refer to Software Data Protection Algorithm). After writing the 3-byte command sequence and after t_{WC} the entire AT28C256 will be protected against inadvertent write operations. It should be noted, that once protected the host may still perform a byte or page write to the AT28C256. This is done by preceding the data to be written by the same 3-byte command sequence used to enable SDP.

Once set, SDP will remain active unless the disable command sequence is issued. Power transitions do not disable SDP and SDP will protect the AT28C256 during power-up and power-down conditions. All command sequences must conform to the page write timing specifications. The data in the enable and disable command sequences is not written to the device and the memory addresses used in the sequence may be written with data in either a byte or page write operation.

After setting SDP, any attempt to write to the device without the 3-byte command sequence will start the internal write timers. No data will be written to the device; however, for the duration of t_{WC}, read operations will effectively be polling operations.

DEVICE IDENTIFICATION: An extra 64 bytes of EEPROM memory are available to the user for device identification. By raising A9 to 12V ± 0.5V and using address locations 7FC0H to 7FFFH the additional bytes may be written to or read from in the same manner as the regular memory array.

OPTIONAL CHIP ERASE MODE: The entire device can be erased using a 6-byte software code. Please see Software Chip Erase application note for details.

DC and AC Operating Range

		AT28C256-15	AT28C256-20	AT28C256-25	AT28C256-35
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	
	Mil.	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write[2]	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X[1]	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z
Chip Erase	V_{IL}	V_H[3]	V_{IL}	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to AC Programming Waveforms.
3. $V_H = 12.0V \pm 0.5V$.

DC Characteristics

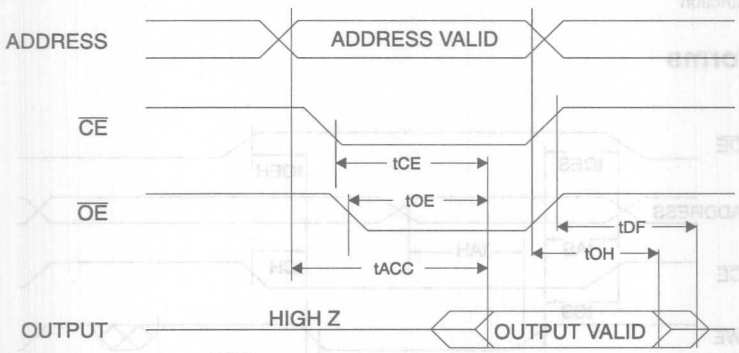
Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	$V_{IN} = 0V$ to $V_{CC} + 1V$			10	µA
I_{LO}	Output Leakage Current	$V_{I/O} = 0V$ to V_{CC}			10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE} = V_{CC} - 0.3V$ to $V_{CC} + 1V$	Com., Ind.		200	µA
			Mil.		300	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE} = 2.0V$ to $V_{CC} + 1V$			3	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz; $I_{OUT} = 0$ mA			50	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1$ mA			0.45	V
V_{OH}	Output High Voltage	$I_{OH} = -400$ µA		2.4		V

AC Read Characteristics

Symbol	Parameter	AT28C256-15		AT28C256-20		AT28C256-25		AT28C256-35		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		150		200		250		350	ns
t_{CE}[1]	$\overline{CE}$ to Output Delay		150		200		250		350	ns
t_{OE}[2]	$\overline{OE}$ to Output Delay	0	70	0	80	0	100	0	100	ns
t_{DF}[3][4]	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	50	0	55	0	60	0	70	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		0		ns

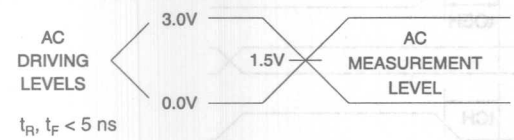
3

AC Read Waveforms[1][2][3][4]

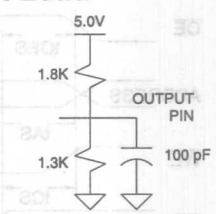


Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



Output Test Load



Pin Capacitance

f = 1 MHz, T = 25°C[1]

Symbol	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

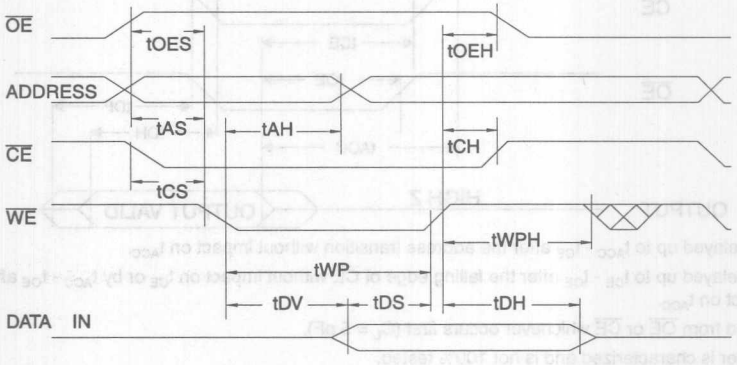
AC Write Characteristics

Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	100		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	0		ns
t_{DV}	Time to Data Valid	NR(1)		

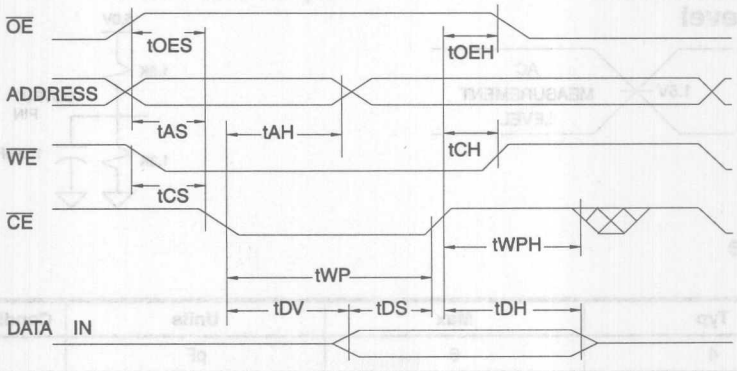
Note: 1. NR = No Restriction

AC Write Waveforms

$\overline{WE}$ Controlled



$\overline{CE}$ Controlled

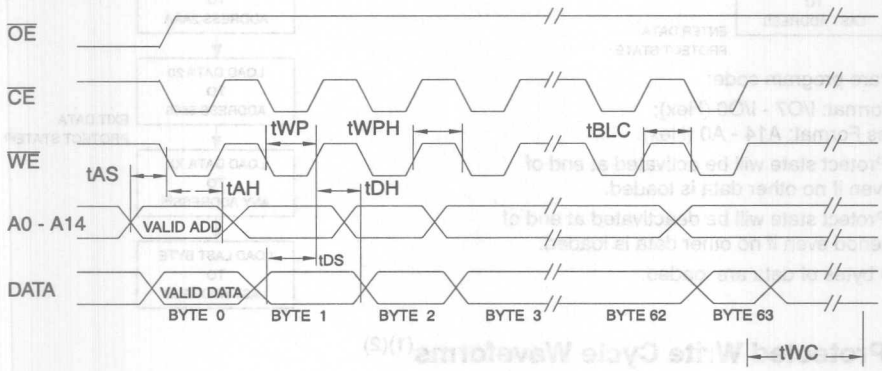


Page Mode Characteristics

Symbol	Parameter		Min	Max	Units
t_{WC}	Write Cycle Time	AT28C256		10	ms
		AT28C256F		3.0	ms
t_{AS}	Address Set-up Time		0		ns
t_{AH}	Address Hold Time		50		ns
t_{DS}	Data Set-up Time		50		ns
t_{DH}	Data Hold Time		0		ns
t_{WP}	Write Pulse Width		100		ns
t_{BLC}	Byte Load Cycle Time			150	µs
t_{WPH}	Write Pulse Width High		50		ns

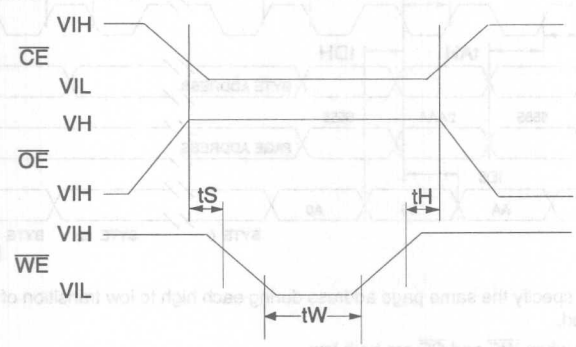
3

Page Mode Write Waveforms(1)(2)



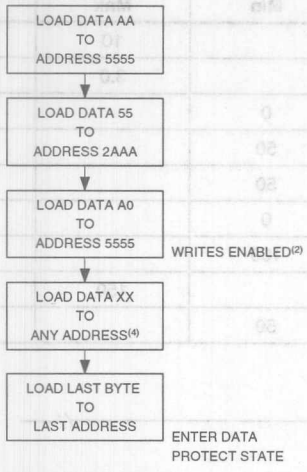
Notes: 1. A6 through A14 must specify the same page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
2. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

Chip Erase Waveforms

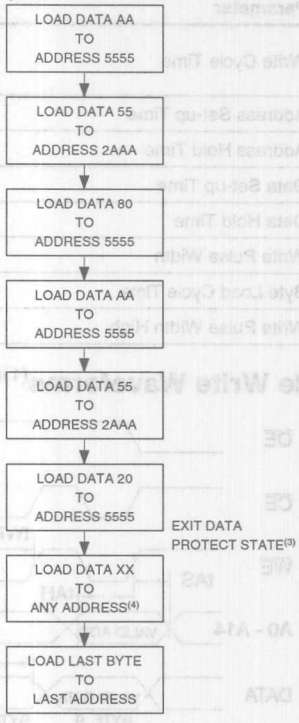


$t_S = t_H = 5$ µsec (min.)
$t_W = 10$ msec (min.)
$V_H = 12.0V \pm 0.5V$

Software Data Protection Enable Algorithm[1]



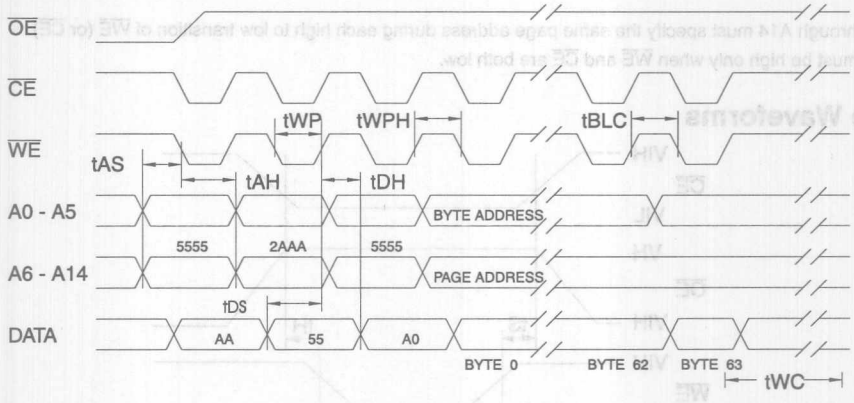
Software Data Protection Disable Algorithm[1]



Notes for software program code:

1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Write Protect state will be activated at end of write even if no other data is loaded.
3. Write Protect state will be deactivated at end of write period even if no other data is loaded.
4. 1 to 64 bytes of data are loaded.

Software Protected Write Cycle Waveforms[1][2]



Notes: 1. A6 through A14 must specify the same page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$) after the software code has been entered.

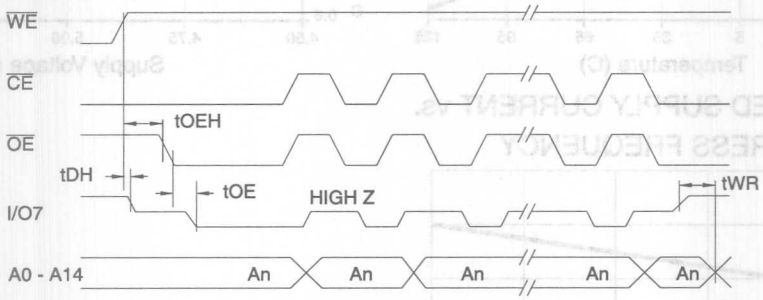
2. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

Data Polling Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	0			ns
t_{OEH}	$\overline{OE}$ Hold Time	0			ns
t_{OE}	$\overline{OE}$ to Output Delay[2]				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See AC Read Characteristics.

Data Polling Waveforms

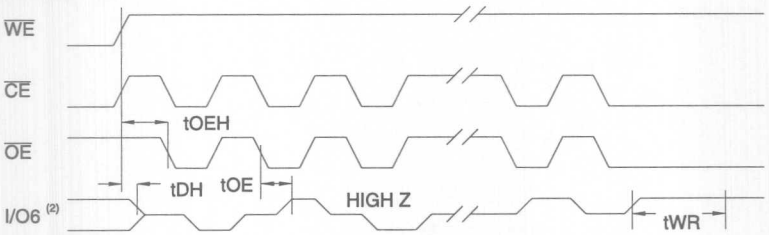


Toggle Bit Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay[2]				ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

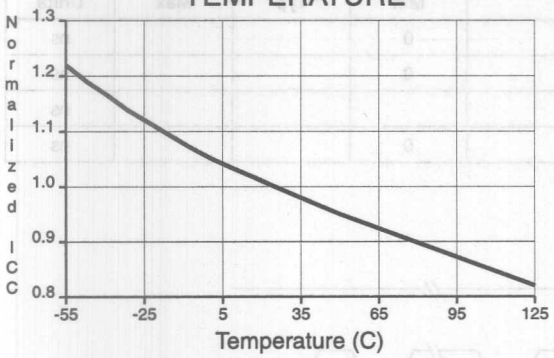
Notes: 1. These parameters are characterized and not 100% tested.
2. See AC Read Characteristics.

Toggle Bit Waveforms[1][2][3]

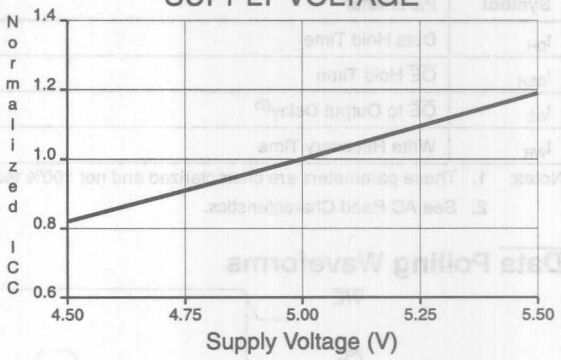


Notes: 1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

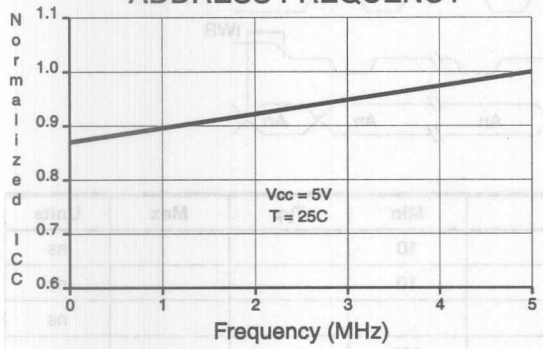
NORMALIZED SUPPLY CURRENT vs. TEMPERATURE



NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



NORMALIZED SUPPLY CURRENT vs. ADDRESS FREQUENCY



Ordering Information[2]

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
150	50	0.2	AT28C256(E,F)-15JC	32J	Commercial (0°C to 70°C)
			AT28C256(E,F)-15PC	28P6	
			AT28C256(E,F)-15SC	28S	
			AT28C256(E,F)-15TC	28T	
			AT28C256(E,F)-15JI	32J	Industrial (-40°C to 85°C)
			AT28C256(E,F)-15PI	28P6	
			AT28C256(E,F)-15SI	28S	
			AT28C256(E,F)-15TI	28T	
	50	0.3	AT28C256(E,F)-15DM/883	28D6	Military/883C Class B, Fully Compliant (-55°C to 125°C)
			AT28C256(E,F)-15FM/883	28F	
			AT28C256(E,F)-15LM/883	32L	
			AT28C256(E,F)-15UM/883	28U	
200	50	0.2	AT28C256(E,F)-20JC	32J	Commercial (0°C to 70°C)
			AT28C256(E,F)-20PC	28P6	
			AT28C256(E,F)-20SC	28S	
			AT28C256(E,F)-20TC	28T	
			AT28C256(E,F)-20JI	32J	Industrial (-40°C to 85°C)
			AT28C256(E,F)-20PI	28P6	
			AT28C256(E,F)-20SI	28S	
			AT28C256(E,F)-20TI	28T	
	50	0.3	AT28C256(E,F)-20DM/883	28D6	Military/883C Class B, Fully Compliant (-55°C to 125°C)
			AT28C256(E,F)-20FM/883	28F	
			AT28C256(E,F)-20LM/883	32L	
			AT28C256(E,F)-20UM/883	28U	

Package Type	
28D6	28-Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
28F	28-Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)
32J	32-Lead, Plastic J-Leaded Chip Carrier (PLCC)
32L	32-Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28-Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
28S	28-Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
28T	28-Lead, Plastic Thin Small Outline Package (TSOP)
28U	28-Pin, Ceramic Pin Grid Array (PGA)
W	Die
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 10 ms
E	High Endurance Option: Endurance = 100K Write Cycles
F	Fast Write Option: Write Time = 3 ms

Ordering Information[2]

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
250	50	0.2	AT28C256(E,F)-25JC	32J	Commercial (0°C to 70°C)
			AT28C256(E,F)-25PC	28P6	
			AT28C256-W	DIE	
			AT28C256(E,F)-25JI	32J	Industrial (-40°C to 85°C)
			AT28C256(E,F)-25PI	28P6	
	50	0.3	AT28C256(E,F)-25DM/883	28D6	Military/883C Class B, Fully Compliant (-55°C to 125°C)
			AT28C256(E,F)-25FM/883	28F	
			AT28C256(E,F)-25LM/883	32L	
			AT28C256(E,F)-25UM/883	28U	
			AT28C256(E,F)-35UM/883	28U	
150[3]	50	0.35	5962-88525 16 UX	28U	Military/883C Class B, Fully Compliant (-55°C to 125°C)
			5962-88525 16 XX	28D6	
			5962-88525 16 YX	32L	
			5962-88525 16 ZX	28F	
			5962-88525 15 UX	28U	Military/883C Class B, Fully Compliant (-55°C to 125°C)
			5962-88525 15 XX	28D6	
			5962-88525 15 YX	32L	
			5962-88525 15 ZX	28F	
			5962-88525 14 UX	28U	Military/883C Class B, Fully Compliant (-55°C to 125°C)
			5962-88525 14 XX	28D6	
			5962-88525 14 YX	32L	
			5962-88525 14 ZX	28F	

Package Type	
28D6	28-Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
28F	28-Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)
32J	32-Lead, Plastic J-Leaded Chip Carrier (PLCC)
32L	32-Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28-Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
28U	28-Pin, Ceramic Pin Grid Array (PGA)
W	Die
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 10 ms
E	High Endurance Option: Endurance = 100K Write Cycles
F	Fast Write Option: Write Time = 3 ms

Ordering Information[2]

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
150[3]	50	0.35	5962-88525 08 UX	28U	Military/883C Class B, Fully Compliant (-55°C to 125°C)
			5962-88525 08 XX	28D6	
			5962-88525 08 YX	32L	
			5962-88525 08 ZX	28F	
			5962-88525 07 UX	28U	Military/883C Class B, Fully Compliant (-55°C to 125°C)
			5962-88525 07 XX	28D6	
			5962-88525 07 YX	32L	
			5962-88525 07 ZX	28F	
			5962-88525 06 UX	28U	Military/883C Class B, Fully Compliant (-55°C to 125°C)
			5962-88525 06 XX	28D6	
			5962-88525 06 YX	32L	
			5962-88525 06 ZX	28F	
200[3]	50	0.35	5962-88525 12 UX	28U	Military/883C Class B, Fully Compliant (-55°C to 125°C)
			5962-88525 12 XX	28D6	
			5962-88525 12 YX	32L	
			5962-88525 12 ZX	28F	
	50	0.35	5962-88525 04 UX	28U	Military/883C Class B, Fully Compliant (-55°C to 125°C)
			5962-88525 04 XX	28D6	
			5962-88525 04 YX	32L	
			5962-88525 04 ZX	28F	
250[3]	50	0.35	5962-88525 13 UX	28U	Military/883C Class B, Fully Compliant (-55°C to 125°C)
			5962-88525 13 XX	28D6	
			5962-88525 13 YX	32L	
			5962-88525 13 ZX	28F	
			5962-88525 11 UX	28U	Military/883C Class B, Fully Compliant (-55°C to 125°C)
			5962-88525 11 XX	28D6	
			5962-88525 11 YX	32L	
			5962-88525 11 ZX	28F	

Package Type	
28D6	28-Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
28F	28-Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)
32L	32-Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
28U	28-Pin, Ceramic Pin Grid Array (PGA)
W	Die
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 10 ms
E	High Endurance Option: Endurance = 100K Write Cycles
F	Fast Write Option: Write Time = 3 ms

Ordering Information[2]

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
250	50	0.35	5962-88525 05 UX	28U	Military/883C
			5962-88525 05 XX	28D6	Class B, Fully Compliant
			5962-88525 05 YX	32L	(-55°C to 125°C)
			5962-88525 05 ZX	28F	
			5962-88525 03 UX	28U	Military/883C
			5962-88525 03 XX	28D6	Class B, Fully Compliant
			5962-88525 03 YX	32L	(-55°C to 125°C)
			5962-88525 03 ZX	28F	
300	50	0.35	5962-88525 10 UX	28U	Military/883C
			5962-88525 10 XX	28D6	Class B, Fully Compliant
			5962-88525 10 YX	32L	(-55°C to 125°C)
			5962-88525 10 ZX	28F	
	50	0.35	5962-88525 02 UX	28U	Military/883C
			5962-88525 02 XX	28D6	Class B, Fully Compliant
			5962-88525 02 YX	32L	(-55°C to 125°C)
			5962-88525 02 ZX	28F	
350	50	0.35	5962-88525 09 UX	28U	Military/883C
			5962-88525 09 XX	28D6	Class B, Fully Compliant
			5962-88525 09 YX	32L	(-55°C to 125°C)
			5962-88525 09 ZX	28F	
	50	0.35	5962-88525 01 UX	28U	Military/883C
			5962-88525 01 XX	28D6	Class B, Fully Compliant
			5962-88525 01 YX	32L	(-55°C to 125°C)
			5962-88525 01 ZX	28F	

Notes: 1. Electrical specifications for these speeds are defined by Standard Microcircuit Drawing 5962-88525.

2. See Valid Part Numbers table below.

3. SMD specifies Software Data Protection feature for device type, although Atmel product supplied to *every* device type in the SMD is 100% tested for this feature.

Package Type	
28D6	28-Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
28F	28-Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)
32L	32-Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
28U	28-Pin, Ceramic Pin Grid Array (PGA)
W	Die
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 10 ms
E	High Endurance Option: Endurance = 100K Write Cycles
F	Fast Write Option: Write Time = 3 ms

Valid Part Numbers

The following table lists standard Atmel products that can be ordered.

Device Numbers	Speed	Package and Temperature Combinations
AT28C256	15	JC, JI, PC, PI, SC, SI, TC, TI, DM/883, FM/883, LM/883, UM/883
AT28C256E	15	JC, JI, PC, PI, SC, SI, TC, TI, DM/883, FM/883, LM/883, UM/883
AT28C256F	15	JC, JI, PC, PI, SC, SI, TC, TI, DM/883, FM/883, LM/883, UM/883
AT28C256	20	JC, JI, PC, PI, SC, SI, TC, TI, DM/883, FM/883, LM/883, UM/883
AT28C256E	20	JC, JI, PC, PI, SC, SI, TC, TI, DM/883, FM/883, LM/883, UM/883
AT28C256F	20	JC, JI, PC, PI, SC, SI, TC, TI, DM/883, FM/883, LM/883, UM/883
AT28C256	25	JC, JI, PC, PI, SC, SI, TC, TI, DM/883, FM/883, LM/883, UM/883
AT28C256E	25	JC, JI, PC, PI, SC, SI, TC, TI, DM/883, FM/883, LM/883, UM/883
AT28C256F	25	JC, JI, PC, PI, SC, SI, TC, TI, DM/883, FM/883, LM/883, UM/883
AT28C256	-	W

Die Products

Reference Section: Parallel EEPROM Die Products

Features

- Fast Read Access Time - 120 ns
- Automatic Page Write Operation
  - Internal Address and Data Latches for 128 Bytes
  - Internal Control Timer
- Fast Write Cycle Time
  - Page Write Cycle Time - 10 ms Maximum
  - 1 to 128-Byte Page Write Operation
- Low Power Dissipation
  - 40 mA Active Current
  - 200 µA CMOS Standby Current
- Hardware and Software Data Protection
- $\overline{\text{DATA}}$ Polling for End of Write Detection
- High Reliability CMOS Technology
  - Endurance: 10^4 or 10^5 Cycles
  - Data Retention: 10 Years
- Single 5V ± 10% Supply
- CMOS and TTL Compatible Inputs and Outputs
- JEDEC Approved Byte-Wide Pinout
- Commercial and Industrial Temperature Ranges

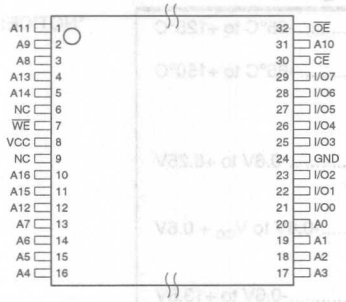
Description

The AT28C010 is a high-performance Electrically Erasable and Programmable Read Only Memory. Its 1 megabit of memory is organized as 131,072 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 120 ns with power dissipation of just 220 mW. When the device is deselected, the CMOS standby current is less than 200 µA. *(continued)*

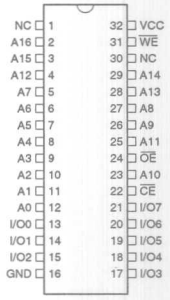
Pin Configurations

Pin Name	Function
A0 - A16	Addresses
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect
DC	Don't Connect

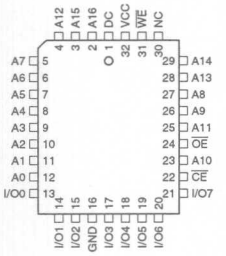
TSOP
Top View



PDIP
Top View



PLCC
Top View



Note: PLCC package pins 1 and 17 are DON'T CONNECT.

1-Megabit (128K x 8) Paged Parallel EEPROMs

AT28C010 Commercial / Industrial

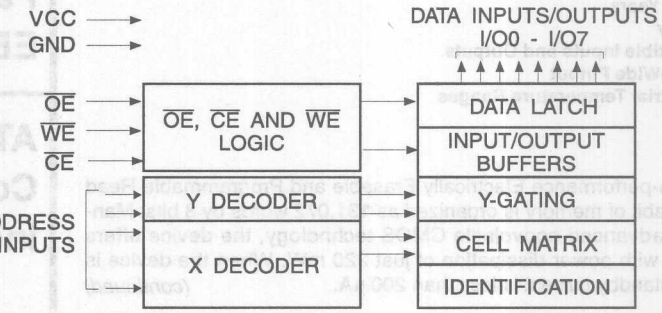
3

Rev. 0353D–10/98

The AT28C010 is accessed like a Static RAM for the read or write cycle without the need for external components. The device contains a 128-byte page register to allow writing of up to 128 bytes simultaneously. During a write cycle, the address and 1 to 128 bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by $\overline{\text{DATA}}$ POLLING of I/O_7. Once the end of a write cycle has been detected a new access for a read or write can begin.

Atmel's 28C010 has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and improved data retention characteristics. An optional software data protection mechanism is available to guard against inadvertent writes. The device also includes an extra 128 bytes of EEPROM for device identification or tracking.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V
Voltage on $\overline{\text{OE}}$ and A9 with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Device Operation

READ: The AT28C010 is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state when either $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention in their system.

BYTE WRITE: A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high initiates a write cycle. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Once a byte write has been started it will automatically time itself to completion. Once a programming operation has been initiated and for the duration of t_{WC}, a read operation will effectively be a polling operation.

PAGE WRITE: The page write operation of the AT28C010 allows 1 to 128 bytes of data to be written into the device during a single internal programming period. A page write operation is initiated in the same manner as a byte write; the first byte written can then be followed by 1 to 127 additional bytes. Each successive byte must be written within 150 µs (t_{BLC}) of the previous byte. If the t_{BLC} limit is exceeded the AT28C010 will cease accepting data and commence the internal programming operation. All bytes during a page write operation must reside on the same page as defined by the state of the A7 - A16 inputs. For each $\overline{WE}$ high to low transition during the page write operation, A7 - A16 must be the same.

The A0 to A6 inputs are used to specify which bytes within the page are to be written. The bytes may be loaded in any order and may be altered within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

$\overline{DATA}$ POLLING: The AT28C010 features $\overline{DATA}$ Polling to indicate the end of a write cycle. During a byte or page write cycle an attempted read of the last byte written will result in the complement of the written data to be presented on I/O_7. Once the write cycle has been completed, true data is valid on all outputs, and the next write cycle may begin. $\overline{DATA}$ Polling may begin at anytime during the write cycle.

TOGGLE BIT: In addition to $\overline{DATA}$ Polling the AT28C010 provides another method for determining the end of a write cycle. During the write operation, successive attempts to read data from the device will result in I/O_6 toggling between one and zero. Once the write has completed, I/O_6 will stop toggling and valid data will be read. Reading the toggle bit may begin at any time during the write cycle.

DATA PROTECTION: If precautions are not taken, inadvertent writes may occur during transitions of the host system power supply. Atmel has incorporated both hardware and software features that will protect the memory against inadvertent writes.

HARDWARE PROTECTION: Hardware features protect against inadvertent writes to the AT28C010 in the following ways: (a) V_{CC} sense—if V_{CC} is below 3.8V (typical) the write function is inhibited; (b) V_{CC} power-on delay—once V_{CC} has reached 3.8V the device will automatically time out 5 ms (typical) before allowing a write; (c) write inhibit—holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits write cycles; and (d) noise filter—pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a write cycle.

SOFTWARE DATA PROTECTION: A software controlled data protection feature has been implemented on the AT28C010. When enabled, the software data protection (SDP), will prevent inadvertent writes. The SDP feature may be enabled or disabled by the user; the AT28C010 is shipped from Atmel with SDP disabled.

SDP is enabled by the host system issuing a series of three write commands; three specific bytes of data are written to three specific addresses (refer to Software Data Protection Algorithm). After writing the 3-byte command sequence and after t_{WC} the entire AT28C010 will be protected against inadvertent write operations. It should be noted, that once protected the host may still perform a byte or page write to the AT28C010. This is done by preceding the data to be written by the same 3-byte command sequence used to enable SDP.

Once set, SDP will remain active unless the disable command sequence is issued. Power transitions do not disable SDP and SDP will protect the AT28C010 during power-up and power-down conditions. All command sequences must conform to the page write timing specifications. The data in the enable and disable command sequences is not written to the device and the memory addresses used in the sequence may be written with data in either a byte or page write operation.

After setting SDP, any attempt to write to the device without the 3-byte command sequence will start the internal write timers. No data will be written to the device; however, for the duration of t_{WC}, read operations will effectively be polling operations.

DEVICE IDENTIFICATION: An extra 128 bytes of EEPROM memory are available to the user for device identification. By raising A9 to 12V ± 0.5V and using address locations 1FF80H to 1FFFFH the bytes may be written to or read from in the same manner as the regular memory array.

OPTIONAL CHIP ERASE MODE: The entire device can be erased using a 6-byte software code. Please see Software Chip Erase application note for details.

DC and AC Operating Range

		AT28C010-12	AT28C010-15	AT28C010-20
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		5V ± 10%	5V ± 10%	5V ± 10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write[2]	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X[1]	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to AC Programming Waveforms.

DC Characteristics

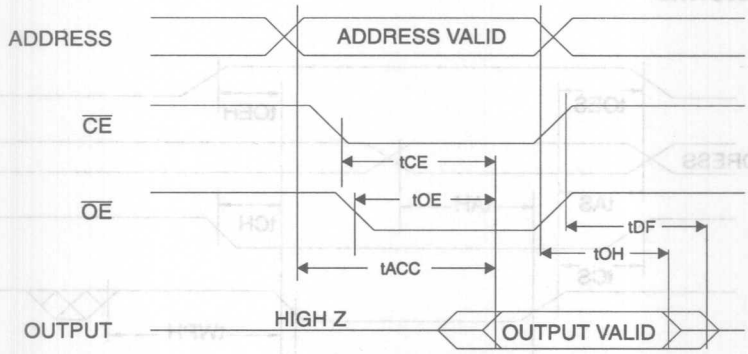
Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC} + 1V		10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}		10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3V to V_{CC} + 1V		200	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V to V_{CC} + 1V		3	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz; I_{OUT} = 0 mA		40	mA
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage		2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.45	V
V_{OH1}	Output High Voltage	I_{OH} = -400 µA	2.4		V
V_{OH2}	Output High Voltage CMOS	I_{OH} = -100 µA; V_{CC} = 4.5V	4.2		V

AC Read Characteristics

Symbol	Parameter	AT28C010-12		AT28C010-15		AT28C010-20		Units
		Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		120		150		200	ns
t_{CE}[1]	$\overline{CE}$ to Output Delay		120		150		200	ns
t_{OE}[2]	$\overline{OE}$ to Output Delay	0	50	0	55	0	55	ns
t_{DF}[3][4]	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	50	0	55	0	55	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		ns

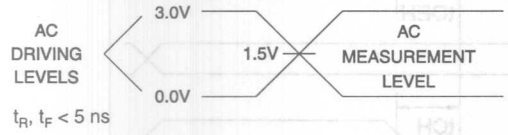
3

AC Read Waveforms[1][2][3][4]

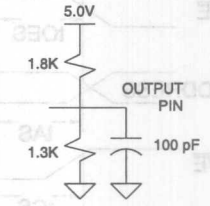


Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



Output Test Load



Pin Capacitance

f = 1 MHz, T = 25°C[1]

Symbol	Typ	Max	Units	Conditions
C_{IN}	4	10	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

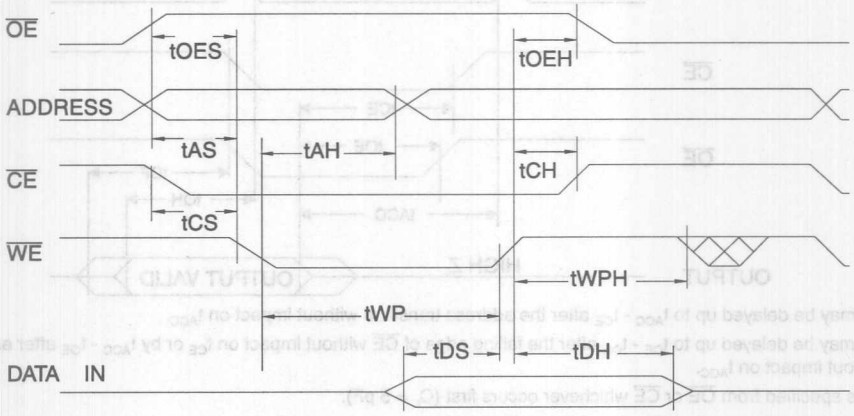
Note: 1. This parameter is characterized and is not 100% tested.

AC Write Characteristics

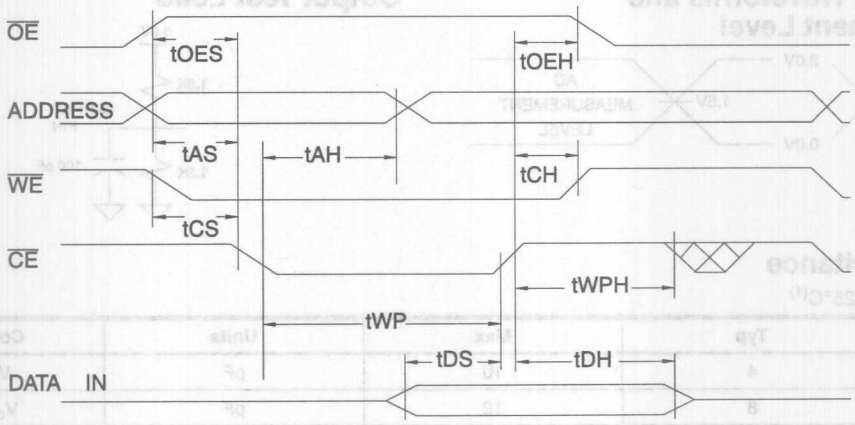
Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	100		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	0		ns

AC Write Waveforms

$\overline{WE}$ Controlled



$\overline{CE}$ Controlled

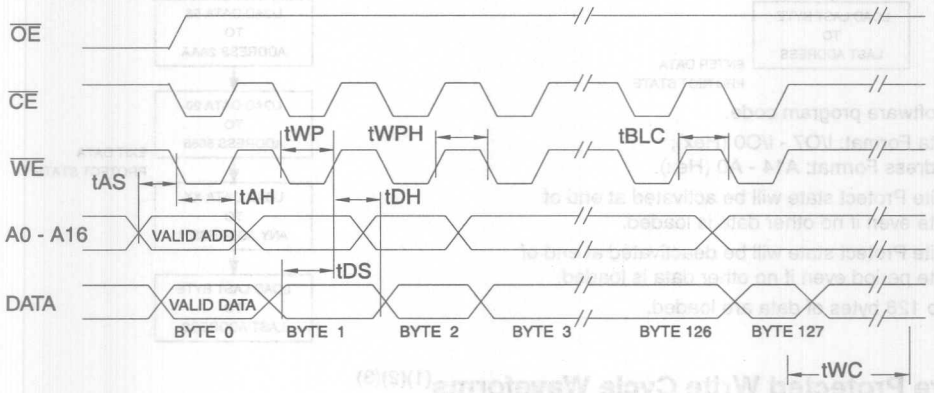


Page Mode Characteristics

Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time		10	ms
t_{AS}	Address Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}	Data Hold Time	0		ns
t_{WP}	Write Pulse Width	100		ns
t_{BLC}	Byte Load Cycle Time		150	µs
t_{WPH}	Write Pulse Width High	50		ns

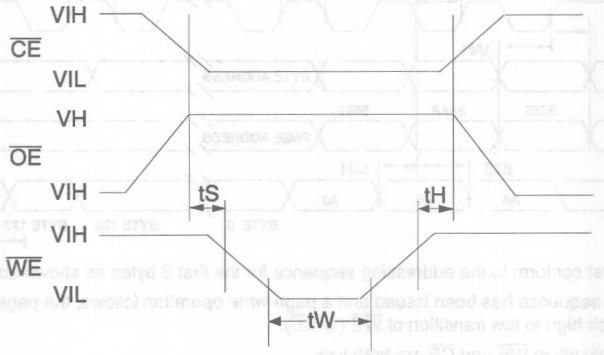
3

Page Mode Write Waveforms(1)(2)



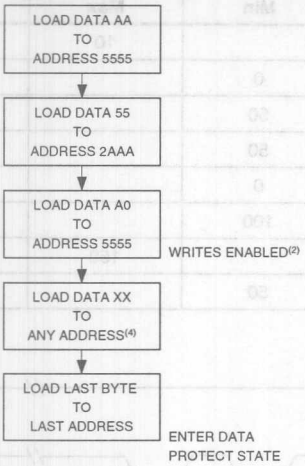
Notes: 1. A7 through A16 must specify the same page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
2. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

Chip Erase Waveforms

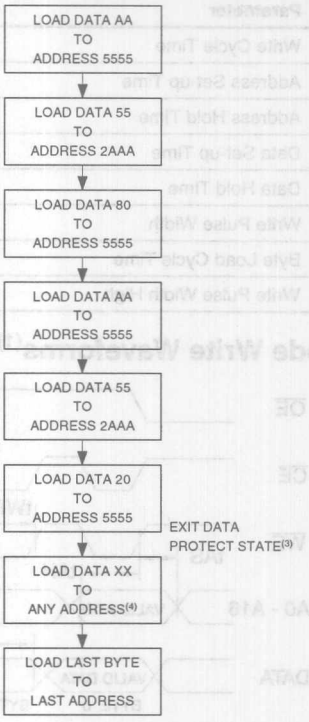


t_S = 5 µsec (min.)
$t_W = t_H$ = 10 msec (min.)
V_H = 12.0V ± 0.5V

Software Data Protection Enable Algorithm[1]



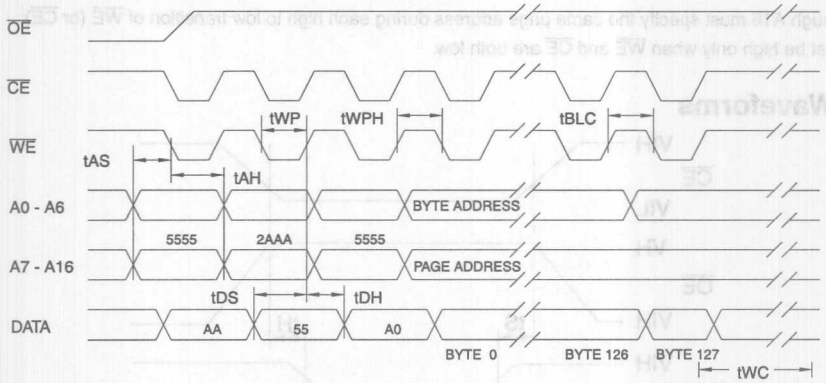
Software Data Protection Disable Algorithm[1]



Notes for software program code:

1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Write Protect state will be activated at end of write even if no other data is loaded.
3. Write Protect state will be deactivated at end of write period even if no other data is loaded.
4. 1 to 128 bytes of data are loaded.

Software Protected Write Cycle Waveforms[1][2][3]



Notes: 1. A0 through A14 must conform to the addressing sequence for the first 3 bytes as shown above.

2. After the command sequence has been issued and a page write operation follows, the page address inputs (A7 - A16) must be the same for each high to low transition of $\overline{WE}$ (or $\overline{CE}$).

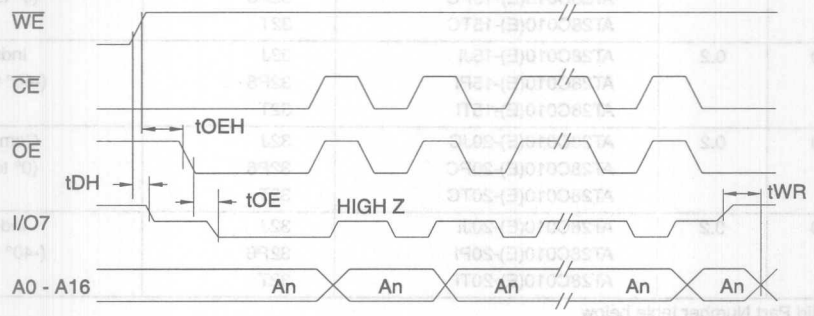
3. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

Data Polling Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay[2]				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See AC Read Characteristics.

Data Polling Waveforms

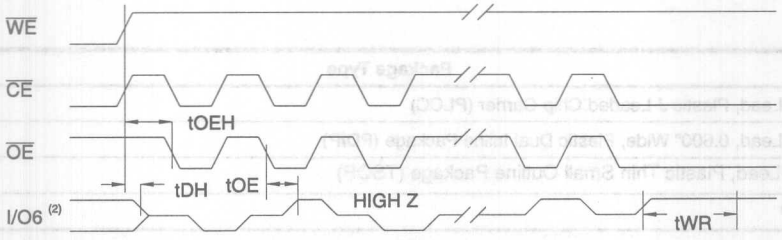


Toggle Bit Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay[2]				ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See AC Read Characteristics.

Toggle Bit Waveforms



Notes: 1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

Ordering Information[1]

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
120	40	0.2	AT28C010(E)-12JC	32J	Commercial
			AT28C010(E)-12PC	32P6	(0° to 70°C)
			AT28C010(E)-12TC	32T	
	40	0.2	AT28C010(E)-12JI	32J	Industrial
			AT28C010(E)-12PI	32P6	(-40° to 85°C)
			AT28C010(E)-12TI	32T	
150	40	0.2	AT28C010(E)-15JC	32J	Commercial
			AT28C010(E)-15PC	32P6	(0° to 70°C)
			AT28C010(E)-15TC	32T	
	40	0.2	AT28C010(E)-15JI	32J	Industrial
			AT28C010(E)-15PI	32P6	(-40° to 85°C)
			AT28C010(E)-15TI	32T	
200	40	0.2	AT28C010(E)-20JC	32J	Commercial
			AT28C010(E)-20PC	32P6	(0° to 70°C)
			AT28C010(E)-20TC	32T	
	40	0.2	AT28C010(E)-20JI	32J	Industrial
			AT28C010(E)-20PI	32P6	(-40° to 85°C)
			AT28C010(E)-20TI	32T	

Note: 1. See Valid Part Number table below.

Package Type	
32J	32-Lead, Plastic J-Leaded Chip Carrier (PLCC)
32P6	32-Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
32T	32-Lead, Plastic Thin Small Outline Package (TSOP)
W	Die
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 10 ms
E	High Endurance Option: Endurance = 100K Write Cycles

Valid Part Numbers

The following table lists standard Atmel products that can be ordered.

Device Numbers	Speed	Package and Temperature Combinations
AT28C010	12	JC, JI, PC, PI, TC, TI
AT28C010E	12	JC, JI, PC, PI, TC, TI
AT28C010	15	JC, JI, PC, PI, TC, TI
AT28C010E	15	JC, JI, PC, PI, TC, TI
AT28C010	20	JC, JI, PC, PI, TC, TI
AT28C010E	20	JC, JI, PC, PI, TC, TI
AT28C010	-	W

Die Products

Reference Section: Parallel EEPROM Die Products

Valid Part Numbers

The following table lists standard Atmel products that can be ordered.

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AT28C010	20	JC, JI, PC, PI, TC, TI
AT28C010E	20	JC, JI, PC, PI, TC, TI
AT28C010	-	W

Die Products

Reference Section: Parallel EEPROM Die Products

Features

- Fast Read Access Time - 120 ns
- Automatic Page Write Operation
  - Internal Address and Data Latches for 128-Bytes
  - Internal Control Timer
- Fast Write Cycle Time
  - Page Write Cycle Time - 10 ms Maximum
  - 1 to 128-Byte Page Write Operation
- Low Power Dissipation
  - 80 mA Active Current
  - 300 µA CMOS Standby Current
- Hardware and Software Data Protection
- $\overline{\text{DATA}}$ Polling for End of Write Detection
- High Reliability CMOS Technology
  - Endurance: 10^4 or 10^5 Cycles
  - Data Retention: 10 Years
- Single 5V ± 10% Supply
- CMOS and TTL Compatible Inputs and Outputs
- JEDEC Approved Byte-Wide Pinout

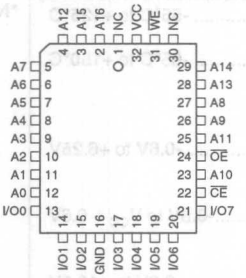
Description

The AT28C010 is a high-performance Electrically Erasable and Programmable Read Only Memory. Its one megabit of memory is organized as 131,072 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 120 ns with power dissipation of just 440 mW. When the device is deselected, the CMOS standby current is less than 300 µA. *(continued)*

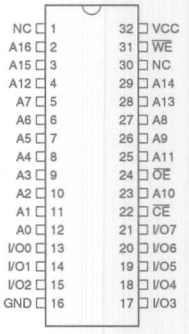
Pin Configuration

Pin Name	Function
A0 - A16	Addresses
CE	Chip Enable
OE	Output Enable
WE	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect

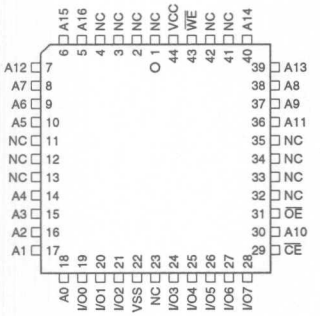
32 LCC
Top View



CERDIP, FLATPACK
Top View



44 LCC
Top View



PGA
Top View

4 A6	3 A7	1 A14	27 WE	26 A13
5 A5	2 A12	28 VCC	24 A9	25 A8
7 A3	6 A4	29 A15	22 OE	23 A11
9 A1	8 A2	30 A16	20 CE	21 A10
11 I/O0	10 A0	14 GND	16 I/O4	19 I/O7
12 I/O1	13 I/O2	15 I/O3	17 I/O5	18 I/O6

1-Megabit (128K x 8) Paged Parallel EEPROMs

AT28C010 Military

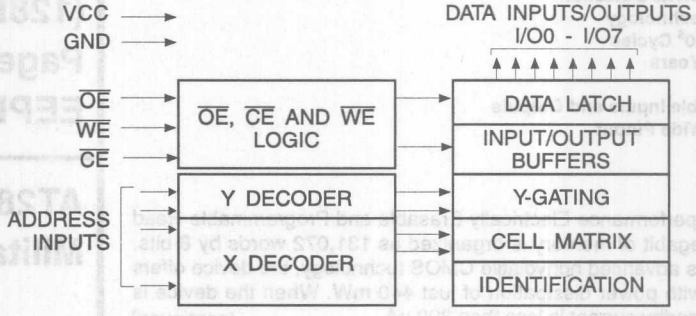
3

Rev. 0010C–10/98

The AT28C010 is accessed like a Static RAM for the read or write cycle without the need for external components. The device contains a 128-byte page register to allow writing of up to 128-bytes simultaneously. During a write cycle, the address and 1 to 128-bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by $\overline{\text{DATA}}$ POLLING of I/O7. Once the end of a write cycle has been detected a new access for a read or write can begin.

Atmel's 28C010 has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and improved data retention characteristics. An optional software data protection mechanism is available to guard against inadvertent writes. The device also includes an extra 128-bytes of EEPROM for device identification or tracking.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V
Voltage on $\overline{\text{OE}}$ and A9 with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Device Operation

READ: The AT28C010 is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state when either $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention in their system.

BYTE WRITE: A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high initiates a write cycle. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Once a byte write has been started it will automatically time itself to completion. Once a programming operation has been initiated and for the duration of t_{WC}, a read operation will effectively be a polling operation.

PAGE WRITE: The page write operation of the AT28C010 allows 1 to 128-bytes of data to be written into the device during a single internal programming period. A page write operation is initiated in the same manner as a byte write; the first byte written can then be followed by 1 to 127 additional bytes. Each successive byte must be written within 150 µs (t_{BLC}) of the previous byte. If the t_{BLC} limit is exceeded the AT28C010 will cease accepting data and commence the internal programming operation. All bytes during a page write operation must reside on the same page as defined by the state of the A7 - A16 inputs. For each $\overline{WE}$ high to low transition during the page write operation, A7 - A16 must be the same.

The A0 to A6 inputs are used to specify which bytes within the page are to be written. The bytes may be loaded in any order and may be altered within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

$\overline{DATA}$ POLLING: The AT28C010 features $\overline{DATA}$ Polling to indicate the end of a write cycle. During a byte or page write cycle an attempted read of the last byte written will result in the complement of the written data to be presented on I/O7. Once the write cycle has been completed, true data is valid on all outputs, and the next write cycle may begin. $\overline{DATA}$ Polling may begin at anytime during the write cycle.

TOGGLE BIT: In addition to $\overline{DATA}$ Polling the AT28C010 provides another method for determining the end of a write cycle. During the write operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the write has completed, I/O6 will stop toggling and valid data will be read. Reading the toggle bit may begin at any time during the write cycle.

DATA PROTECTION: If precautions are not taken, inadvertent writes may occur during transitions of the host system power supply. Atmel has incorporated both hardware and software features that will protect the memory against inadvertent writes.

HARDWARE PROTECTION: Hardware features protect against inadvertent writes to the AT28C010 in the following ways: (a) V_{CC} sense - if V_{CC} is below 3.8V (typical) the write function is inhibited; (b) V_{CC} power-on delay - once V_{CC} has reached 3.8V the device will automatically time out 5 ms (typical) before allowing a write: (c) write inhibit - holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits write cycles; (d) noise filter - pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a write cycle.

SOFTWARE DATA PROTECTION: A software controlled data protection feature has been implemented on the AT28C010. When enabled, the software data protection (SDP), will prevent inadvertent writes. The SDP feature may be enabled or disabled by the user; the AT28C010 is shipped from Atmel with SDP disabled.

SDP is enabled by the host system issuing a series of three write commands; three specific bytes of data are written to three specific addresses (refer to Software Data Protection Algorithm). After writing the 3-byte command sequence and after t_{WC} the entire AT28C010 will be protected against inadvertent write operations. It should be noted, that once protected the host may still perform a byte or page write to the AT28C010. This is done by preceding the data to be written by the same 3-byte command sequence used to enable SDP.

Once set, SDP will remain active unless the disable command sequence is issued. Power transitions do not disable SDP and SDP will protect the AT28C010 during power-up and power-down conditions. All command sequences must conform to the page write timing specifications. The data in the enable and disable command sequences is not written to the device and the memory addresses used in the sequence may be written with data in either a byte or page write operation.

After setting SDP, any attempt to write to the device without the 3-byte command sequence will start the internal write timers. No data will be written to the device; however, for the duration of t_{WC}, read operations will effectively be polling operations.

DEVICE IDENTIFICATION: An extra 128-bytes of EEPROM memory are available to the user for device identification. By raising A9 to 12V ± 0.5V and using address locations 1FF80H to 1FFFFH the bytes may be written to or read from in the same manner as the regular memory array.

OPTIONAL CHIP ERASE MODE: The entire device can be erased using a 6-byte software code. Please see Software Chip Erase application note for details.

DC and AC Operating Range

		AT28C010-12	AT28C010-15	AT28C010-20	AT28C010-25
Operating Temperature (Case)	Mil.	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%

Operating Modes

Mode	CE	OE	WE	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write (2)	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X (1)	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z

Notes: 1. X can be VIL or VIH.
2. Refer to AC Programming Waveforms

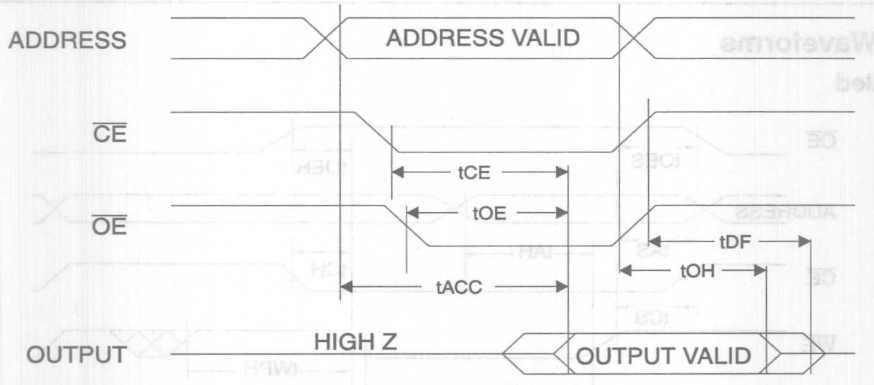
DC Characteristics

Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC} + 1V		10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}		10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3V to V_{CC} + 1V		300	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V to V_{CC} + 1V		3	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz; I_{OUT} = 0 mA		80	mA
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage		2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.45	V
V_{OH1}	Output High Voltage	I_{OH} = -400 µA	2.4		V
V_{OH2}	Output High Voltage CMOS	I_{OH} = -100 µA; V_{CC} = 4.5V	4,2		V

AC Read Characteristics

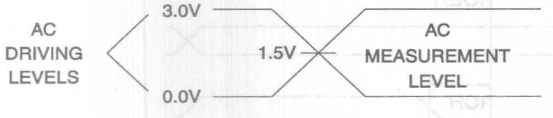
Symbol	Parameter	AT28C010-12		AT28C010-15		AT28C010-20		AT28C010-25		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		120		150		200		250	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		120		150		200		250	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay	0	50	0	55	0	55	0	55	ns
t_{DF} (3, 4)	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	50	0	55	0	55	0	55	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		0		ns

AC Read Waveforms(1)(2)(3)(4)

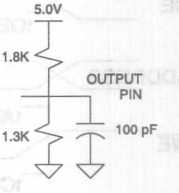


Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact in t_{ACC}.
3. t_{DF} is specified from OE or CE wichever occurs first (CL = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



Output Test Load



Pin Capacitance

f = 1 MHz, T = 25°C(1)

Symbol	Typ	Max	Units	Conditions
C_{IN}	4	10	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

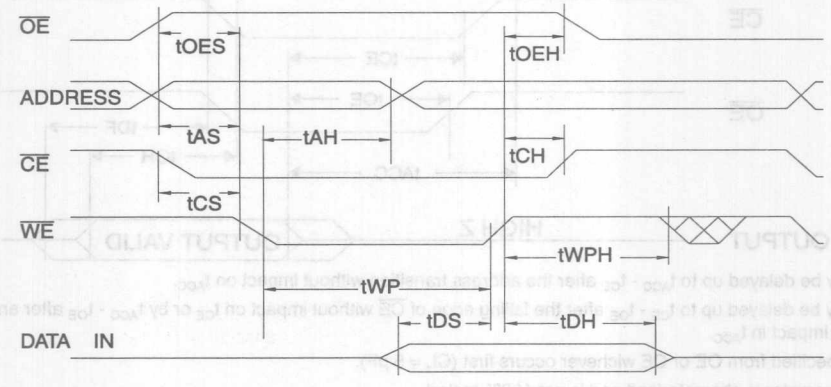
Note: 1. This parameter is 100% characterized and is not 100% tested.

AC Write Characteristics

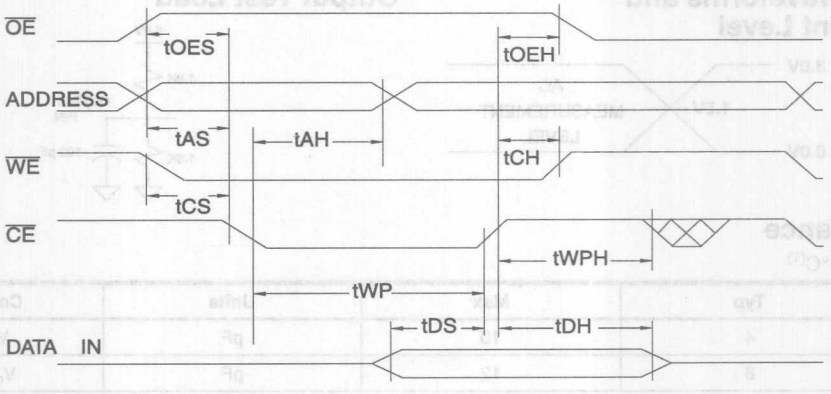
Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time		10	ms
t_{AS}	Address Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}	Data Hold Time	0		ns
t_{WP}	Write Pulse Width	100		ns
t_{BLC}	Byte Load Cycle Time		150	µs
t_{WPH}	Write Pulse Width High	50		ns

AC Write Waveforms

$\overline{WE}$ Controlled



$\overline{CE}$ Controlled

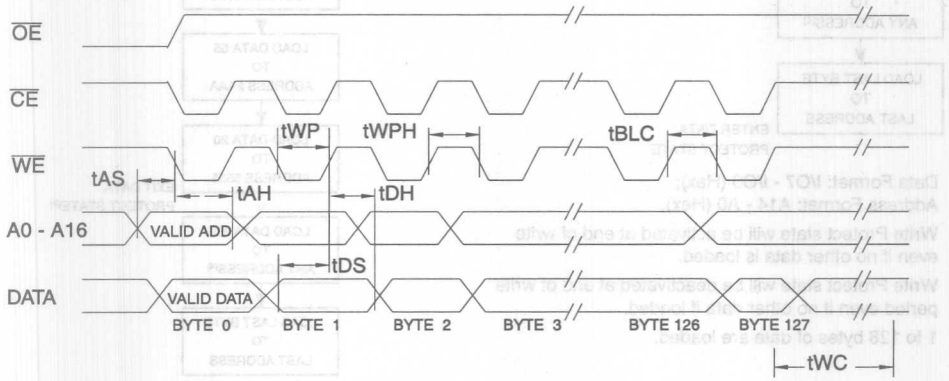


Page Mode Characteristics

Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	100		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	0		ns

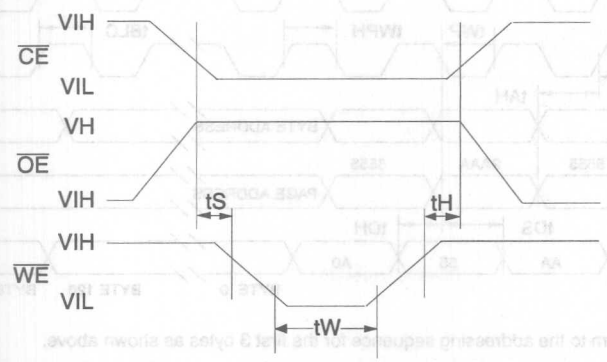
3

Page Mode Write Waveforms (1)(2)



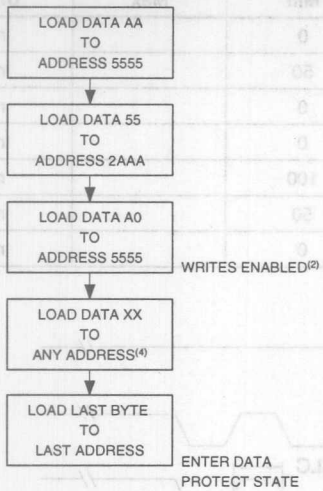
Notes: 1. A7 through A16 must specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
2. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

Chip Erase Waveforms

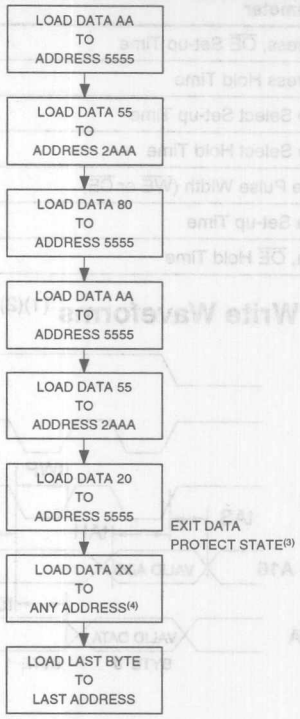


t_S = 5 msec (min.)
$t_W = t_H$ = 10 msec (min.)
V_H = 12.0V ± 0.5V

Software Data Protection Enable Algorithm[1]

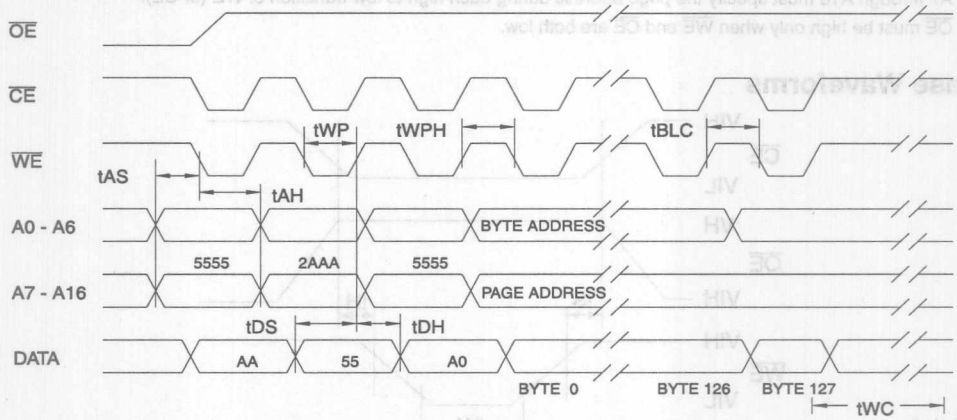


Software Data Protection Disable Algorithm[1]



Notes:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Write Protect state will be activated at end of write even if no other data is loaded.
3. Write Protect state will be deactivated at end of write period even if no other data if loaded.
4. 1 to 128 bytes of data are loaded.

Software Protected Program Cycle Waveform[1][2][3]



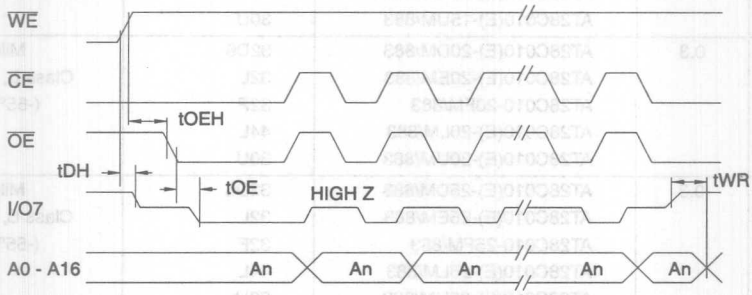
Notes:
1. A0 - A14 must conform to the addressing sequence for the first 3 bytes as shown above.
2. After the command sequence has been issued and a page write operation follows, the page address inputs (A7 - A16) must be the same for each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
3. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

$\overline{\text{Data}}$ Polling Characterstics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay [2]				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See AC Read Characteristics.

$\overline{\text{Data}}$ Polling Waveforms

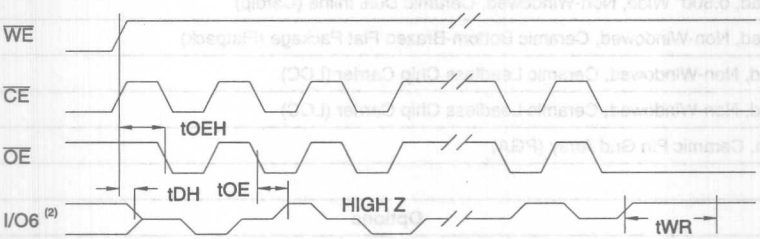


Toggle Bit Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay [2]				ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See AC Read Characteristics.

Toggle Bit Waveforms[1][2][3]



Notes: 1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any addres location may be used but the address should not vary.

AT28C010 Ordering Information[1]

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
120	80	0.3	AT28C010(E)-12DM/883	32D6	Military/883C
			AT28C010(E)-12EM/883	32L	Class B, Fully Compliant
			AT28C010-12FM/883	32F	(-55°C to 125°C)
			AT28C010(E)-12LM/883	44L	
			AT28C010(E)-12UM/883	30U	
150	80	0.3	AT28C010(E)-15DM/883	32D6	Military/883C
			AT28C010(E)-15EM/883	32L	Class B, Fully Compliant
			AT28C010-15FM/883	32F	(-55°C to 125°C)
			AT28C010(E)-15LM/883	44L	
			AT28C010(E)-15UM/883	30U	
200	80	0.3	AT28C010(E)-20DM/883	32D6	Military/883C
			AT28C010(E)-20EM/883	32L	Class B, Fully Compliant
			AT28C010-20FM/883	32F	(-55°C to 125°C)
			AT28C010(E)-20LM/883	44L	
			AT28C010(E)-20UM/883	30U	
250	80	0.3	AT28C010(E)-25DM/883	32D6	Military/883C
			AT28C010(E)-25EM/883	32L	Class B, Fully Compliant
			AT28C010-25FM/883	32F	(-55°C to 125°C)
			AT28C010(E)-25LM/883	44L	
			AT28C010(E)-25UM/883	30U	

Note: 1. See Valid Part Number table below.

Package Type	
32D6	32-Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline (Cerdip)
32F	32-Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)
32L	32-Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
44L	44-Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
30U	30-Pin, Ceramic Pin Grid Array (PGA)
W	Die
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 10 ms
E	High Endurance Option: Endurance = 100K Write Cycles

5962-38267 Ordering Information[1]

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
120	80	0.3	5962-38267 07 MXX	32D6	Military/883C
			5962-38267 07 MZX	32F	Class B, Fully Compliant
			5962-38267 07 MYX	44L	(-55°C to 125°C)
			5962-38267 07 MTX	30U	
150	80	0.3	5962-38267 05 MXX	32D6	Military/883C
			5962-38267 05 MUX	32L	Class B, Fully Compliant
			5962-38267 05 MZX	32F	(-55°C to 125°C)
			5962-38267 05 MYX	44L	
			5962-38267 05 MTX	30U	
200	80	0.3	5962-38267 03 MXX	32D6	Military/883C
			5962-38267 03 MUX	32L	Class B, Fully Compliant
			5962-38267 03 MZX	32F	(-55°C to 125°C)
			5962-38267 03 MYX	44L	
			5962-38267 03 MTX	30U	
250	80	0.3	5962-38267 01 MXX	32D6	Military/883C
			5962-38267 01 MUX	32L	Class B, Fully Compliant
			5962-38267 01 MZX	32F	(-55°C to 125°C)
			5962-38267 01 MYX	44L	
			5962-38267 01 MTX	30U	

Note: 1. See Valid Part Number table below.

Package Type	
32D6	32-Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline (Cerdip)
32F	32-Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)
32L	32-Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
44L	44-Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
30U	30-Pin, Ceramic Pin Grid Array (PGA)
W	Die
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 10 ms
E	High Endurance Option: Endurance = 100K Write Cycles

Valid Part Numbers

The following table lists standard Atmel products that can be ordered.

Device Numbers	Speed	Package and Temperature Combinations
AT28C010	12	DM/883, EM/883, FM/883, LM/883, UM/883
AT28C010E	12	DM/883, EM/883, LM/883, UM/883
AT28C010	15	DM/883, EM/883, FM/883, LM/883, UM/883
AT28C010E	15	DM/883, EM/883, LM/883, UM/883
AT28C010	20	DM/883, EM/883, FM/883, LM/883, UM/883
AT28C010E	20	DM/883, EM/883, LM/883, UM/883
AT28C010	25	DM/883, EM/883, FM/883, LM/883, UM/883
AT28C010E	25	DM/883, EM/883, LM/883, UM/883
AT28C010	–	W

Die Products

Reference Section: Parallel EEPROM Die Products

Features

- Read Access Time - 200 ns
- Automatic Page Write Operation
  - Internal Address and Data Latches for 256 Bytes
  - Internal Control Timer
- Fast Write Cycle Time
  - Page Write Cycle Time - 10 ms Maximum
  - 1 to 256 Byte Page Write Operation
- Low Power Dissipation
  - 80 mA Active Current
- Hardware and Software Data Protection
- $\overline{\text{DATA}}$ Polling for End of Write Detection
- High Reliability CMOS Technology
  - Endurance: 10,000 Cycles
  - Data Retention: 10 Years
- Single 5V ± 10% Supply
- CMOS and TTL Compatible Inputs and Outputs
- JEDEC Approved Byte-Wide Pinout

Description

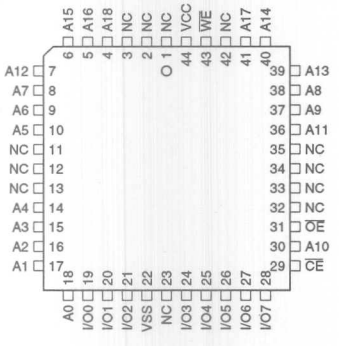
The AT28C040 is a high-performance electrically erasable and programmable read only memory (EEPROM). Its 4 megabits of memory is organized as 524,288 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 200 ns with power dissipation of just 440 mW.

(continued)

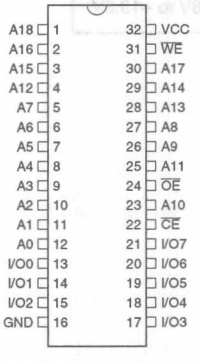
Pin Configurations

Pin Name	Function
A0 - A18	Addresses
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect

LCC
Top View



SIDE BRAZE,
FLATPACK
Top View



4-Megabit (512K x 8) Paged Parallel EEPROMs

AT28C040

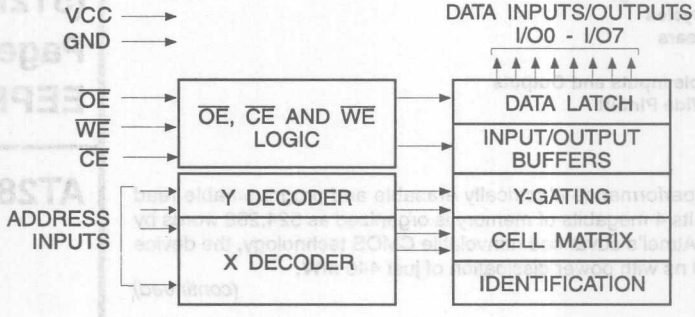
3

Rev. 0542B–10/98

The AT28C040 is accessed like a static RAM for the read or write cycle without the need for external components. The device contains a 256-byte page register to allow writing of up to 256 bytes simultaneously. During a write cycle, the address and 1 to 256 bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by $\overline{\text{DATA}}$ POLLING of I/O7. Once the end of a write cycle has been detected, a new access for a read or write can begin.

Atmel's AT28C040 has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and improved data retention characteristics. An optional software data protection mechanism is available to guard against inadvertent writes. The device also includes an extra 256 bytes of EEPROM for device identification or tracking.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V
Voltage on $\overline{\text{OE}}$ and A9 with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Device Operation

READ: The AT28C040 is accessed like a static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state when either $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention in their systems.

BYTE WRITE: A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high initiates a write cycle. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Once a byte write has been started, it will automatically time itself to completion. Once a programming operation has been initiated and for the duration of t_{WC}, a read operation will effectively be a polling operation.

PAGE WRITE: The page write operation of the AT28C040 allows 1 to 256 bytes of data to be written into the device during a single internal programming period. A page write operation is initiated in the same manner as a byte write; the first byte written can then be followed by 1 to 255 additional bytes. Each successive byte must be written within 150 µs (t_{BLC}) of the previous byte. If the t_{BLC} limit is exceeded, the AT28C040 will cease accepting data and commence the internal programming operation. All bytes during a page write operation must reside on the same page as defined by the state of the A8 - A18 inputs. For each $\overline{WE}$ high to low transition during the page write operation, A8 - A18 must be the same.

The A0 to A7 inputs specify which bytes within the page are to be written. The bytes may be loaded in any order and may be altered within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

$\overline{DATA}$ POLLING: The AT28C040 features $\overline{DATA}$ Polling to indicate the end of a write cycle. During a byte or page write cycle an attempted read of the last byte written will result in the complement of the written data to be presented on I/O7. Once the write cycle has been completed, true data is valid on all outputs, and the next write cycle may begin. $\overline{DATA}$ Polling may begin at anytime during the write cycle.

TOGGLE BIT: In addition to $\overline{DATA}$ Polling, the AT28C040 provides another method for determining the end of a write cycle. During the write operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the write has completed, I/O6 will stop toggling and valid data will be read. Reading the toggle bit may begin at any time during the write cycle.

DATA PROTECTION: If precautions are not taken, inadvertent writes may occur during transitions of the host system power supply. Atmel has incorporated both hardware and software features that will protect the memory against inadvertent writes.

HARDWARE PROTECTION: Hardware features protect against inadvertent writes to the AT28C040 in the following ways: (a) V_{CC} sense - if V_{CC} is below 3.8V (typical) the write function is inhibited; (b) V_{CC} power-on delay - once V_{CC} has reached 3.8V the device will automatically time out 5 ms (typical) before allowing a write: (c) write inhibit - holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits write cycles; (d) noise filter - pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a write cycle.

SOFTWARE DATA PROTECTION: A software controlled data protection feature has been implemented on the AT28C040. When enabled, the software data protection (SDP), will prevent inadvertent writes. The SDP feature may be enabled or disabled by the user; the AT28C040 is shipped from Atmel with SDP disabled.

SDP is enabled when the host system issues a series of three write commands; three specific bytes of data are written to three specific addresses (refer to Software Data Protection Algorithm). After writing the 3-byte command sequence and after t_{WC}, the entire AT28C040 will be protected against inadvertent write operations. It should be noted that once protected, the host can still perform a byte or page write to the AT28C040. To do so, the same 3-byte command sequence used to enable SDP must precede the data to be written.

Once set, SDP will remain active unless the disable command sequence is issued. Power transitions do not disable SDP, and SDP will protect the AT28C040 during power-up and power-down conditions. All command sequences must conform to the page write timing specifications. The data in the enable and disable command sequences is not written to the device, and the memory addresses used in the sequence may be written with data in either a byte or page write operation.

After setting SDP, any attempt to write to the device without the 3-byte command sequence will start the internal write timers. No data will be written to the device; however, for the duration of t_{WC}, read operations will effectively be polling operations.

DEVICE IDENTIFICATION: An extra 256 bytes of EEPROM memory are available to the user for device identification. By raising A9 to 12V ± 0.5V and using address locations 7FF80H to 7FFFFH, the bytes may be written to or read from in the same manner as the regular memory array.

OPTIONAL CHIP ERASE MODE: The entire device can be erased using a 6-byte software erase code. Please see Software Chip Erase application note for details.

DC and AC Operating Range

		AT28C040-20		AT28C040-25	
		Operation		Operation	
		Read	Program	Read	Program
Operating Temperature (Case)	Commercial	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Industrial	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Extended	-55°C - 125°C	-40°C - 85°C	-55°C - 125°C	-40°C - 85°C
V_{CC} Power Supply		5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write[2]	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X[1]	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to AC Programming Waveforms.

DC Characteristics

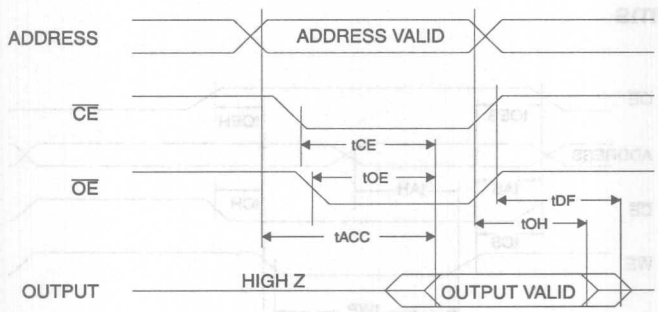
Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC} + 1V		10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}		10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3V to V_{CC} + 1V		3	mA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V to V_{CC} + 1V		3	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz; I_{OUT} = 0 mA		80	mA
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage		2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.45	V
V_{OH1}	Output High Voltage	I_{OH} = -400 µA	2.4		V
V_{OH2}	Output High Voltage CMOS	I_{OH} = -100 µA; V_{CC} = 4.5V	4.2		V

AC Read Characteristics

Symbol	Parameter	AT28C040-20		AT28C040-25		Units
		Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		200		250	ns
t_{CE}[1]	$\overline{CE}$ to Output Delay		200		250	ns
t_{OE}[2]	$\overline{OE}$ to Output Delay	0	55	0	55	ns
t_{DF}[3][4]	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	55	0	55	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		ns

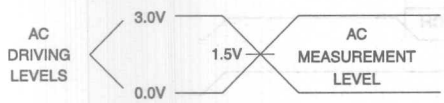
3

AC Read Waveforms[1][2][3][4]



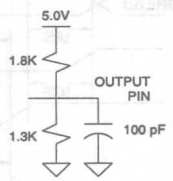
Note: 1. $\overline{CE}$ May be delayed up to $t_{ACC} - t_{CE}$ after the address transition wihtout impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 5 ns

Output Test Load



Pin Capacitance

f = 1 MHz, T = 25°C[1]

Symbol	Typ	Max	Units	Conditions
C_{IN}	4	10	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

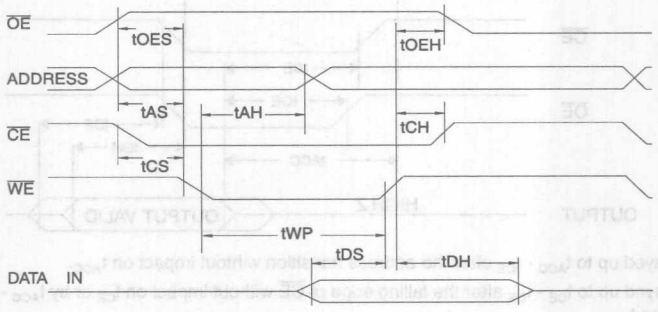
Note: 1. This parameter is characterized and is not 100% tested.

AC Write Characteristics

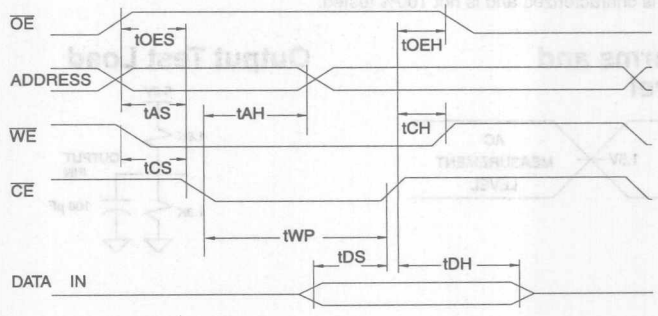
Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	100		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	0		ns

AC Write Waveforms

$\overline{WE}$ Controlled



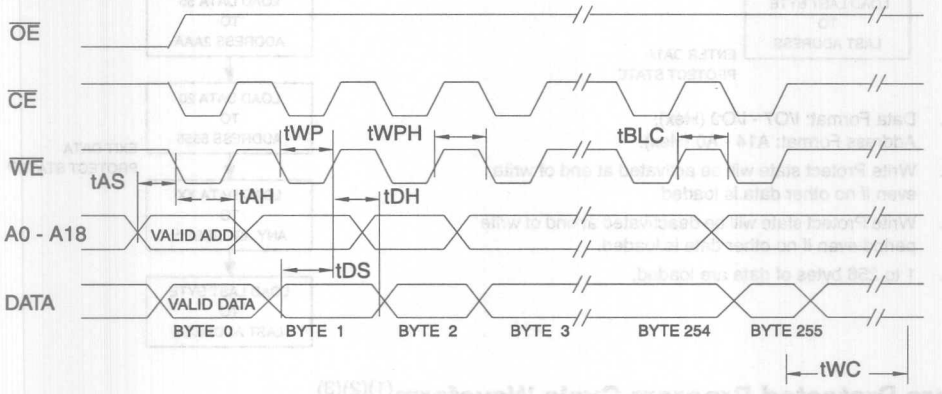
$\overline{CE}$ Controlled



Page Mode Characteristics

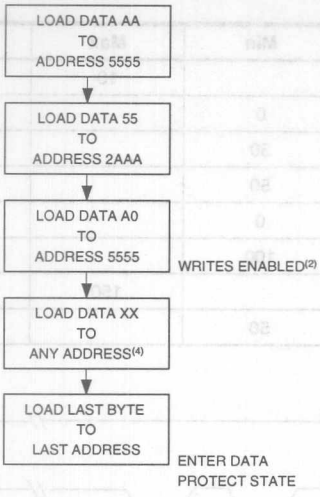
Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time		10	ms
t_{AS}	Address Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}	Data Hold Time	0		ns
t_{WP}	Write Pulse Width	100		ns
t_{BLC}	Byte Load Cycle Time		150	µs
t_{WPH}	Write Pulse Width High	50		ns

Page Mode Write Waveforms[1][2]

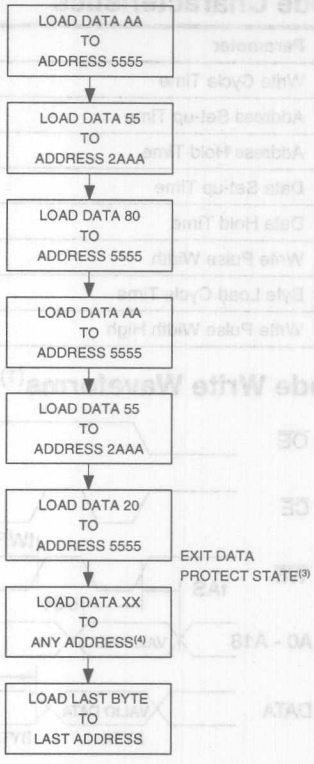


Notes: 1. A8 through A18 must specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
2. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

Software Data Protection Enable Algorithm[1]

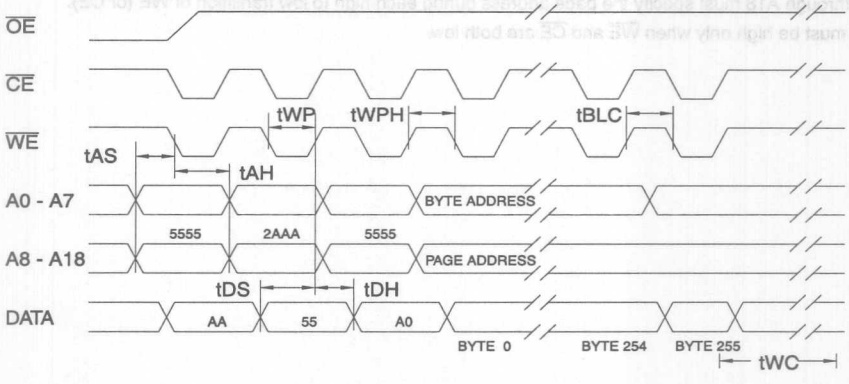


Software Data Protection Disable Algorithm[1]



Notes:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Write Protect state will be activated at end of write even if no other data is loaded.
3. Write Protect state will be deactivated at end of write period even if no other data is loaded.
4. 1 to 256 bytes of data are loaded.

Software Protected Program Cycle Waveform[1][2][3]



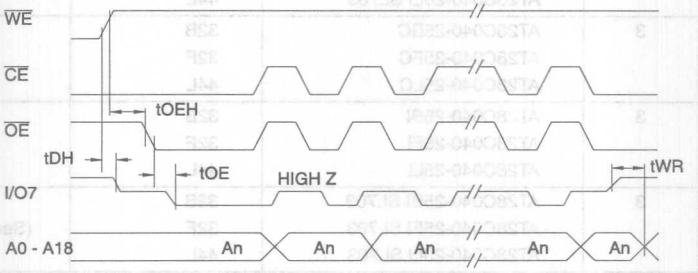
Notes:
1. A0 - A14 must conform to the addressing sequence for the first 3 bytes as shown above.
2. After the command sequence has been issued and a page write operation follows, the page address inputs (A8 - A18) must be the same for each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
3. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

$\overline{\text{Data}}$ Polling Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay[2]				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See AC Read Characteristics.

$\overline{\text{Data}}$ Polling Waveforms

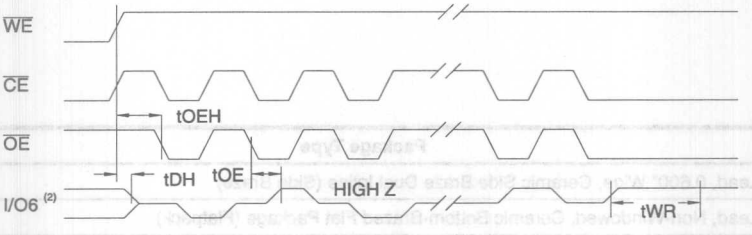


Toggle Bit Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay[2]				ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See AC Read Characteristics.

Toggle Bit Waveforms[1][2][3]



Notes: 1. Toggling either OE or CE or both OE and CE will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

Ordering Information[1]

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
200	80	3	AT28C040-20BC AT28C040-20FC AT28C040-20LC	32B 32F 44L	Commercial (0° to 70°C)
	80	3	AT28C040-20BI AT28C040-20FI AT28C040-20LI	32B 32F 44L	Industrial (-40° to 85°C)
	80	3	AT28C040-20BI SL703 AT28C040-20FI SL703 AT28C040-20LI SL703	32B 32F 44L	Extended (See DC and AC Operating Range Table)
250	80	3	AT28C040-25BC AT28C040-25FC AT28C040-25LC	32B 32F 44L	Commercial (0° to 70°C)
	80	3	AT28C040-25BI AT28C040-25FI AT28C040-25LI	32B 32F 44L	Industrial (-40° to 85°C)
	80	3	AT28C040-25BI SL703 AT28C040-25FI SL703 AT28C040-25LI SL703	32B 32F 44L	Extended (See DC and AC Operating Range Table)

Note: 1. See Valid Part Numbers.

Valid Part Numbers

The following table lists standard Atmel products that can be ordered.

Device Numbers	Speed	Package and Temperature Combinations
AT28C040	20	BC, BI, FC, FI, LC, LI, BI SL703, FI SL703, LI SL703
AT28C040	25	BC, BI, FC, FI, LC, LI, BI SL703, FI SL703, LI SL703

Die Products

Reference Section: Parallel EEPROM Die Products

Package Type	
32B	32-Lead, 0.600" Wide, Ceramic Side Braze Dual Inline (Side Braze)
32F	32-Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)
44L	44-Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 10 ms

Features

- Fast Read Access Time - 55 ns
- Automatic Page Write Operation
  - Internal Address and Data Latches for 64 Bytes
- Fast Write Cycle Times
  - Page Write Cycle Time: 10 ms Maximum
  - 1 to 64-Byte Page Write Operation
- Low Power Dissipation
  - 40 mA Active Current
  - 100 µA CMOS Standby Current
- Hardware and Software Data Protection
- $\overline{\text{DATA}}$ Polling and Toggle Bit for End of Write Detection
- High Reliability CMOS Technology
  - Endurance: 100,000 Cycles
  - Data Retention: 10 Years
- Single 5V ± 10% Supply
- CMOS and TTL Compatible Inputs and Outputs
- JEDEC Approved Byte-Wide Pinout
- Commercial and Industrial Temperature Ranges

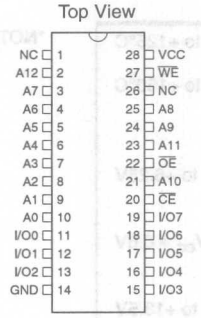
Description

The AT28HC64B is a high-performance electrically erasable and programmable read only memory (EEPROM). Its 64K of memory is organized as 8,192 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 55 ns with power dissipation of just 220 mW. When the device is deselected, the CMOS standby current is less than 100 µA. *(continued)*

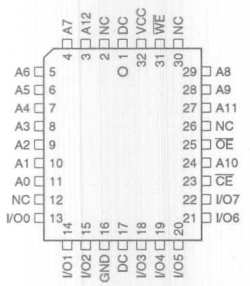
Pin Configurations

Pin Name	Function
A0 - A12	Addresses
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect
DC	Don't Connect

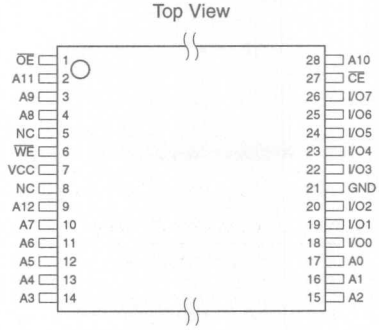
PDIP, SOIC
Top View



PLCC
Top View



TSOP
Top View



Note: PLCC package pins 1 and 17 are DON'T CONNECT.

64K (8K x 8) High Speed Parallel EEPROMs with Page Write and Software Data Protection

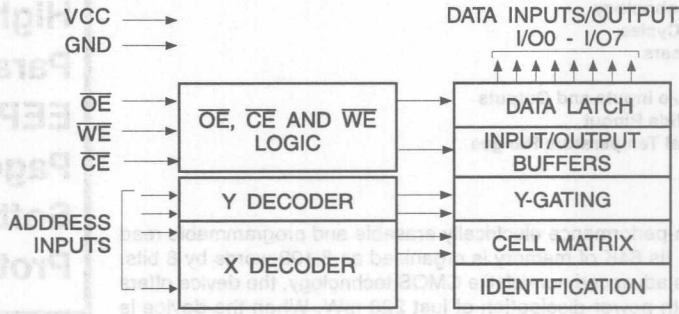
AT28HC64B

3

Rev. 0274E–10/98

The AT28HC64B is accessed like a Static RAM for the read or write cycle without the need for external components. The device contains a 64-byte page register to allow writing of up to 64 bytes simultaneously. During a write cycle, the addresses and 1 to 64 bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by $\overline{DATA}$ Polling of I/O_7. Once the end of a write cycle has been detected, a new access for a read or write can begin. Atmel's AT28HC64B has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and improved data retention. An optional software data protection mechanism is available to guard against inadvertent writes. The device also includes an extra 64 bytes of EEPROM for device identification or tracking.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V
Voltage on $\overline{OE}$ and A9 with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Device Operation

READ: The AT28HC64B is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high-impedance state when either $\overline{CE}$ or $\overline{OE}$ is high. This dual line control gives designers flexibility in preventing bus contention in their systems.

BYTE WRITE: A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high initiates a write cycle. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Once a byte write has been started, it will automatically time itself to completion. Once a programming operation has been initiated and for the duration of t_{WC}, a read operation will effectively be a polling operation.

PAGE WRITE: The page write operation of the AT28HC64B allows 1 to 64 bytes of data to be written into the device during a single internal programming period. A page write operation is initiated in the same manner as a byte write; after the first byte is written, it can then be followed by 1 to 63 additional bytes. Each successive byte must be loaded within 150 µs (t_{BLC}) of the previous byte. If the t_{BLC} limit is exceeded, the AT28HC64B will cease accepting data and commence the internal programming operation. All bytes during a page write operation must reside on the same page as defined by the state of the A6 to A12 inputs. For each $\overline{WE}$ high to low transition during the page write operation, A6 to A12 must be the same.

The A0 to A5 inputs specify which bytes within the page are to be written. The bytes may be loaded in any order and may be altered within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

$\overline{DATA}$ POLLING: The AT28HC64B features $\overline{DATA}$ Polling to indicate the end of a write cycle. During a byte or page write cycle, an attempted read of the last byte written will result in the complement of the written data to be presented on I/O_7. Once the write cycle has been completed, true data is valid on all outputs, and the next write cycle may begin. $\overline{DATA}$ Polling may begin at any time during the write cycle.

TOGGLE BIT: In addition to $\overline{DATA}$ Polling, the AT28HC64B provides another method for determining the end of a write cycle. During the write operation, successive attempts to read data from the device will result in I/O_6 toggling between one and zero. Once the write has completed, I/O_6 will stop toggling, and valid data will be read. Toggle bit reading may begin at any time during the write cycle.

DATA PROTECTION: If precautions are not taken, inadvertent writes may occur during transitions of the host system power supply. Atmel has incorporated both hardware and software features that will protect the memory against inadvertent writes.

HARDWARE DATA PROTECTION: Hardware features protect against inadvertent writes to the AT28HC64B in the following ways: (a) V_{CC} sense—if V_{CC} is below 3.8V (typical), the write function is inhibited; (b) V_{CC} power-on delay—once V_{CC} has reached 3.8V, the device will automatically time out 5 ms (typical) before allowing a write; (c) write inhibit—holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits write cycles; and (d) noise filter—pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a write cycle.

SOFTWARE DATA PROTECTION: A software-controlled data protection feature has been implemented on the AT28HC64B. When enabled, the software data protection (SDP), will prevent inadvertent writes. The SDP feature may be enabled or disabled by the user; the AT28HC64B is shipped from Atmel with SDP disabled.

SDP is enabled by the user issuing a series of three write commands in which three specific bytes of data are written to three specific addresses (refer to the *Software Data Protection Algorithm* diagram in this data sheet). After writing the 3-byte command sequence and waiting t_{WC}, the entire AT28HC64B will be protected against inadvertent writes. It should be noted that even after SDP is enabled, the user may still perform a byte or page write to the AT28HC64B. This is done by preceding the data to be written by the same 3-byte command sequence used to enable SDP.

Once set, SDP remains active unless the disable command sequence is issued. Power transitions do not disable SDP, and SDP protects the AT28HC64B during power-up and power-down conditions. All command sequences must conform to the page write timing specifications. The data in the enable and disable command sequences is not actually written into the device; their addresses may still be written with user data in either a byte or page write operation.

After setting SDP, any attempt to write to the device without the 3-byte command sequence will start the internal write timers. No data will be written to the device, however. For the duration of t_{WC}, read operations will effectively be polling operations.

DEVICE IDENTIFICATION: An extra 64 bytes of EEPROM memory are available to the user for device identification. By raising A9 to 12V ± 0.5V and using address locations 1FC0H to 1FFFH, the additional bytes may be written to or read from in the same manner as the regular memory array.

DC and AC Operating Range

		AT28HC64B-55	AT28HC64B-70	AT28HC64B-90	AT28HC64B-120
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.		-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write[2]	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X[1]	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z
Chip Erase	V_{IL}	V_H[3]	V_{IL}	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to the *AC Write Waveforms* diagrams in this data sheet.
3. $V_H = 12.0V \pm 0.5V$.

DC Characteristics

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	$V_{IN} = 0V$ to $V_{CC} + 1V$			10	µA
I_{LO}	Output Leakage Current	$V_{I/O} = 0V$ to V_{CC}			10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE} = V_{CC} - 0.3V$ to $V_{CC} + 1V$	Com., Ind.		100[1]	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE} = 2.0V$ to $V_{CC} + 1V$			2[1]	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz; $I_{OUT} = 0$ mA			40	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1$ mA			0.40	V
V_{OH}	Output High Voltage	$I_{OH} = -400$ µA		2.4		V

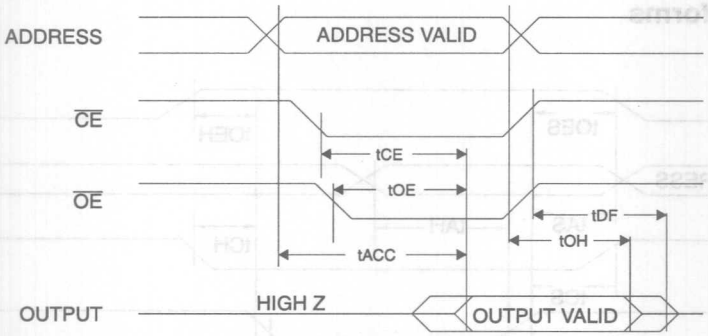
Note: 1. I_{SB1} and I_{SB2} for the 55 ns part is 40 mA maximum.

AC Read Characteristics

Symbol	Parameter	AT28HC64B-55		AT28HC64B-70		AT28HC64B-90		AT28HC64B-120		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		55		70		90		120	ns
t_{CE}[1]	$\overline{CE}$ to Output Delay		55		70		90		120	ns
t_{OE}[2]	$\overline{OE}$ to Output Delay	0	30	0	35	0	40	0	50	ns
t_{DF}[3][4]	$\overline{OE}$ to Output Float	0	30	0	35	0	40	0	50	ns
t_{OH}	Output Hold	0		0		0		0		ns

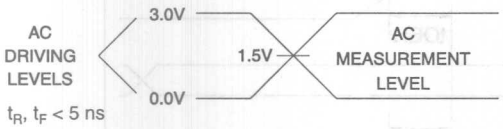
3

AC Read Waveforms[1][2][3][4]

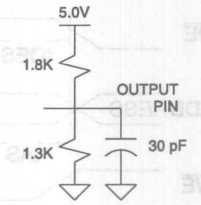


Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



Output Test Load



Pin Capacitance

f = 1 MHz, T = 25°C[1]

Symbol	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

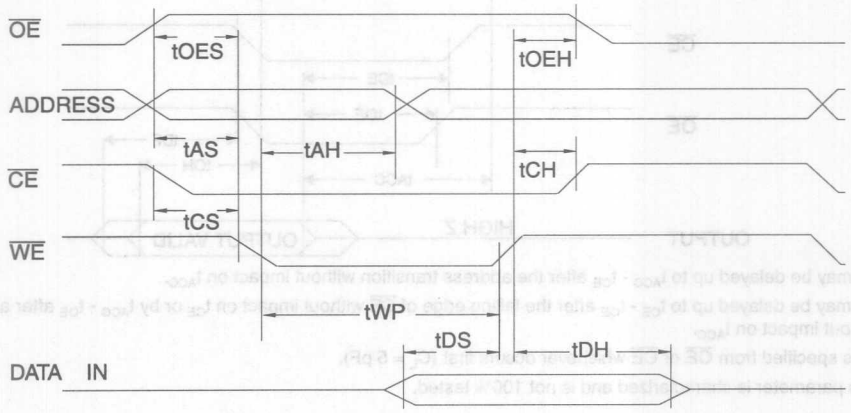
Note: 1. This parameter is characterized and is not 100% tested.

AC Write Characteristics

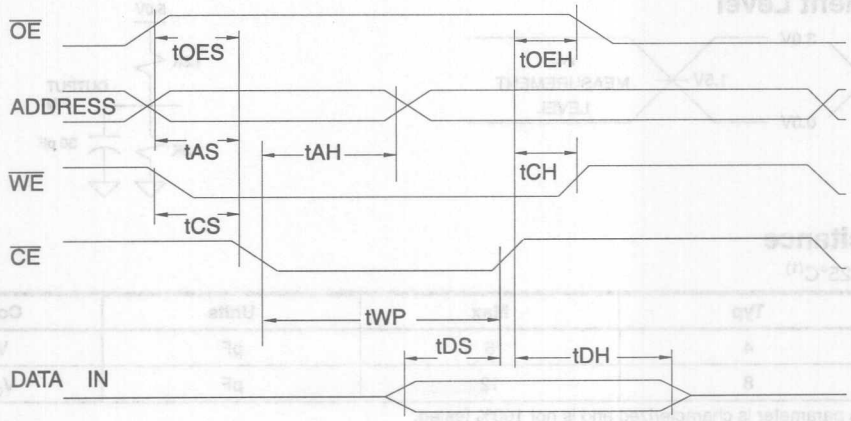
Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	100		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	0		ns

AC Write Waveforms

$\overline{WE}$ Controlled



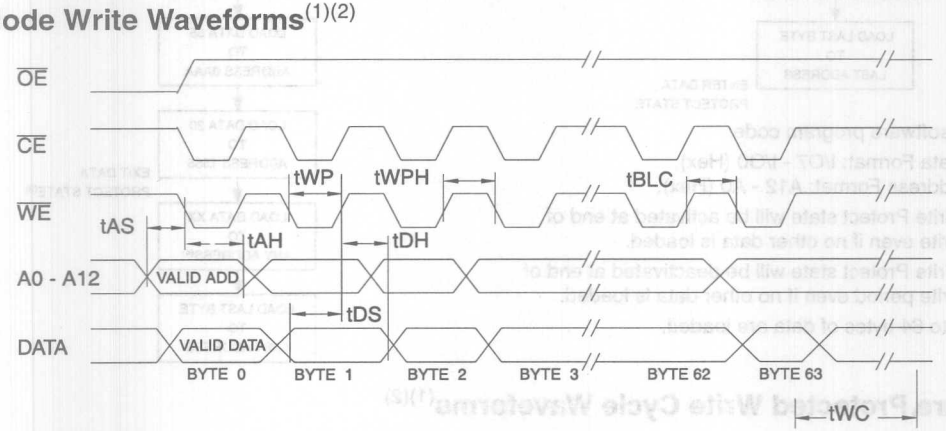
$\overline{CE}$ Controlled



Page Mode Characteristics

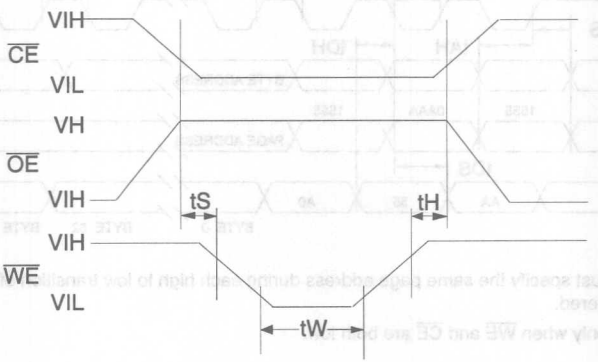
Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time		10	ms
t_{WC}	Write Cycle Time (28HC64B SL184)	0	2	ms
t_{AS}	Address Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}	Data Hold Time	0		ns
t_{WP}	Write Pulse Width	100		ns
t_{BLC}	Byte Load Cycle Time		150	µs
t_{WPH}	Write Pulse Width High	50		ns

Page Mode Write Waveforms(1)(2)



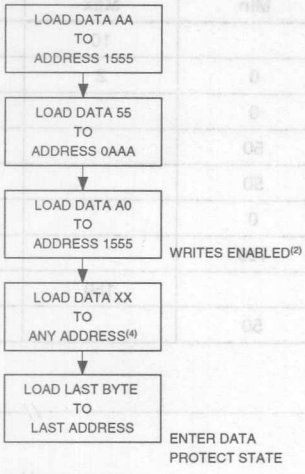
Notes: 1. A6 through A12 must specify the same page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
2. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

Chip Erase Waveforms

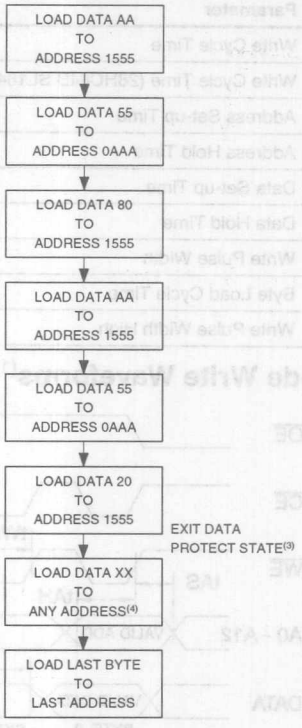


$t_S = t_H = 5$ µsec (min.)
$t_W = 10$ msec (min.)
V_H - 12.0V ± 0.5V

Software Data Protection Enable Algorithm[1]



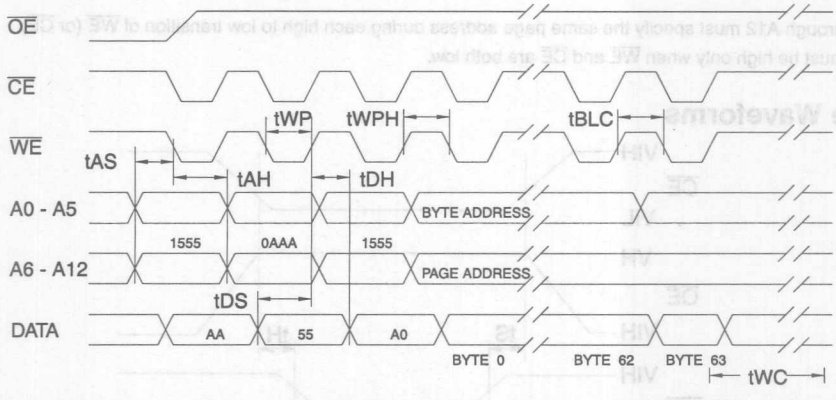
Software Data Protection Disable Algorithm[1]



Notes for software program code:

1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A12 - A0 (Hex).
2. Write Protect state will be activated at end of write even if no other data is loaded.
3. Write Protect state will be deactivated at end of write period even if no other data is loaded.
4. 1 to 64 bytes of data are loaded.

Software Protected Write Cycle Waveforms[1][2]



Notes: 1. A6 through A12 must specify the same page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$) after the software code has been entered.

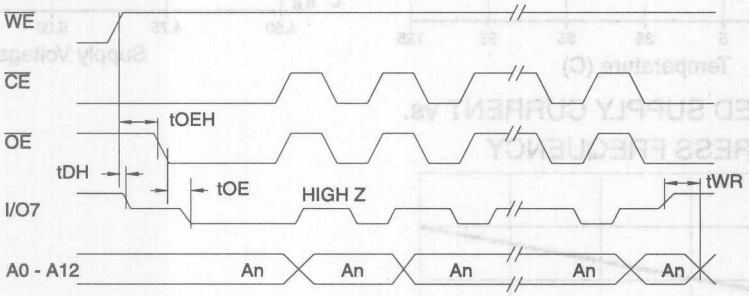
2. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

$\overline{\text{Data}}$ Polling Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	0			ns
t_{OEH}	$\overline{OE}$ Hold Time	0			ns
t_{OE}	$\overline{OE}$ to Output Delay[2]				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. This parameter is characterized and is not 100% tested.
2. See AC Read Characteristics.

$\overline{\text{Data}}$ Polling Waveforms

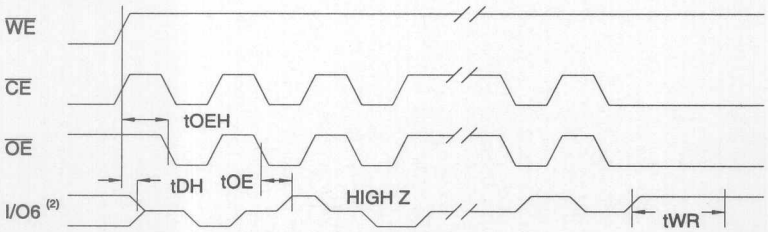


Toggle Bit Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay[2]				ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

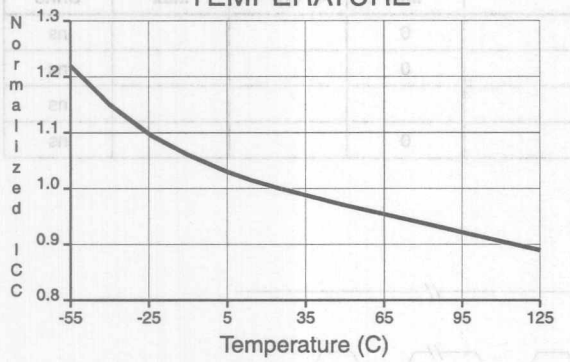
Notes: 1. This parameter is characterized and is not 100% tested.
2. See AC Read Characteristics.

Toggle Bit Waveforms[1][2][3]

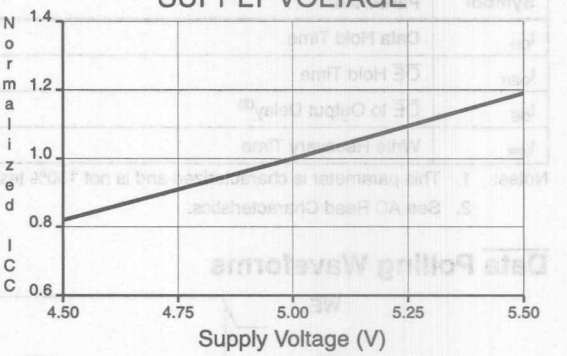


Notes: 1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used, but the address should not vary.

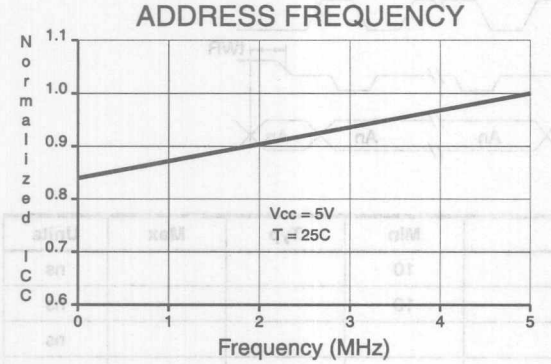
NORMALIZED SUPPLY CURRENT vs. TEMPERATURE



NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



NORMALIZED SUPPLY CURRENT vs. ADDRESS FREQUENCY



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
55	40	0.1	AT28HC64B-55JC	32J	Commercial
			AT28HC64B-55PC	28P6	0°C to 70°C)
			AT28HC64B-55SC	28S	
70	40	0.1	AT28HC64B-70JC	32J	Commercial
			AT28HC64B-70PC	28P6	(0°C to 70°C)
			AT28HC64B-70SC	28S	
			AT28HC64B-70TC	28T	
	40	0.1	AT28HC64B-70JI	32J	Industrial
			AT28HC64B-70PI	28P6	(-40°C to 85°C)
			AT28HC64B-70SI	28S	
			AT28HC64B-70TI	28T	
90	40	0.1	AT28HC64B-90JC	32J	Commercial
			AT28HC64B-90PC	28P6	(0°C to 70°C)
			AT28HC64B-90SC	28S	
			AT28HC64B-90TC	28T	
	40	0.1	AT28HC64B-90JI	32J	Industrial
			AT28HC64B-90PI	28P6	(-40°C to 85°C)
			AT28HC64B-90SI	28S	
			AT28HC64B-90TI	28T	
120	40	0.1	AT28HC64B-12JC	32J	Commercial
			AT28HC64B-12PC	28P6	(0°C to 70°C)
			AT28HC64B-12SC	28S	
			AT28HC64B-12TC	28T	
	40	0.1	AT28HC64B-12JI	32J	Industrial
			AT28HC64B-12PI	28P6	(-40°C to 85°C)
			AT28HC64B-12SI	28S	
			AT28HC64B-12TI	28T	

Note: 1. See Valid Part Numbers table below.

Package Type	
32J	32-Lead, Plastic J-Leaded Chip Carrier (PLCC)
28P6	28-Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
28S	28-Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
28T	28-Lead, Plastic Thin Small Outline Package (TSOP)
W	Die

Valid Part Numbers

The following table lists standard Atmel products that can be ordered.

Device Numbers	Speed	Package and Temperature Combinations
AT28HC64B	55	PC, SC
AT28HC64B	70	JI, PC, PI, SC, SI, TC, TI
AT28HC64B	90	JI, PC, PI, SC, SI, TC, TI
AT28HC64B	12	JI, PC, PI, SC, SI, TC, TI
AT28HC64B	–	W

Die Products

Reference Section: Parallel EEPROM Die Products

Features

- Fast Read Access Time - 70 ns
- Automatic Page Write Operation
  - Internal Address and Data Latches for 64 Bytes
  - Internal Control Timer
- Fast Write Cycle Times
  - Page Write Cycle Time: 3 ms or 10 ms Maximum
  - 1 to 64-Byte Page Write Operation
- Low Power Dissipation
  - 80 mA Active Current
  - 3 mA Standby Current
- Hardware and Software Data Protection
- $\overline{\text{DATA}}$ Polling for End of Write Detection
- High Reliability CMOS Technology
  - Endurance: 10^4 or 10^5 Cycles
  - Data Retention: 10 Years
- Single 5V ± 10% Supply
- CMOS and TTL Compatible Inputs and Outputs
- JEDEC Approved Byte-Wide Pinout
- Full Military, Commercial, and Industrial Temperature Ranges

Description

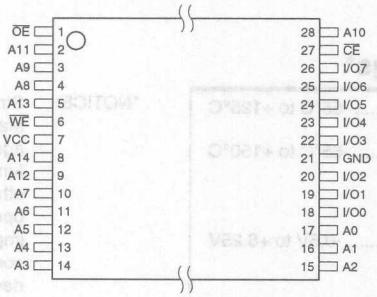
The AT28HC256 is a high-performance Electrically Erasable and Programmable Read Only Memory. Its 256K of memory is organized as 32,768 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the AT28HC256

(continued)

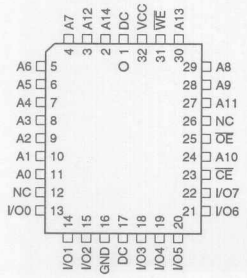
Pin Configurations

Pin Name	Function
A0 - A14	Addresses
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect
DC	Don't Connect

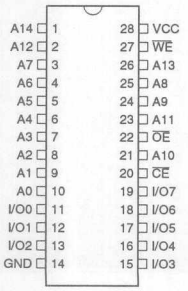
TSOP
Top View



LCC, PLCC
Top View



CERDIP, PDIP, FLATPACK
Top View



PGA
Top View

4 A6	3 A7	1 A14	27 WE	26 A13
5 A5	2 A12	28 VCC	24 A9	25 A8
7 A3	6 A4		22 OE	23 A11
9 A1	8 A2		20 CE	21 A10
11 I/O0	10 A0	14 GND	16 I/O4	19 I/O7
12 I/O1	13 I/O2	15 I/O3	17 I/O5	18 I/O6

Note: PLCC package pins 1 and 17 are DON'T CONNECT.

256 (32K x 8) High Speed Parallel EEPROMs

AT28HC256

3

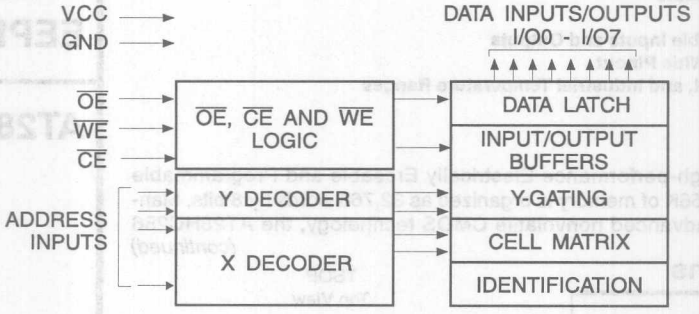
Rev. 0007G–10/98

offers access times to 70 ns with power dissipation of just 440 mW. When the AT28HC256 is deselected, the standby current is less than 5 mA.

The AT28HC256 is accessed like a Static RAM for the read or write cycle without the need for external components. The device contains a 64-byte page register to allow writing of up to 64 bytes simultaneously. During a write cycle, the address and 1 to 64 bytes of data are internally latched, freeing the addresses and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by $\overline{DATA}$ polling of I/O_7. Once the end of a write cycle has been detected a new access for a read or write can begin.

Atmel's 28HC256 has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and improved data retention characteristics. An optional software data protection mechanism is available to guard against inadvertent writes. The device also includes an extra 64 bytes of EEPROM for device identification or tracking.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V
Voltage on $\overline{OE}$ and A9 with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Device Operation

READ: The AT28HC256 is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state when either $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention in their system.

BYTE WRITE: A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high initiates a write cycle. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Once a byte write has been started it will automatically time itself to completion. Once a programming operation has been initiated and for the duration of t_{WC}, a read operation will effectively be a polling operation.

PAGE WRITE: The page write operation of the AT28HC256 allows 1 to 64 bytes of data to be written into the device during a single internal programming period. A page write operation is initiated in the same manner as a byte write; the first byte written can then be followed by 1 to 63 additional bytes. Each successive byte must be written within 150 µs (t_{BLC}) of the previous byte. If the t_{BLC} limit is exceeded the AT28C256 will cease accepting data and commence the internal programming operation. All bytes during a page write operation must reside on the same page as defined by the state of the A6 - A14 inputs. That is, for each $\overline{WE}$ high to low transition during the page write operation, A6 - A14 must be the same.

The A0 to A5 inputs are used to specify which bytes within the page are to be written. The bytes may be loaded in any order and may be altered within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

$\overline{DATA}$ POLLING: The AT28HC256 features $\overline{DATA}$ Polling to indicate the end of a write cycle. During a byte or page write cycle an attempted read of the last byte written will result in the complement of the written data to be presented on I/O_7. Once the write cycle has been completed, true data is valid on all outputs, and the next write cycle may begin. $\overline{DATA}$ Polling may begin at anytime during the write cycle.

TOGGLE BIT: In addition to $\overline{DATA}$ Polling the AT28HC256 provides another method for determining the end of a write cycle. During the write operation, successive attempts to read data from the device will result in I/O_6 toggling between one and zero. Once the write has completed, I/O_6 will stop toggling and valid data will be read. Testing the toggle bit may begin at any time during the write cycle.

DATA PROTECTION: If precautions are not taken, inadvertent writes to any 5-volt-only nonvolatile memory may occur during transition of the host system power supply. Atmel has incorporated both hardware and software features that will protect the memory against inadvertent writes.

HARDWARE PROTECTION: Hardware features protect against inadvertent writes to the AT28HC256 in the following ways: (a) V_{CC} sense—if V_{CC} is below 3.8V (typical) the write function is inhibited; (b) V_{CC} power-on delay—once V_{CC} has reached 3.8V the device will automatically time out 5 ms typical) before allowing a write; (c) write inhibit—holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits write cycles; and (d) noise filter—pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a write cycle.

SOFTWARE DATA PROTECTION: A software controlled data protection feature has been implemented on the AT28HC256. When enabled, the software data protection (SDP), will prevent inadvertent writes. The SDP feature may be enabled or disabled by the user; the AT28HC256 is shipped from Atmel with SDP disabled.

SDP is enabled by the host system issuing a series of three write commands; three specific bytes of data are written to three specific addresses (refer to Software Data Protection Algorithm). After writing the 3-byte command sequence and after t_{WC} the entire AT28HC256 will be protected against inadvertent write operations. It should be noted, that once protected the host may still perform a byte or page write to the AT28HC256. This is done by preceding the data to be written by the same 3-byte command sequence.

Once set, SDP will remain active unless the disable command sequence is issued. Power transitions do not disable SDP and SDP will protect the AT28HC256 during power-up and power-down conditions. All command sequences must conform to the page write timing specifications. It should also be noted that the data in the enable and disable command sequences is not written to the device and the memory addresses used in the sequence may be written with data in either a byte or page write operation.

After setting SDP, any attempt to write to the device without the three byte command sequence will start the internal write timers. No data will be written to the device; however, for the duration of t_{WC}, read operations will effectively be polling operations.

DEVICE IDENTIFICATION: An extra 64 bytes of EEPROM memory are available to the user for device identification. By raising A9 to 12V ± 0.5V and using address locations 7FC0H to 7FFFH the additional bytes may be written to or read from in the same manner as the regular memory array.

OPTIONAL CHIP ERASE MODE: The entire device can be erased using a 6-byte software code. Please see Software Chip Erase application note for details.

DC and AC Operating Range

		AT28HC256-70	AT28HC256-90	AT28HC256-12
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.		-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5V ± 10%	5V ± 10%	5V ± 10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write[2]	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X[1]	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X		X	
Output Disable	X	V_{IH}	X	High Z
Chip Erase	V_{IL}	V_H[3]	V_{IL}	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to AC Programming Waveforms.
3. V_H = 12.0V ± 0.5V.

DC Characteristics

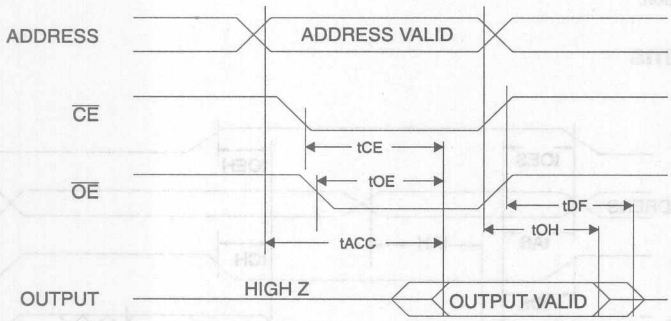
Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC} + 1V			10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}			10	µA
I_{SB1}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V to V_{CC} + 1V	AT28HC256-90, -12		3	mA
			AT28HC256-70		60	mA
I_{SB2}	V_{CC} Standby Current CMOS	$\overline{CE}$ = -3.0V to V_{CC} + 1V	AT28HC256-90, -12		300	µA
I_{CC}	V_{CC} Active Current	f = 5 MHz; I_{OUT} = 0 mA			80	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 6.0 mA			0.45	V
V_{OH}	Output High Voltage	I_{OH} = -4 mA		2.4		V

AC Read Characteristics

Symbol	Parameter	AT28HC256-70		AT28C256-90		AT28HC256-12		Units
		Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		70		90		120	ns
t_{CE}[1]	$\overline{CE}$ to Output Delay		70		90		120	ns
t_{OE}[2]	$\overline{OE}$ to Output Delay	0	35	0	40	0	50	ns
t_{DF}[3][4]	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	35	0	40	0	50	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		ns

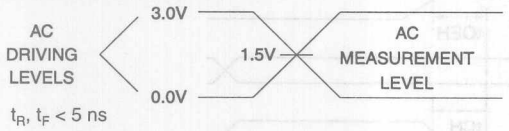
3

AC Read Waveforms[1][2][3][4]

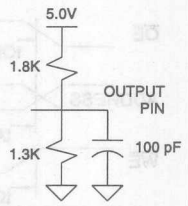


Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



Output Test Load



Pin Capacitance

f = 1 MHz, T = 25°C[1]

Symbol	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

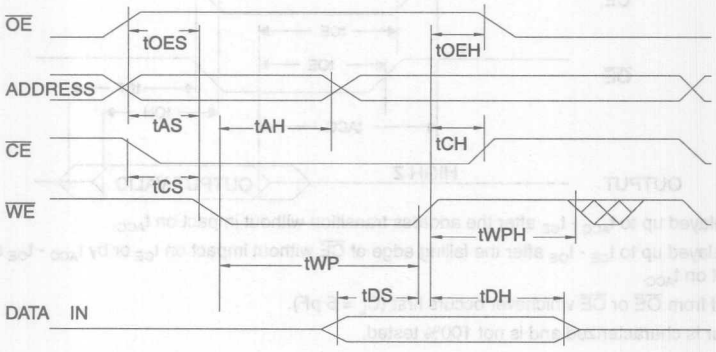
AC Write Characteristics

Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	100		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	0		ns
t_{DV}	Time to Data Valid	NR[1]		

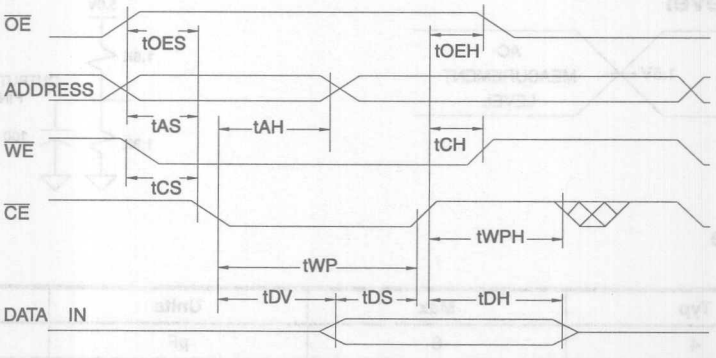
Note: 1. NR = No Restriction.

AC Write Waveforms

$\overline{WE}$ Controlled



$\overline{CE}$ Controlled

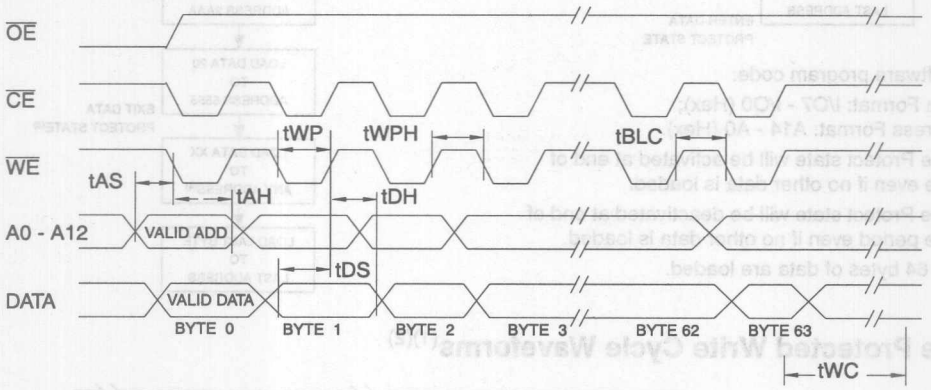


Page Mode Write Characteristics

Symbol	Parameter		Min	Typ	Max	Units
t_{WC}	Write Cycle Time	AT28HC256		5	10	ms
		AT28HC256F		2	3.0	ms
t_{AS}	Address Set-up Time		0			ns
t_{AH}	Address Hold Time		50			ns
t_{DS}	Data Set-up Time		50			ns
t_{DH}	Data Hold Time		0			ns
t_{WP}	Write Pulse Width		100			ns
t_{BLC}	Byte Load Cycle Time				150	µs
t_{WPH}	Write Pulse Width High		50			ns

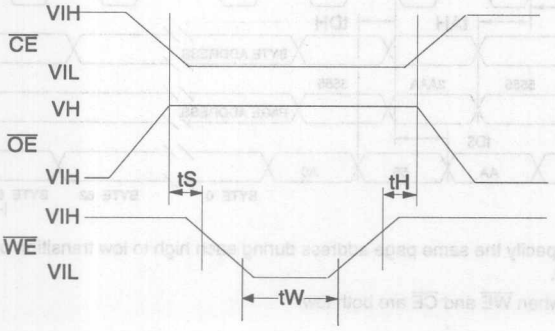
3

Page Mode Write Waveforms(1)(2)



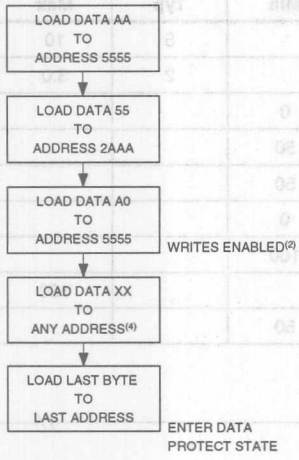
Notes: 1. A6 through A14 must specify the same page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
2. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

Chip Erase Waveforms

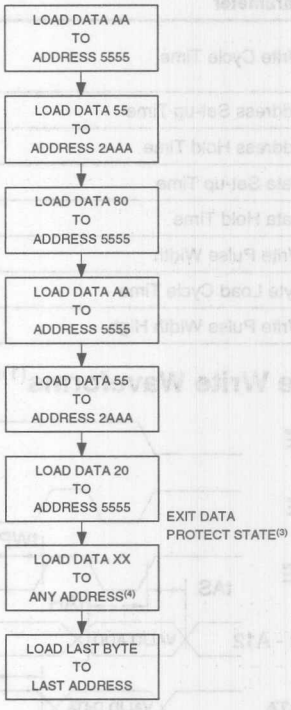


$t_S = t_H = 5$ µsec (min.)
$t_W = 10$ msec (min.)
$V_H = 12.0V \pm 0.5V$

Software Data Protection Enable Algorithm[1]



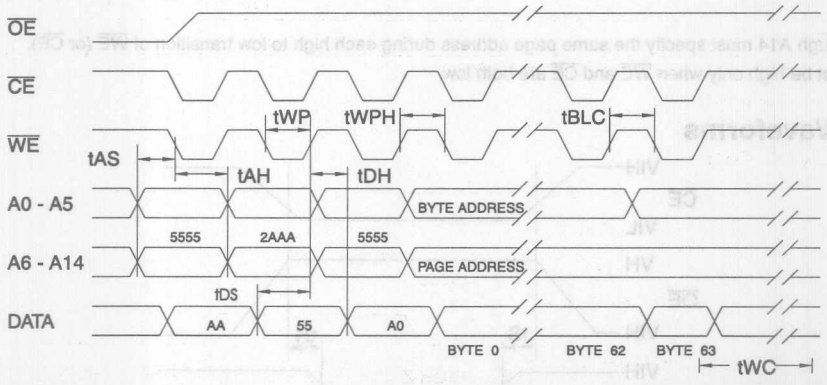
Software Data Protection Disable Algorithm[1]



Notes for software program code:

1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Write Protect state will be activated at end of write even if no other data is loaded.
3. Write Protect state will be deactivated at end of write period even if no other data is loaded.
4. 1 to 64 bytes of data are loaded.

Software Protected Write Cycle Waveforms[1][2]



Notes: 1. A6 through A14 must specify the same page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$) after the software code has been entered.

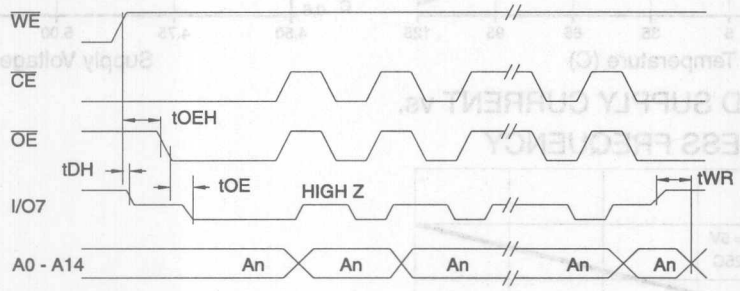
2. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

Data Polling Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	0			ns
t_{OEH}	$\overline{OE}$ Hold Time	0			ns
t_{OE}	$\overline{OE}$ to Output Delay[2]				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See AC Read Characteristics.

Data Polling Waveforms

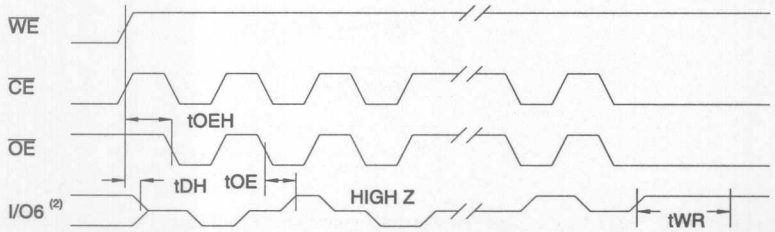


Toggle Bit Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay[2]				ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

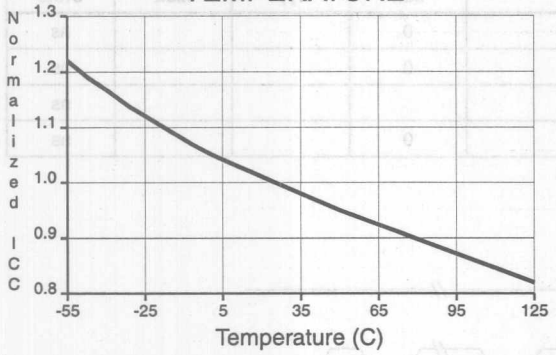
Notes: 1. These parameters are characterized and not 100% tested.
2. See AC Read Characteristics.

Toggle Bit Waveforms

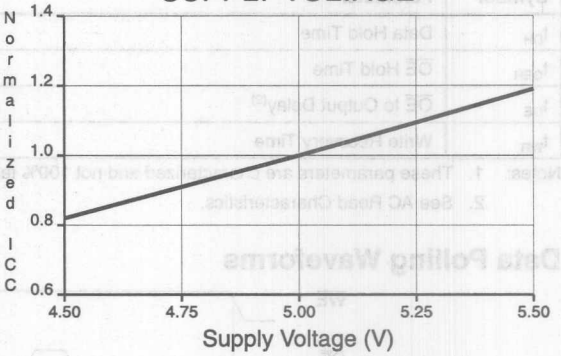


Notes: 1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

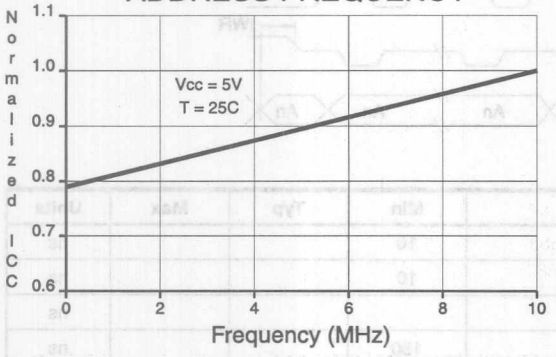
NORMALIZED SUPPLY CURRENT vs. TEMPERATURE



NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



NORMALIZED SUPPLY CURRENT vs. ADDRESS FREQUENCY



Ordering Information[1]

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
70	80	60	AT28HC256(E,F)-70JC AT28HC256(E,F)-70PC	32J 28P6	Commercial (0°C to 70°C)
		0.3	AT28HC256(E,F)-70JI AT28HC256(E,F)-70PI	32J 28P6	Industrial (-40°C to 85°C)
90	80	0.3	AT28HC256(E,F)-90JC AT28HC256(E,F)-90PC	32J 28P6	Commercial (0°C to 70°C)
			AT28HC256(E,F)-90JI AT28HC256(E,F)-90PI	32J 28P6	Industrial (-40°C to 85°C)
	80	0.3	AT28HC256(E,F)-90DM/883 AT28HC256(E,F)-90FM/883 AT28HC256(E,F)-90LM/883 AT28HC256(E,F)-90UM/883	28D6 28F 32L 28U	Military/883C Class B, Fully Compliant (-55°C to 125°C)
120	80	0.3	AT28HC256(E,F)-12JC AT28HC256(E,F)-12PC AT28HC256(E,F)-12SC AT28HC256(E,F)-12TC	32J 28P6 28S 28T	Commercial (0°C to 70°C)
	80	0.3	AT28HC256(E,F)-12JI AT28HC256(E,F)-12PI AT28HC256(E,F)-12SI AT28HC256(E,F)-12TI	32J 28P6 28S 28T	Industrial (-40°C to 85°C)
	80	0.3	AT28HC256(E,F)-12DM/883 AT28HC256(E,F)-12FM/883 AT28HC256(E,F)-12LM/883 AT28HC256(E,F)-12UM/883	28D6 28F 32L 28U	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Package Type	
28D6	28-Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
28F	28-Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)
32J	32-Lead, Plastic J-Leaded Chip Carrier (PLCC)
32L	32-Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28-Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
28S	28-Lead, 0.300" Wide Plastic Gull Wing Small Outline (SOIC)
28T	28-Lead, Plastic Thin Small Outline Package (TSOP)
28U	28-Pin, Ceramic Pin Grid Array (PGA)
W	Die
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 10 ms
E	High Endurance Option: Endurance = 100K Write Cycles
F	Fast Write Option: Write Time = 3 ms

Ordering Information[1] (Continued)

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
90	80	0.3	5962-88634 03 UX 5962-88634 03 XX 5962-88634 03 YX 5962-88634 03 ZX	28U 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)
	80	0.3	5962-88634 04 UX 5962-88634 04 XX 5962-88634 04 YX 5962-88634 04 ZX	28U 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)
120	80	0.3	5962-88634 01 UX 5962-88634 01 XX 5962-88634 01 YX 5962-88634 01 ZX	28U 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)
	80	0.3	5962-88634 02 UX 5962-88634 02 XX 5962-88634 02 YX 5962-88634 02 ZX	28U 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Note: 1. See Valid Part Numbers table on next page.

Package Type	
28D6	28-Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
28F	28-Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)
32J	32-Lead, Plastic J-Leaded Chip Carrier (PLCC)
32L	32-Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28-Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
28S	28-Lead, 0.300" Wide Plastic Gull Wing Small Outline (SOIC)
28T	28-Lead, Plastic Thin Small Outline Package (TSOP)
28U	28-Pin, Ceramic Pin Grid Array (PGA)
W	Die
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 10 ms
E	High Endurance Option: Endurance = 100K Write Cycles
F	Fast Write Option: Write Time = 3 ms

Ordering Information Note

Previous data sheets included the low power suffixes L, LE and LF on the At28HC256 for 120 ns and 90 ns speeds. The low power parameters are now standard; therefore, the L, LE and LF suffixes are no longer required.

Valid Part Numbers

The following table lists standard Atmel products that can be ordered:

Device Numbers	Speed	Package and Temperature Combinations
AT28HC256	70	JC, JI, PC, PI
AT28HC256	90	JC, JI, PC, PI, TC, TI, DM/883, FM/883, UM/883
AT28HC256E	90	JC, JI, PC, PI, TC, TI, DM/883, FM/883, UM/883
AT28HC256F	90	JC, JI, PC, PI, TC, TI, DM/883, FM/883, UM/883
AT28HC256	12	JC, JI, PC, PI, TC, TI, DM/883, FM/883, UM/883
AT28HC256E	12	JC, JI, PC, PI, TC, TI, DM/883, FM/883, UM/883
AT28HC256F	12	JC, JI, PC, PI, TC, TI, DM/883, FM/883, UM/883

Die Products

Reference Section: Parallel EEPROM Die Products

Parallel EEPROM Data Protection

Advantages of EEPROMs

EEPROMs provide the memory solution wherever reprogrammable, nonvolatile memory is required. They are easy to use, requiring little or no support hardware such as refresh clocks or batteries. Each memory location can be selectively changed without impact on any other location; blanket erasure and rewriting of the entire device or a large section of it is not required.

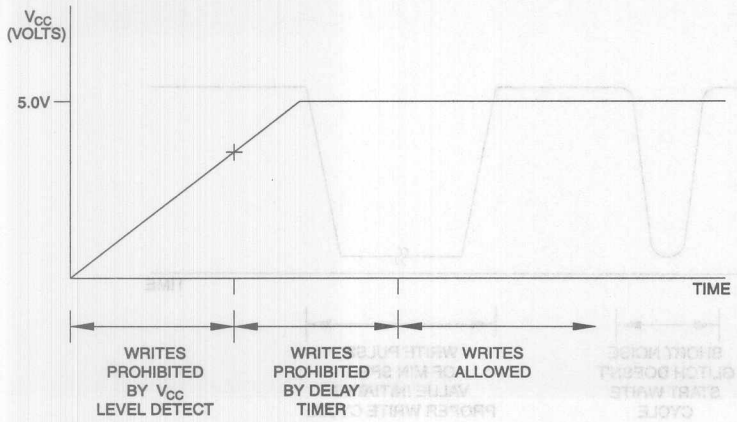
EEPROMs made at Atmel were designed to provide the best features available. Atmel EEPROMs provide high speed read access times so that many applications can use them without inserting costly wait states. The page mode write operation of Atmel EEPROMs allows for the fastest effective write time available in EEPROM memories. Since all of Atmel's devices are made in CMOS, they offer the benefits of low operating and standby power.

In order to take advantage of all of the benefits of Atmel EEPROMs, care must be taken to maintain the integrity of the data. While an EEPROM will retain its data for many years with or without power applied, improper operation of the device could result in data being inadvertently rewritten.

When is Data Susceptible to Corruption

In the use of any memory device, it is expected that the data stored in it is available as it is written. This is especially true of EEPROMs since their code often controls the operation of the system in which they are contained. Unlike most other memory types that are rewritten in systems, EEPROMs are often expected to retain their data for a period of many years, with or without power applied and during power transitions. For these reasons, added attention is given to avoid corrupting data in EEPROMs.

Figure 1. Hardware Data Protection - Power Level Sense Detector and Power On Delay Timer



Parallel EEPROMs

Application Note

3

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There are a number of situations in which data is particularly prone to corruption. These situations include powering on and off of the devices, noise spikes on the control lines and system glitches. Atmel EEPROMs include features to help protect against each of these potential sources of inadvertent writes. Atmel data protection features are broken down into two different types: hardware data protection features and software data protection features.

Atmel Hardware Data Protection Features

Atmel EEPROMs include four different types of hardware data protection. These features provide protection against most inadvertent writes that might occur in a system. Atmel hardware data protection features include: three line write control, power level sense detector, power on delay timer and noise filters on $\overline{CE}$ and $\overline{WE}$.

THREE-LINE WRITE CONTROL: In order to write a device the $\overline{OE}$ signal must be high with the $\overline{CE}$ and $\overline{WE}$ signals low. Holding any of the three lines in the opposite state will prohibit a write cycle. For example, whenever the $\overline{OE}$ signal is low, a write to the device cannot be started.

POWER LEVEL SENSE DETECTOR: An active circuit in Atmel EEPROMs monitors the level of the supply voltage to the device. If the supply is below 3.8 volts, typical, write cycles to the devices can not be activated.

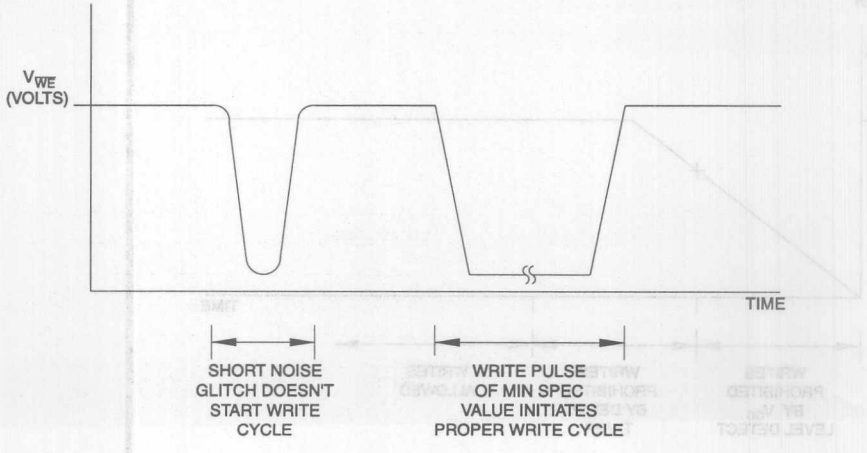
POWER ON DELAY TIMER: As power is applied to Atmel EEPROMs, the power level sense detector will issue an internal signal that indicates that the supply is above the sense level. At this time an internal timer is initiated that times out in typically 5 ms. During this time period, writes to the device cannot be performed. This delay period serves two purposes. First, it allows the supply level additional time to rise to within the standard operating region before writes are permitted. Secondly, it lets the system stabilize and present the correct levels to the control pins of the EEPROM so that the EEPROM doesn't react to its inputs before they are actually valid. Figure 1 shows the combined action of the power supply level detector and the delay timer upon writes to the device.

NOISE FILTERS ON $\overline{WE}$ AND $\overline{CE}$: If brief noise pulses below V_{IH} occur on the $\overline{WE}$ or $\overline{CE}$ inputs to the device, a write cycle will not be initiated. Internal to the EEPROM, a noise filter does not allow the short pulses to activate a write cycle. As shown in Figure 2, write pulses of sufficient length will still initiate writes but short noise spikes on the $\overline{WE}$ or $\overline{CE}$ control lines will not.

Atmel Software Data Protection Feature

Available on some Atmel EEPROMs is a user selectable feature that requires a software sequence at the beginning of each write cycle in order for a write to be performed. To enable the software data protection feature, a series of three-write commands to specific addresses with specific data must be performed. Once set, the same 3-byte code must begin each write request. (A separate write cycle to enable the software feature is not necessary; after any write that is preceded with the 3-byte code, the software data protection function will be enabled, see Figure 3.) The feature may be disabled by issuing a 6-byte code to the device as shown in Figure 4. After being set, the software data protection feature remains active until its disable command is issued. Power transitions will not reset the software data protection feature, but the feature will prevent against inadvertent writes during power transitions.

Figure 2. Hardware Data Protection - Noise Filter



The software data protection feature protects data against various causes of inadvertent writes. Since it is active during power transitions it protects data when powering on or off the device. Noise spikes that occur on the control lines will be ignored since they will not show the correct address and data needed to start a write cycle. Even for system malfunctions, such as when write pulses of adequate length are given to the device, the software feature can prevent the corruption of the data in the EEPROM. The address locations used for the software code are not sacrificed from the usable memory array. The device recognizes the software code and does not alter the data stored at the address locations of the code. Byte locations of code are still usable, and don't have to be rewritten.

System Design Considerations

Designing systems with data integrity in mind can greatly reduce the chance of lost data. The amount of attention needed depends upon the nature of the design. Following are a few areas that might need special attention in certain designs.

External Power On Protection

Many systems will have a PON (power on) signal to control the operation of the system. Such a signal can be gated with the logic creating the $\overline{OE}$ signal to the EEPROM, holding $\overline{OE}$ low when the PON signal is false. Similarly, a PON-type signal could be gated with the $\overline{WE}$ or $\overline{CE}$ logic, forcing $\overline{WE}$ or $\overline{CE}$ high when writes should not be allowed.

If the system does not include a PON-type signal, one can be created from various programmable voltage reference devices. With such a device, the user can select the voltage supply level below which the device cannot be written. It should be noted that in many systems, using Atmel's EEPROMS with their internal power level detection and power delay timer, no additional power on circuitry is required for the device.

Multiple Power Supplies

In systems that utilize more than one power supply, extra care must be taken during power transitions to both the EEPROM and the devices controlling the inputs to the EEPROM. Power on rates of the different supplies are likely to vary. Using programmable voltage reference devices to detect the power level of both supplies and forcing the $\overline{OE}$ pin low when either line is below the desired level may be used in such situations to avoid inadvertent writes.

Memory Cards

Since memory cards are often pushed into and pulled out of systems that are already powered on, they have additional chances of inadvertent writes. If the edge connector is arranged such that power and control lines are not asserted in a prescribed manner, false writes to the device may occasionally occur depending upon how the card is inserted. To provide proper power on sequencing, a card could be designed with its control pins recessed from the edge of the card. Resistors would be placed on the card to connect $\overline{CE}$ and $\overline{WE}$ to V_{CC} and $\overline{OE}$ to ground. This arrangement insures that power is first applied to the device and that the control pins are not in the write state until each pin is being controlled by the host system. Variations of this technique may be used effectively in different systems; the basic idea is to guarantee systematic application of the power and control pins such that a write state is not entered upon insertion or removal of the card from the host.

Figure 3. Software Data Protection - Enable

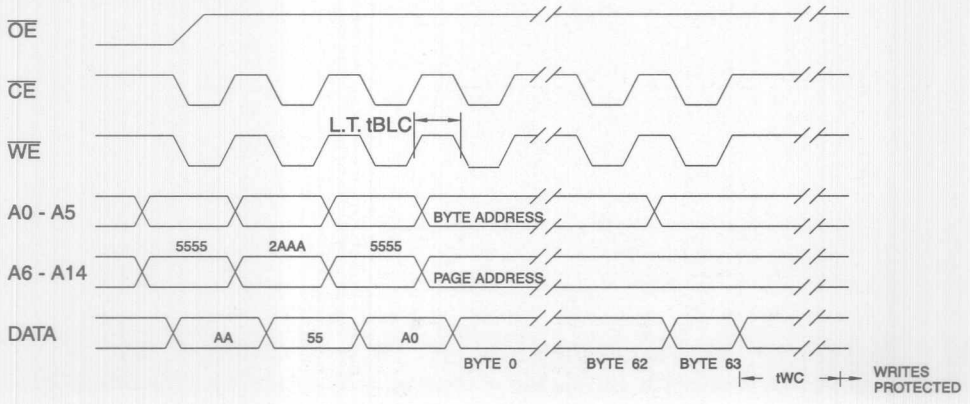
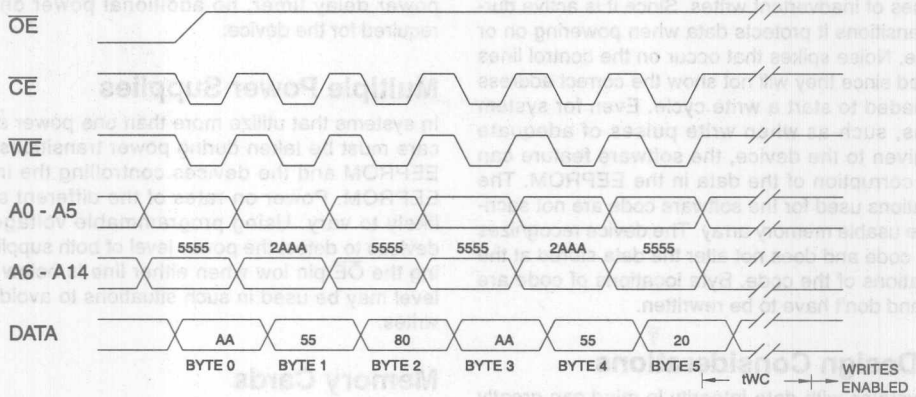


Figure 4. Software Data Protection - Disable



Software Chip Erase

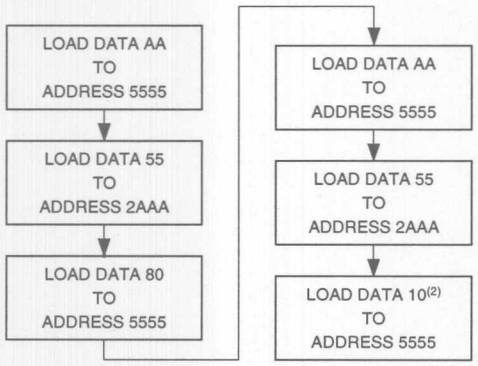
The entire device can be erased at one time by using a 6-byte software code. The software chip erase code consists of 6-byte load commands to specific address locations with specific data patterns. Once the code has been entered, the device will set each byte to the high state (FFH). After the software chip erase has been initiated, the device will internally time the erase operation so that no external clocks are required. The maximum time required to erase the whole chip is t_{EC} (20 ms). The software data protection is still enabled even after the software chip erase is performed.

Chip Erase Cycle Characteristics

Symbol	Parameter	
t_{EC}	Chip Erase Cycle Time	20 ms Max

Note: 1. Please refer to individual data sheets for the minimum and maximum values of the t_{AS}, t_{AH}, t_{DS}, t_{DH}, t_{WP}, t_{BLC}, and t_{WPH} parameters.

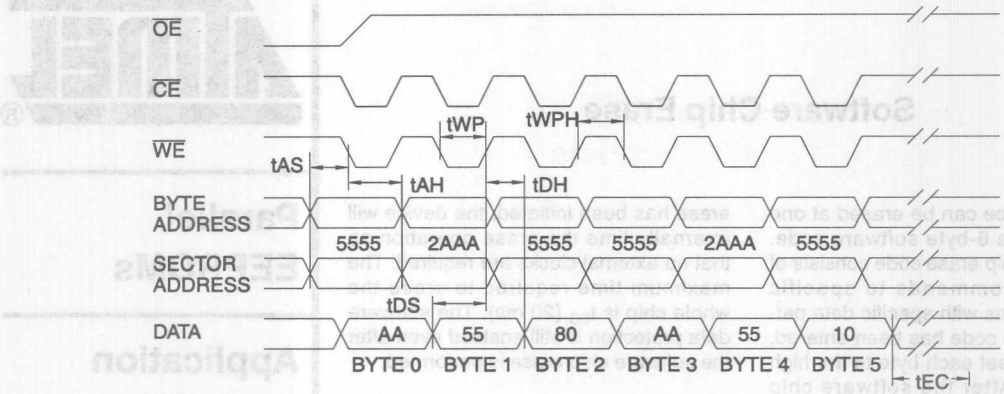
Chip Erase Software Algorithm[1][3]



Notes:
1. Data Format: (Hex); Address Format: (Hex).
2. After loading the 6-byte code, no byte loads are allowed until the completion of the erase cycle. The erase cycle will time itself to completion in 20 ms (max).
3. The flow diagram shown is for a x8 part. For a x16 part, the data should be 16 bits long (e.g., the data to be loaded should be AAAA for step 1 in the algorithm).

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Chip Erase Cycle Waveforms



Note: 1. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

Programmers That Support Atmel Memory Products

The following programmers support Atmel memory products. Please contact the companies individually to find out if specific products and packages are supported.

Advin Systems Inc.
1050-L East Duane Avenue
Sunnyvale, California 95086
(408) 243-7000

BP Microsystems
1000 North Post Oak Road, Suite #225
Houston, Texas 77055-7237
(713) 688-4600

Bytek Corporation
543 North West 77th Street
Bocaraton, Florida 33487-1323
(407) 994-3520

Data I/O Corporation
P.O. Box 97946
10525 Willows Road NE
Redmond, Washington 98073-9746
(800) 247-5700

Elan Systems, Inc.
365 Woodview Avenue, Suite #700
Morgan Hill, California 95037
(408) 778-7267

Logical Devices
692 South Military Trail
Deerfield Beach, Florida 33442
(305) 428-6868

Minato Electronics
3628 Madison Avenue, Suite #5
North Highlands, California 95660
(916) 348-6066

Needham's Electronics
4630 Beloit Drive, Suite #20
Sacramento, California 95841
(916) 924-8037

SMS
17411 N.E. Union Hill Road, Suite #100
Redmond, Washington 98052
(206) 883-8447

System General
1603A South Main Street
Milpitas, California 95035
(408) 263-6667

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Parallel EEPROMs

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Contents

Section 4 DataFlash®

***Battery*-Voltage™ • 2.7V - 3.6V Operation**

AT45DB011	128K x 8	1M-bit, 2.7-volt Only Serial Interface Flash 4-3
AT45DB021	256K x 8	2M-bit, 2.7-volt Only Serial Interface Flash 4-21
AT45DB041	512K x 8	4M-bit, 2.7-volt Only Serial Interface Flash 4-39
AT45DB080	1024K x 8	8M-bit, 2.7-volt Only Sequential Access, Parallel I/O Flash 4-57
AT45DB081	1024K x 8	8M-bit, 2.7-volt Only Serial Interface Flash 4-75
AT45DB161	2048K x 8	16M-bit, 2.7-volt Only Serial Interface Flash 4-93
AT45DB321	4096K x 8	32M-bit, 2.7-volt Only Serial Interface Flash 4-113

Standard Voltage • 5V Operation

AT45D011	128K x 8	1M-bit, 5-volt Only Serial Interface Flash 4-133
AT45D021	256K x 8	2M-bit, 5-volt Only Serial Interface Flash 4-153
AT45D041	512K x 8	4M-bit, 5-volt Only Serial Interface Flash 4-171
AT45D081	1024K x 8	8M-bit, 5-volt Only Serial Interface Flash 4-189
AT45D161	2048K x 8	16M-bit, 5-volt Only Serial Interface Flash 4-207

DataFlash Application Note

Serial DataFlash — Using Atmel's Serial DataFlash 4-227

Features

- Single 2.7V - 3.6V Supply
- Serial Interface Architecture
- Page Program Operation
  - Single Cycle Reprogram (Erase and Program)
  - 512 Pages (264 Bytes/Page) Main Memory
- Optional Page and Block Erase Operations
- One 264-Byte SRAM Data Buffer
- Internal Program and Control Timer
- Fast Page Program Time – 7 ms Typical
- 120 µs Typical Page to Buffer Transfer Time
- Low-Power Dissipation
  - 4 mA Active Read Current Typical
  - 2 µA CMOS Standby Current Typical
- 13 MHz Max Clock Frequency
- Hardware Data Protection Feature
- Serial Peripheral Interface (SPI) Compatible – Modes 0 and 3
- CMOS and TTL Compatible Inputs and Outputs
- Commercial and Industrial Temperature Ranges

Description

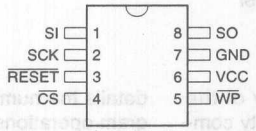
The AT45DB011 is a 2.7-volt only, serial interface Flash memory suitable for in-system reprogramming. Its 1,081,344 bits of memory are organized as 512 pages of 264 bytes each. In addition to the main memory, the AT45DB011 also contains one SRAM data buffer of 264 bytes. Unlike conventional Flash memories that are accessed randomly with multiple address lines and a parallel interface, the DataFlash uses a serial interface to sequentially access its data. The simple serial interface facilitates hard-

(continued)

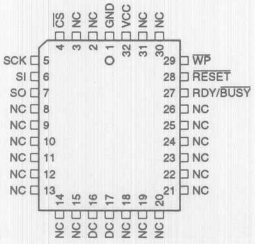
Pin Configurations

Pin Name	Function
$\overline{CS}$	Chip Select
SCK	Serial Clock
SI	Serial Input
SO	Serial Output
$\overline{WP}$	Hardware Page Write Protect Pin
$\overline{RESET}$	Chip Reset
RDY/$\overline{BUSY}$	Ready/Busy

SOIC



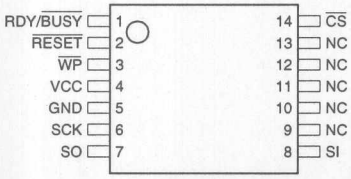
PLCC



Note: PLCC package pins 16 and 17 are DON'T CONNECT

TSSOP Top View

Type 1



1-Megabit 2.7-volt Only Serial DataFlash®

4

AT45DB011 Preliminary

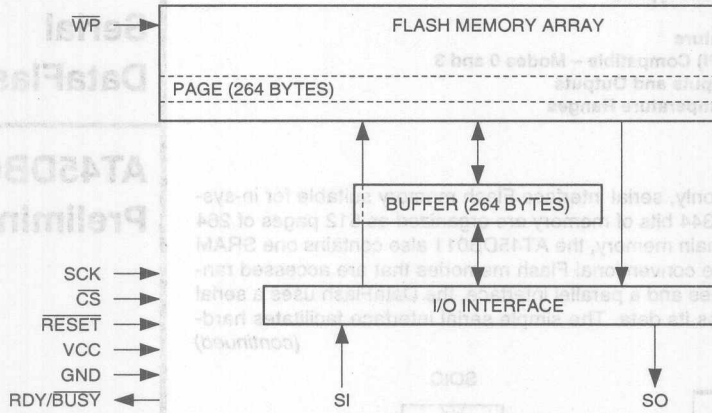
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ware layout, increases system reliability, minimizes switching noise, and reduces package size and active pin count. The device is optimized for use in many commercial and industrial applications where high density, low pin count, low voltage, and low power are essential. Typical applications for the DataFlash are digital voice storage, image storage, and data storage. The device operates at clock frequencies up to 13 MHz with a typical active read current consumption of 4 mA.

To allow for simple in-system reprogrammability, the AT45DB011 does not require high input voltages for programming. The device operates from a single power supply, 2.7V to 3.6V, for both the program and read operations. The AT45DB011 is enabled through the chip select pin ($\overline{CS}$) and accessed via a three-wire interface consisting of the Serial Input (SI), Serial Output (SO), and the Serial Clock (SCK).

All programming cycles are self-timed, and no separate erase cycle is required before programming.

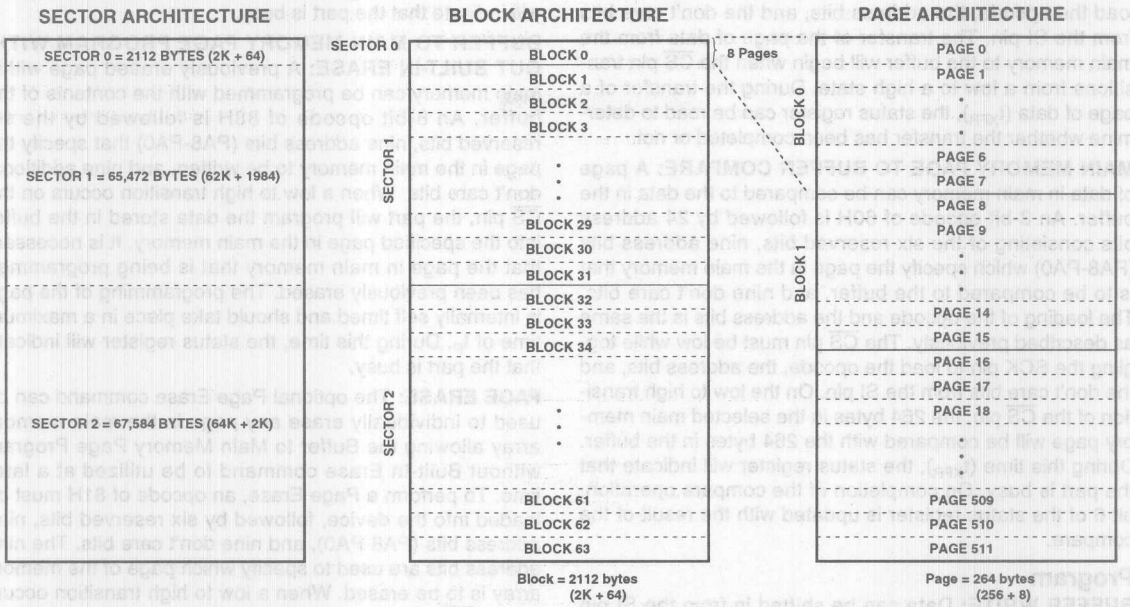
Block Diagram



Memory Array

To provide optimal flexibility, the memory array of the AT45DB011 is divided into three levels of granularity comprising of sectors, blocks, and pages. The Memory Architecture Diagram illustrates the breakdown of each level and details the number of pages per sector and block. All program operations to the DataFlash occur on a page by page basis; however, the optional erase operations can be performed at the block or page level.

Memory Architecture Diagram



Device Operation

The device operation is controlled by instructions from the host processor. The list of instructions and their associated opcodes are contained in Tables 1 and 2. A valid instruction starts with the falling edge of $\overline{CS}$ followed by the appropriate 8-bit opcode and the desired buffer or main memory address location. While the $\overline{CS}$ pin is low, toggling the SCK pin controls the loading of the opcode and the desired buffer or main memory address location through the SI (serial input) pin. All instructions, addresses, and data are transferred with the most significant bit (MSB) first.

Read

By specifying the appropriate opcode, data can be read from the main memory or from the data buffer.

MAIN MEMORY PAGE READ: A main memory read allows the user to read data directly from any one of the 512 pages in the main memory, bypassing the data buffer and leaving the contents of the buffer unchanged. To start a page read, the 8-bit opcode, 52H, is followed by 24 address bits and 32 don't care bits. In the AT45DB011, the first six address bits are reserved for larger density devices (see Notes on page 9), the next nine address bits (PA8-PA0) specify the page address, and the next nine address bits (BA8-BA0) specify the starting byte address within the page. The 32 don't care bits which follow the 24 address bits are sent to initialize the read operation. Following the 32 don't care bits, additional pulses on SCK result in serial data being output on the SO (serial output) pin. The $\overline{CS}$ pin must remain low during the loading of the opcode, the address bits, and the reading of data. When the end of a page in main memory is reached during a main memory page read, the device will continue reading at the beginning of the same page. A low to high transition on the $\overline{CS}$ pin will terminate the read operation and tri-state the SO pin.

BUFFER READ: Data can be read from the data buffer using an opcode of 54H. To perform a buffer read, the eight bits of the opcode must be followed by 15 don't care bits, nine address bits, and eight don't care bits. Since the buffer size is 264-bytes, nine address bits (BFA8-BFA0) are required to specify the first byte of data to be read from the buffer. The $\overline{CS}$ pin must remain low during the loading of the opcode, the address bits, the don't care bits, and the reading of data. When the end of the buffer is reached, the device will continue reading back at the beginning of the buffer. A low to high transition on the $\overline{CS}$ pin will terminate the read operation and tri-state the SO pin.

MAIN MEMORY PAGE TO BUFFER TRANSFER: A page of data can be transferred from the main memory to buffer. An 8-bit opcode of 53H is followed by the six reserved bits, nine address bits (PA8-PA0) which specify the page in

main memory that is to be transferred, and nine don't care bits. The $\overline{CS}$ pin must be low while toggling the SCK pin to load the opcode, the address bits, and the don't care bits from the SI pin. The transfer of the page of data from the main memory to the buffer will begin when the $\overline{CS}$ pin transitions from a low to a high state. During the transfer of a page of data (t_{XFR}), the status register can be read to determine whether the transfer has been completed or not.

MAIN MEMORY PAGE TO BUFFER COMPARE: A page of data in main memory can be compared to the data in the buffer. An 8-bit opcode of 60H is followed by 24 address bits consisting of the six reserved bits, nine address bits (PA8-PA0) which specify the page in the main memory that is to be compared to the buffer, and nine don't care bits. The loading of the opcode and the address bits is the same as described previously. The $\overline{CS}$ pin must be low while toggling the SCK pin to load the opcode, the address bits, and the don't care bits from the SI pin. On the low to high transition of the $\overline{CS}$ pin, the 264 bytes in the selected main memory page will be compared with the 264 bytes in the buffer. During this time (t_{XFR}), the status register will indicate that the part is busy. On completion of the compare operation, bit 6 of the status register is updated with the result of the compare.

Program

BUFFER WRITE: Data can be shifted in from the SI pin into the data buffer. To load data into the buffer, an 8-bit opcode of 84H is followed by 15 don't care bits and nine address bits (BFA8-BFA0). The nine address bits specify the first byte in the buffer to be written. The data is entered following the address bits. If the end of the data buffer is reached, the device will wrap around back to the beginning of the buffer. Data will continue to be loaded into the buffer until a low to high transition is detected on the $\overline{CS}$ pin.

BUFFER TO MAIN MEMORY PAGE PROGRAM WITH BUILT-IN ERASE: Data written into the buffer can be programmed into the main memory. An 8-bit opcode of 83H is followed by the six reserved bits, nine address bits (PA8-PA0) that specify the page in the main memory to be written, and nine additional don't care bits. When a low to high transition occurs on the $\overline{CS}$ pin, the part will first erase the selected page in main memory to all 1s and then program the data stored in the buffer into the specified page in the main memory. Both the erase and the programming of the page are internally self timed and should take place in a maximum time of t_{EP}. During this time, the status register will indicate that the part is busy.

BUFFER TO MAIN MEMORY PAGE PROGRAM WITHOUT BUILT-IN ERASE: A previously erased page within main memory can be programmed with the contents of the buffer. An 8-bit opcode of 88H is followed by the six reserved bits, nine address bits (PA8-PA0) that specify the page in the main memory to be written, and nine additional don't care bits. When a low to high transition occurs on the $\overline{CS}$ pin, the part will program the data stored in the buffer into the specified page in the main memory. It is necessary that the page in main memory that is being programmed has been previously erased. The programming of the page is internally self timed and should take place in a maximum time of t_P. During this time, the status register will indicate that the part is busy.

PAGE ERASE: The optional Page Erase command can be used to individually erase any page in the main memory array allowing the Buffer to Main Memory Page Program without Built-In Erase command to be utilized at a later time. To perform a Page Erase, an opcode of 81H must be loaded into the device, followed by six reserved bits, nine address bits (PA8-PA0), and nine don't care bits. The nine address bits are used to specify which page of the memory array is to be erased. When a low to high transition occurs on the $\overline{CS}$ pin, the part will erase the selected page to 1s. The erase operation is internally self-timed and should take place in a maximum time of t_{PE}. During this time, the status register will indicate that the part is busy.

BLOCK ERASE: A block of eight pages can be erased at one time allowing the Buffer to Main Memory Page Program without Built-In Erase command to be utilized to reduce programming times when writing large amounts of data to the device. To perform a Block Erase, an opcode of 50H must be loaded into the device, followed by six reserved bits, six address bits (PA8-PA3), and 12 don't care bits. The six address bits are used to specify which block of eight pages is to be erased. When a low to high transition occurs on the $\overline{CS}$ pin, the part will erase the selected block of eight pages to 1s. The erase operation is internally self-timed and should take place in a maximum time of t_{BE}. During this time, the status register will indicate that the part is busy.

Block Erase Addressing

PA8	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	Block
0	0	0	0	0	0	X	X	X	0
0	0	0	0	0	1	X	X	X	1
0	0	0	0	1	0	X	X	X	2
0	0	0	0	1	1	X	X	X	3
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
1	1	1	1	0	0	X	X	X	60
1	1	1	1	0	1	X	X	X	61
1	1	1	1	1	0	X	X	X	62
1	1	1	1	1	1	X	X	X	63

MAIN MEMORY PAGE PROGRAM: This operation is a combination of the Buffer Write and Buffer to Main Memory Page Program with Built-In Erase operations. Data is first shifted into the buffer from the SI pin and then programmed into a specified page in the main memory. An 8-bit opcode of 82H is followed by the six reserved bits and 18 address bits. The nine most significant address bits (PA8-PA0) select the page in the main memory where data is to be written, and the next nine address bits (BFA8-BFA0) select the first byte in the buffer to be written. After all address bits are shifted in, the part will take data from the SI pin and store it in the data buffer. If the end of the buffer is reached, the device will wrap around back to the beginning of the buffer. When there is a low to high transition on the $\overline{CS}$ pin, the part will first erase the selected page in main memory to all 1s and then program the data stored in the buffer into the specified page in the main memory. Both the erase and the programming of the page are internally self timed and should take place in a maximum of time t_{EP}. During this time, the status register will indicate that the part is busy.

AUTO PAGE REWRITE: This mode is only needed if multiple bytes within a page or multiple pages of data are modified in a random fashion. This mode is a combination of two operations: Main Memory Page to Buffer Transfer and Buffer to Main Memory Page Program with Built-In Erase. A page of data is first transferred from the main memory to the data buffer, and then the same data (from the buffer) is programmed back into its original page of main memory. An 8-bit opcode of 58H is followed by the six reserved bits, nine address bits (PA8-PA0) that specify the page in main memory to be rewritten, and nine additional don't care bits. When a low to high transition occurs on the $\overline{CS}$ pin, the part will first transfer data from the page in main memory to the buffer and then program the data from the buffer back into same page of main memory. The operation is internally self-timed and should take place in a maximum time of t_{EP}. During this time, the status register will indicate that the part is busy.

If a sector is programmed or reprogrammed sequentially page by page, then the programming algorithm shown in Figure 1 is recommended. Otherwise, if multiple bytes in a page or several pages are programmed randomly in a sector, then the programming algorithm shown in Figure 2 is recommended.

STATUS REGISTER: The status register can be used to determine the device's ready/busy status, the result of a Main Memory Page to Buffer Compare operation, or the device density. To read the status register, an opcode of 57H must be loaded into the device. After the last bit of the opcode is shifted in, the eight bits of the status register, starting with the MSB (bit 7), will be shifted out on the SO pin during the next eight clock cycles. The five most-significant bits of the status register will contain device information, while the remaining three least-significant bits are reserved for future use and will have undefined values. After bit 0 of the status register has been shifted out, the sequence will repeat itself (as long as $\overline{CS}$ remains low and SCK is being toggled) starting again with bit 7. The data in the status register is constantly updated, so each repeating sequence will output new data.

Ready/busy status is indicated using bit 7 of the status register. If bit 7 is a 1, then the device is not busy and is ready to accept the next command. If bit 7 is a 0, then the device is in a busy state. The user can continuously poll bit 7 of the status register by stopping SCK once bit 7 has been output. The status of bit 7 will continue to be output on the SO pin, and once the device is no longer busy, the state of SO will change from 0 to 1. There are eight operations which can cause the device to be in a busy state: Main Memory Page to Buffer Transfer, Main Memory Page to Buffer Compare,

Buffer to Main Memory Page Program with Built-In Erase, Buffer to Main Memory Page Program without Built-In Erase, Page Erase, Block Erase, Main Memory Page Program, and Auto Page Rewrite.

The result of the most recent Main Memory Page to Buffer Compare operation is indicated using bit 6 of the status register. If bit 6 is a 0, then the data in the main memory page matches the data in the buffer. If bit 6 is a 1, then at least one bit of the data in the main memory page does not match the data in the buffer.

The device density is indicated using bits 5, 4, and 3 of the status register. For the AT45DB011, the three bits are 0, 0, and 1. The decimal value of these three binary bits does not equate to the device density; the three bits represent a combinational code relating to differing densities of Serial DataFlash devices, allowing a total of eight different density configurations.

HARDWARE PAGE WRITE PROTECT: If the $\overline{WP}$ pin is held low, the first 256 pages of the main memory cannot be reprogrammed. The only way to reprogram the first 256 pages is to first drive the protect pin high and then use the program commands previously mentioned. The $\overline{WP}$ pin is internally pulled high; therefore, in low pin count applications, connection of the $\overline{WP}$ pin is not necessary if this pin and feature will not be utilized. However, it is recommended that the $\overline{WP}$ pin be driven high externally whenever possible.

$\overline{RESET}$: A low state on the reset pin ($\overline{RESET}$) will terminate the operation in progress and reset the internal state machine to an idle state. The device will remain in the reset condition as long as a low level is present on the $\overline{RESET}$ pin. Normal operation can resume once the $\overline{RESET}$ pin is brought back to a high level.

The device incorporates an internal power-on reset circuit, so there are no restrictions on the $\overline{RESET}$ pin during power-on sequences. The $\overline{RESET}$ pin is also internally pulled high; therefore, in low pin count applications, connection of the $\overline{RESET}$ pin is not necessary if this pin and feature will not be utilized. However, it is recommended that the $\overline{RESET}$ pin be driven high externally whenever possible.

READY/$\overline{BUSY}$: This open drain output pin will be driven low when the device is busy in an internally self-timed operation. This pin, which is normally in a high state (through an external pull-up resistor), will be pulled low during programming operations, compare operations, and during page-to-buffer transfers.

The busy status indicates that the Flash memory array and the buffer cannot be accessed.

Power On/Reset State

When power is first applied to the device, or when recovering from a reset condition, the device will default to SPI mode 3. In addition, the SO pin will be in a high impedance state, and a high to low transition on the $\overline{CS}$ pin will be required to start a valid instruction. The SPI mode will be automatically selected on every falling edge of $\overline{CS}$ by sampling the inactive clock state.

Status Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RDY/$\overline{BUSY}$	COMP	0	0	1	X	X	X

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC and AC Operating Range

		AT45DB011
Operating Temperature (Case)	Com.	0°C to 70°C
	Ind.	-40°C to 85°C
V_{CC} Power Supply[1]		2.7V to 3.6V

Note: 1. After power is applied and V_{CC} is at the minimum specified data sheet value, the system should wait 20 ms before an operational mode is started.

DC Characteristics

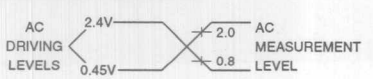
Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{SB}	Standby Current	$\overline{CS}$, $\overline{RESET}$, $\overline{WP}$ = V_{IH}, all inputs at CMOS levels		2	10	µA
I_{CC1}	Active Current, Read Operation	f = 13 MHz; I_{OUT} = 0 mA; V_{CC} = 3.6V		4	10	mA
I_{CC2}	Active Current, Program/Erase Operation	V_{CC} = 3.6V		10	25	mA
I_{LI}	Input Load Current	V_{IN} = CMOS levels			1	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = CMOS levels			1	µA
V_{IL}	Input Low Voltage				0.6	V
V_{IH}	Input High Voltage		2.0			V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA; V_{CC} = 2.7V			0.4	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA	V_{CC} - 0.2V			V

4

AC Characteristics

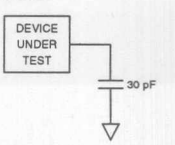
Symbol	Parameter	Min	Typ	Max	Units
f_{SCK}	SCK Frequency			13	MHz
t_{WH}	SCK High Time	35			ns
t_{WL}	SCK Low Time	35			ns
t_{CS}	Minimum $\overline{CS}$ High Time	250			ns
t_{CSS}	$\overline{CS}$ Setup Time	250			ns
t_{CSH}	$\overline{CS}$ Hold Time	250			ns
t_{CSB}	$\overline{CS}$ High to RDY/$\overline{BUSY}$ Low			200	ns
t_{SU}	Data In Setup Time	10			ns
t_H	Data In Hold Time	20			ns
t_{HO}	Output Hold Time	0			ns
t_{DIS}	Output Disable Time			25	ns
t_V	Output Valid			30	ns
t_{XFR}	Page to Buffer Transfer/Compare Time		120	200	µs
t_{EP}	Page Erase and Programming Time		10	20	ms
t_P	Page Programming Time		7	15	ms
t_{PE}	Page Erase Time		6	10	ms
t_{BE}	Block Erase Time		7	15	ms
t_{RST}	$\overline{RESET}$ Pulse Width	10			µs
t_{REC}	$\overline{RESET}$ Recovery Time			1	µs

Input Test Waveforms and Measurement Levels



t_R, t_F < 5 ns (10% to 90%)

Output Test Load

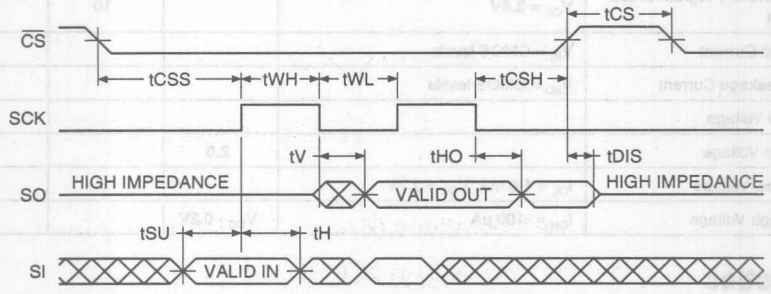


AC Waveforms

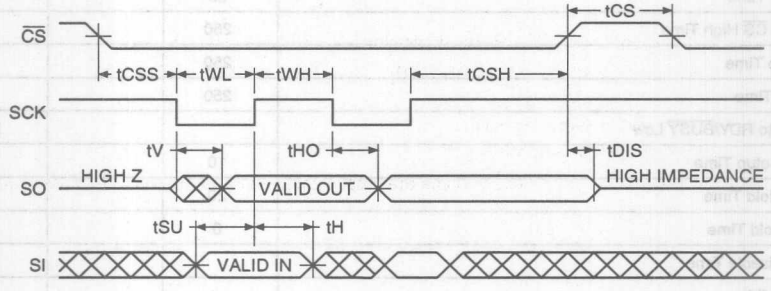
Two different timing diagrams are shown below. Waveform 1 shows the SCK signal being low when $\overline{CS}$ makes a high-to-low transition, and Waveform 2 shows the SCK signal being high when $\overline{CS}$ makes a high-to-low transition. Both waveforms show valid timing diagrams. The setup and hold times for the SI signal are referenced to the low-to-high transition on the SCK signal.

Waveform 1 shows timing that is also compatible with SPI Mode 0, and Waveform 2 shows timing that is compatible with SPI Mode 3.

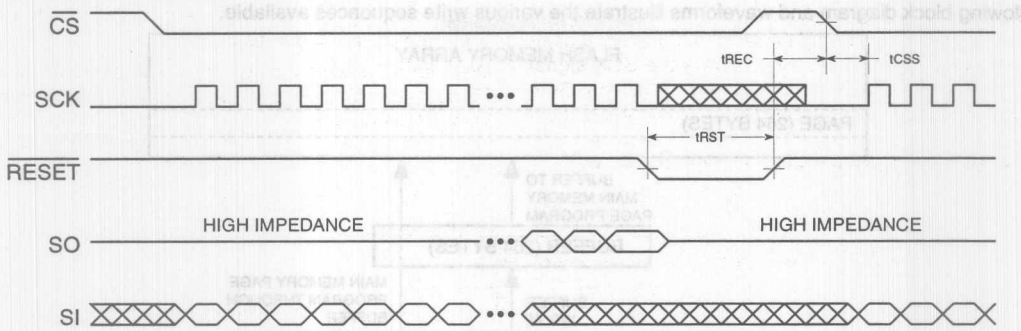
Waveform 1 – Inactive Clock Polarity Low



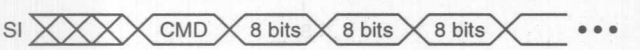
Waveform 2 – Inactive Clock Polarity High

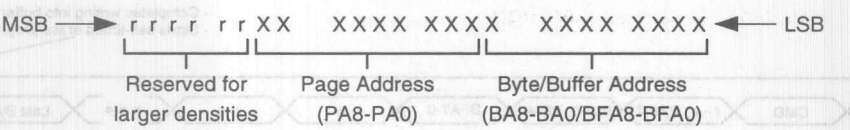


Reset Timing (Inactive Clock Polarity Low Shown)



Command Sequence for Read/Write Operations (Except Status Register Read)

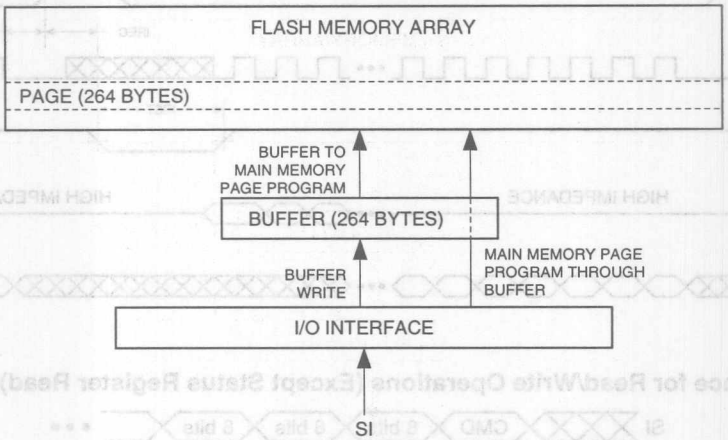




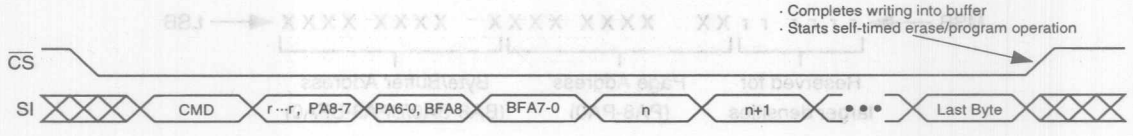
Notes: 1. "r" designates bits reserved for larger densities.
2. It is recommended that "r" be a logical "0".
3. For densities larger than 1M bit, the "r" bits become the most significant Page Address bit for the appropriate density.

Write Operations

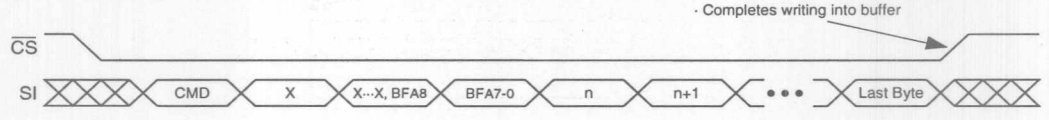
The following block diagram and waveforms illustrate the various write sequences available.



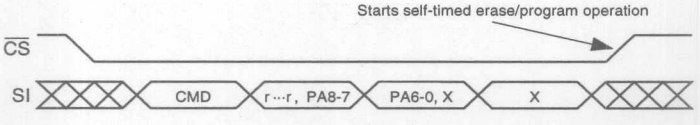
Main Memory Page Program through Buffer



Buffer Write



Buffer to Main Memory Page Program (Data from Buffer Programmed into Flash Page)

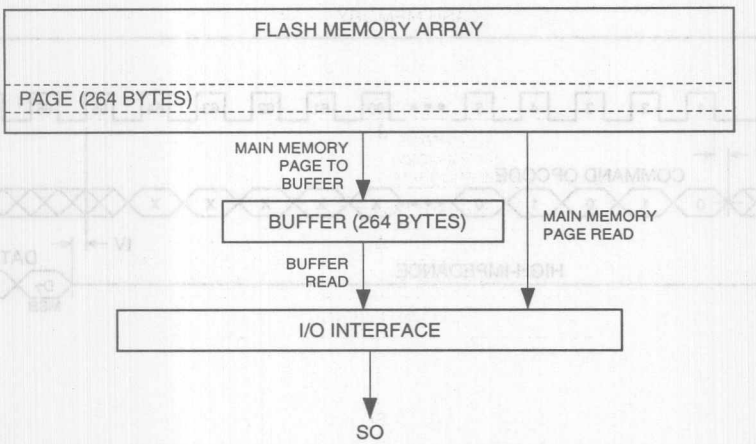


Each transition represents 8 bits and 8 clock cycles

n = 1st byte written
n+1 = 2nd byte written

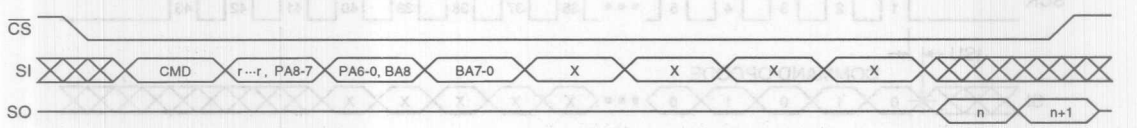
Read Operations

The following block diagram and waveforms illustrate the various read sequences available.

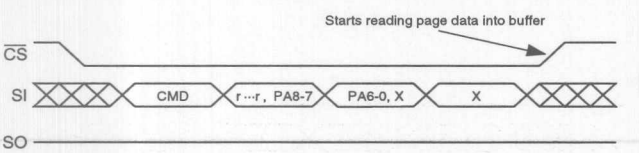


4

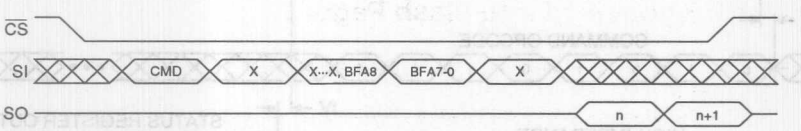
Main Memory Page Read



Main Memory Page to Buffer Transfer (Data from Flash Page Read into Buffer)



Buffer Read

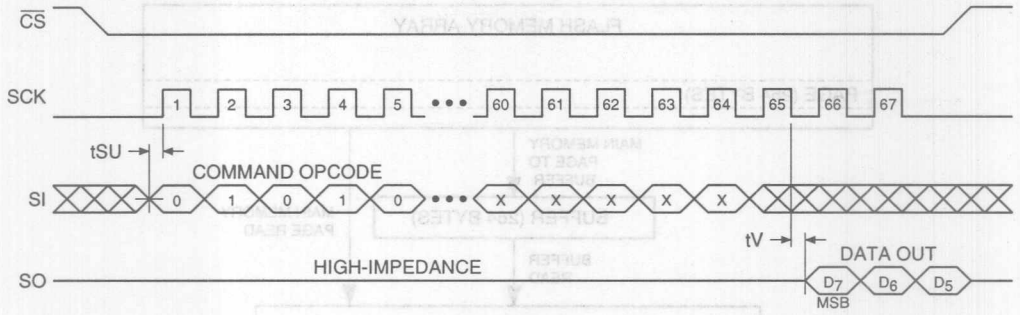


Each transition represents 8 bits and 8 clock cycles

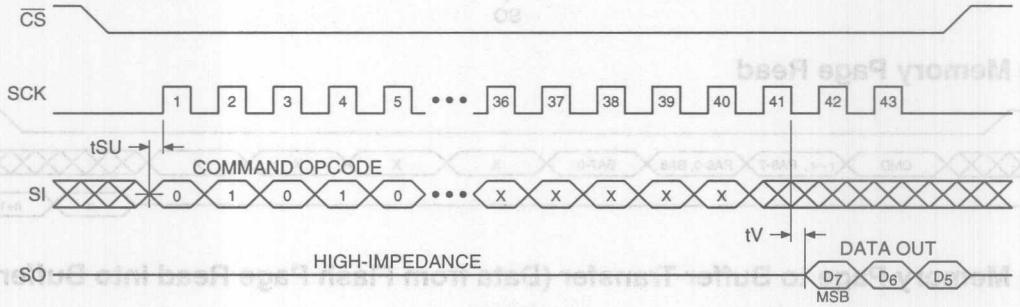
n = 1st byte read
n+1 = 2nd byte read

Detailed Bit-Level Read Timing – Inactive Clock Polarity Low

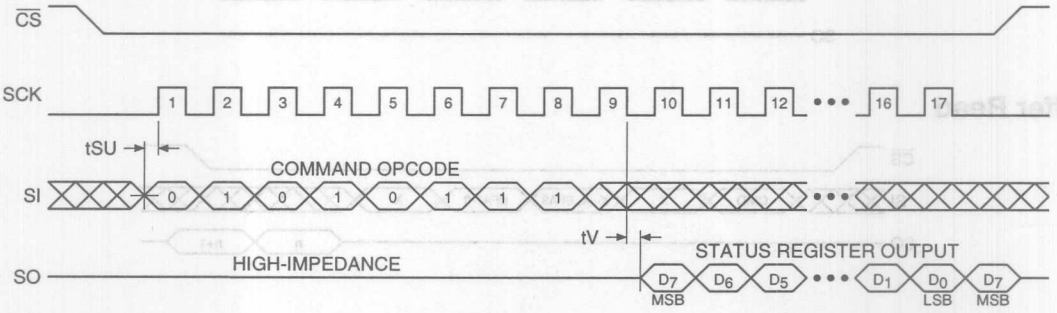
Main Memory Page Read



Buffer Read

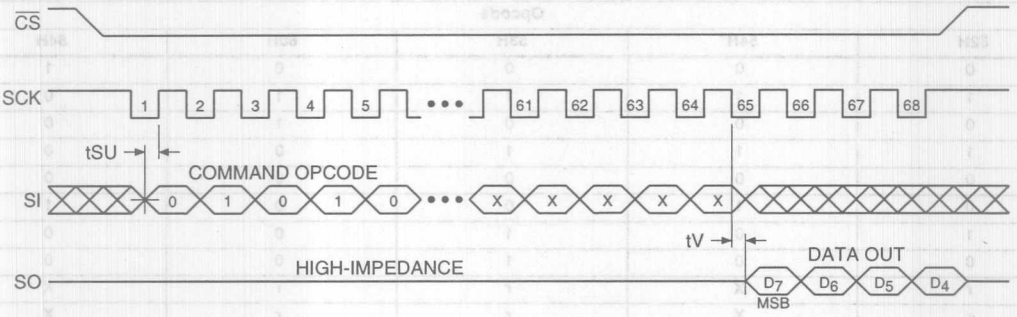


Status Register Read

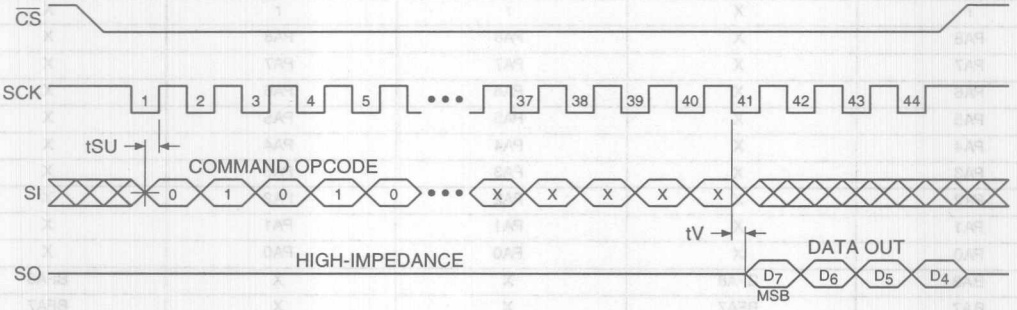


Detailed Bit-Level Read Timing – Inactive Clock Polarity High

Main Memory Page Read



Buffer Read



Status Register Read

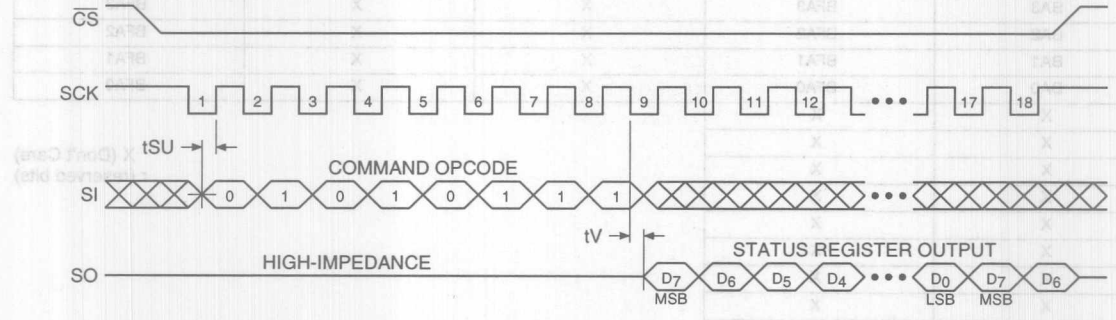


Table 1.

Main Memory Page Read	Buffer Read	Main Memory Page to Buffer Transfer	Main Memory Page to Buffer Compare	Buffer Write
Opcode				
52H	54H	53H	60H	84H
0	0	0	0	1
1	1	1	1	0
0	0	0	1	0
1	1	1	0	0
0	0	0	0	0
0	1	0	0	1
1	0	1	0	0
0	0	1	0	0
r	X	r	r	X
r	X	r	r	X
r	X	r	r	X
r	X	r	r	X
r	X	r	r	X
r	X	r	r	X
PA8	X	PA8	PA8	X
PA7	X	PA7	PA7	X
PA6	X	PA6	PA6	X
PA5	X	PA5	PA5	X
PA4	X	PA4	PA4	X
PA3	X	PA3	PA3	X
PA2	X	PA2	PA2	X
PA1	X	PA1	PA1	X
PA0	X	PA0	PA0	X
BA8	BFA8	X	X	BFA8
BA7	BFA7	X	X	BFA7
BA6	BFA6	X	X	BFA6
BA5	BFA5	X	X	BFA5
BA4	BFA4	X	X	BFA4
BA3	BFA3	X	X	BFA3
BA2	BFA2	X	X	BFA2
BA1	BFA1	X	X	BFA1
BA0	BFA0	X	X	BFA0
X	X			
X	X			
X	X			
X	X			
X	X			
X	X			
X	X			
X	X			
•				
•				
•				
X (64th bit)				

X (Don't Care)
r (reserved bits)

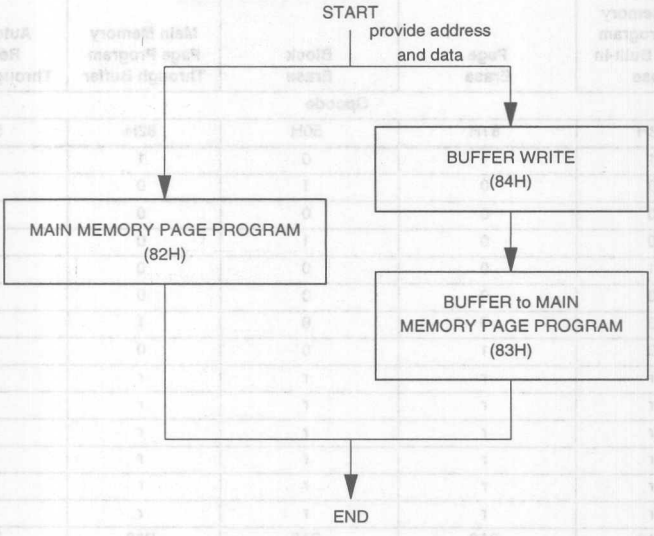
Table 2.

Buffer to Main Memory Page Program with Built-In Erase	Buffer to Main Memory Page Program without Built-In Erase	Page Erase	Block Erase	Main Memory Page Program Through Buffer	Auto Page Rewrite Through Buffer	Status Register
Opcode						
83H	88H	81H	50H	82H	58H	57H
1	1	1	0	1	0	0
0	0	0	1	0	1	1
0	0	0	0	0	0	0
0	0	0	1	0	1	1
0	1	0	0	0	1	0
0	0	0	0	0	0	1
1	0	0	0	1	0	1
1	0	1	0	0	0	1
r	r	r	r	r	r	
r	r	r	r	r	r	
r	r	r	r	r	r	
r	r	r	r	r	r	
r	r	r	r	r	r	
r	r	r	r	r	r	
PA8	PA8	PA8	PA8	PA8	PA8	
PA7	PA7	PA7	PA7	PA7	PA7	
PA6	PA6	PA6	PA6	PA6	PA6	
PA5	PA5	PA5	PA5	PA5	PA5	
PA4	PA4	PA4	PA4	PA4	PA4	
PA3	PA3	PA3	PA3	PA3	PA3	
PA2	PA2	PA2	X	PA2	PA2	
PA1	PA1	PA1	X	PA1	PA1	
PA0	PA0	PA0	X	PA0	PA0	
X	X	X	X	BFA8	X	
X	X	X	X	BFA7	X	
X	X	X	X	BFA6	X	
X	X	X	X	BFA5	X	
X	X	X	X	BFA4	X	
X	X	X	X	BFA3	X	
X	X	X	X	BFA2	X	
X	X	X	X	BFA1	X	
X	X	X	X	BFA0	X	

X (Don't Care)
r (reserved bits)

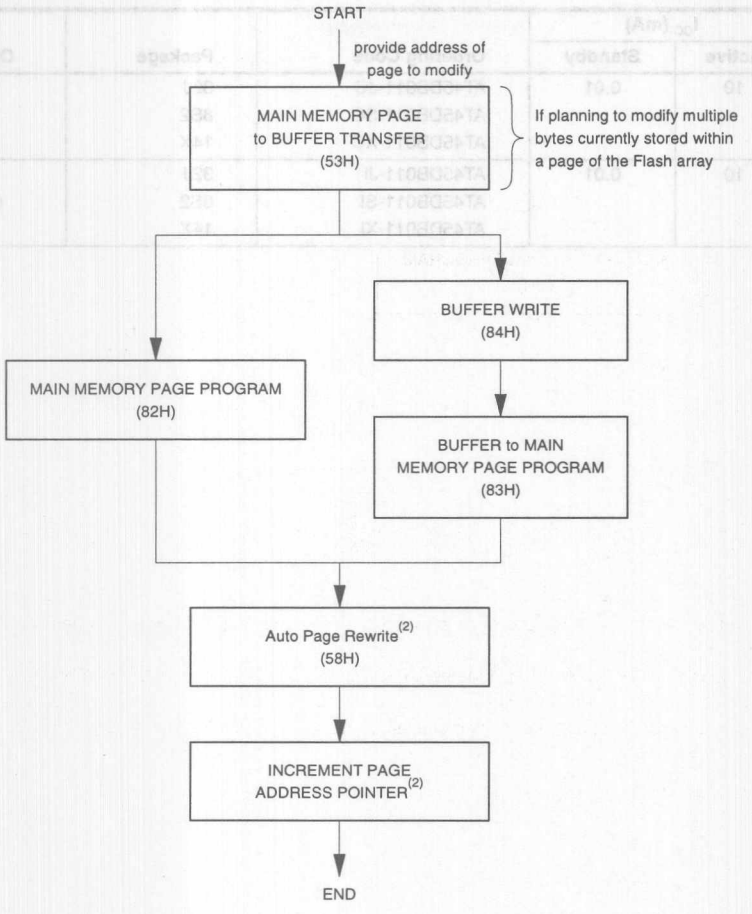
4

Figure 1. Algorithm for Programming or Reprogramming of the Entire Array Sequentially



Notes:
1. This type of algorithm is used for applications in which the entire array is programmed sequentially, filling the array page-by-page.
2. A page can be written using either a Main Memory Page Program operation or a Buffer Write operation followed by a Buffer to Main Memory Page Program operation.
3. The algorithm above shows the programming of a single page. The algorithm will be repeated sequentially for each page within the entire array.

Figure 2. Algorithm for Randomly Modifying Data



Notes:
1. To preserve data integrity, each page of a DataFlash sector must be updated/rewritten at least once within every 10,000 cumulative page erase/program operations within that sector.
2. A Page Address Pointer must be maintained to indicate which page is to be rewritten. The Auto Page Rewrite command must use the address specified by the Page Address Pointer.
3. Other algorithms can be used to rewrite portions of the Flash array. Low power applications may choose to wait until 10,000 cumulative page erase/program operations have accumulated before rewriting all pages of the sector. See application note AN-4 ("Using Atmel's Serial DataFlash") for more details.

Sector Addressing

PA8	PA7	PA6	PA5	PA4	PA3	PA2-PA0	Sector
0	0	0	0	0	0	X	0
0	X	X	X	X	X	X	1
1	X	X	X	X	X	X	2

Ordering Information

f_{SCK} (MHz)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
13	10	0.01	AT45DB011-JC AT45DB011-SC AT45DB011-XC	32J 8S2 14X	Commercial (0°C to 70°C)
13	10	0.01	AT45DB011-JI AT45DB011-SI AT45DB011-XI	32J 8S2 14X	Industrial (-40°C to 85°C)

Package Type	
32J	32-Lead, Plastic J-Leaded Chip Carrier (PLCC)
8S2	8-Lead, 0.210" Wide, Plastic Gull Wing Small Outline (EIAJ SOIC)
14X	14-Lead, 0.170" Wide, Plastic Thin Shrink Small Outline Package (TSSOP)

Features

- Single 2.7V - 3.6V Supply
- Serial Interface Architecture
- Page Program Operation
  - Single Cycle Reprogram (Erase and Program)
  - 1024 Pages (264 Bytes/Page) Main Memory
- Two 264-Byte SRAM Data Buffers – Allows Receiving of Data while Reprogramming of Non-Volatile Memory
- Internal Program and Control Timer
- Fast Page Program Time – 7 ms Typical
- 120 µs Typical Page to Buffer Transfer Time
- Low Power Dissipation
  - 4 mA Active Read Current Typical
  - 5 µA CMOS Standby Current Typical
- 5 MHz Max Clock Frequency
- Hardware Data Protection Feature
- Serial Peripheral Interface (SPI) Compatible – Modes 0 and 3
- CMOS and TTL Compatible Inputs and Outputs
- Commercial and Industrial Temperature Ranges

Description

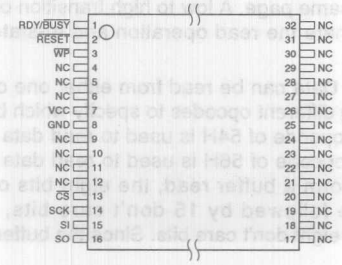
The AT45DB021 is a 2.7-volt only, serial interface Flash memory suitable for in-system reprogramming. Its 2,162,688 bits of memory are organized as 1024 pages of 264-bytes each. In addition to the main memory, the AT45DB021 also contains two SRAM data buffers of 264-bytes each. The buffers allow receiving of data while a page in the main memory is being reprogrammed. Unlike conventional Flash memories that are accessed randomly with multiple address lines and a parallel interface,

(continued)

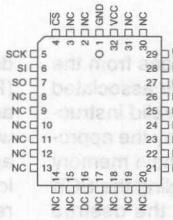
Pin Configurations

Pin Name	Function
$\overline{CS}$	Chip Select
SCK	Serial Clock
SI	Serial Input
SO	Serial Output
$\overline{WP}$	Hardware Page Write Protect Pin
$\overline{RESET}$	Chip Reset
RDY/$\overline{BUSY}$	Ready/Busy

TSOP Top View
Type 1

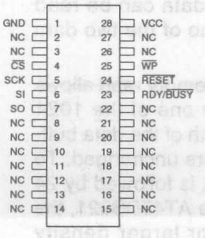


PLCC



Note: PLCC package pins 16 and 17 are DON'T CONNECT.

SOIC



2-Megabit 2.7-volt Only Serial DataFlash®

4

AT45DB021

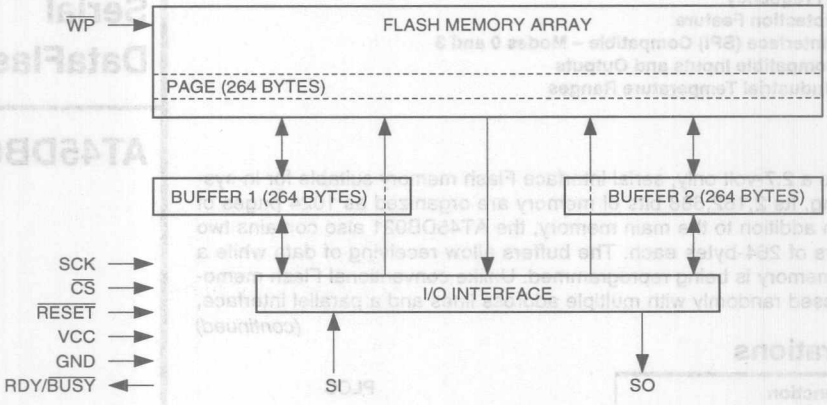
Rev. 0868B–10/98

the DataFlash uses a serial interface to sequentially access its data. The simple serial interface facilitates hardware layout, increases system reliability, minimizes switching noise, and reduces package size and active pin count. The device is optimized for use in many commercial and industrial applications where high density, low pin count, low voltage, and low power are essential. Typical applications for the DataFlash are digital voice storage, image storage, and data storage. The device operates at clock frequencies up to 5 MHz with a typical active read current consumption of 4 mA.

To allow for simple in-system reprogrammability, the AT45DB021 does not require high input voltages for programming. The device operates from a single power supply, 2.7V to 3.6V, for both the program and read operations. The AT45DB021 is enabled through the chip select pin ($\overline{CS}$) and accessed via a three-wire interface consisting of the Serial Input (SI), Serial Output (SO), and the Serial Clock (SCK).

All programming cycles are self-timed, and no separate erase cycle is required before programming.

Block Diagram



Device Operation

The device operation is controlled by instructions from the host processor. The list of instructions and their associated opcodes are contained in Tables 1 and 2. A valid instruction starts with the falling edge of $\overline{CS}$ followed by the appropriate 8-bit opcode and the desired buffer or main memory address location. While the $\overline{CS}$ pin is low, toggling the SCK pin controls the loading of the opcode and the desired buffer or main memory address location through the SI (serial input) pin. All instructions, addresses, and data are transferred with the most significant bit (MSB) first.

Read

By specifying the appropriate opcode, data can be read from the main memory or from either one of the two data buffers.

MAIN MEMORY PAGE READ: A main memory read allows the user to read data directly from any one of the 1024 pages in the main memory, bypassing both of the data buffers and leaving the contents of the buffers unchanged. To start a page read, the 8-bit opcode, 52H, is followed by 24 address bits and 32 don't care bits. In the AT45DB021, the first five address bits are reserved for larger density devices (see Notes on page 28), the next 10 address bits (PA9-PA0) specify the page address, and the next nine address bits (BA8-BA0) specify the starting byte address within the page. The 32 don't care bits which follow the 24 address bits are sent to initialize the read operation. Following the 32 don't care bits, additional pulses on SCK result in serial data being output on the SO (serial output) pin. The $\overline{CS}$ pin must remain low during the loading of the opcode, the address bits, and the reading of data. When the end of a page in main memory is reached during a main memory page read, the device will continue reading at the beginning of the same page. A low to high transition on the $\overline{CS}$ pin will terminate the read operation and tri-state the SO pin.

BUFFER READ: Data can be read from either one of the two buffers, using different opcodes to specify which buffer to read from. An opcode of 54H is used to read data from buffer 1, and an opcode of 56H is used to read data from buffer 2. To perform a buffer read, the eight bits of the opcode must be followed by 15 don't care bits, nine address bits, and eight don't care bits. Since the buffer size

is 264-bytes, nine address bits (BFA8-BFA0) are required to specify the first byte of data to be read from the buffer. The $\overline{CS}$ pin must remain low during the loading of the opcode, the address bits, the don't care bits, and the reading of data. When the end of a buffer is reached, the device will continue reading back at the beginning of the buffer. A low to high transition on the $\overline{CS}$ pin will terminate the read operation and tri-state the SO pin.

MAIN MEMORY PAGE TO BUFFER TRANSFER: A page of data can be transferred from the main memory to either buffer 1 or buffer 2. An 8-bit opcode, 53H for buffer 1 and 55H for buffer 2, is followed by the five reserved bits, 10 address bits (PA9-PA0) which specify the page in main memory that is to be transferred, and nine don't care bits. The $\overline{CS}$ pin must be low while toggling the SCK pin to load the opcode, the address bits, and the don't care bits from the SI pin. The transfer of the page of data from the main memory to the buffer will begin when the $\overline{CS}$ pin transitions from a low to a high state. During the transfer of a page of data (t_{XFR}), the status register can be read to determine whether the transfer has been completed or not.

MAIN MEMORY PAGE TO BUFFER COMPARE: A page of data in main memory can be compared to the data in buffer 1 or buffer 2. An 8-bit opcode, 60H for buffer 1 and 61H for buffer 2, is followed by 24 address bits consisting of the five reserved bits, 10 address bits (PA9-PA0) which specify the page in the main memory that is to be compared to the buffer, and nine don't care bits. The loading of the opcode and the address bits is the same as described previously. The $\overline{CS}$ pin must be low while toggling the SCK pin to load the opcode, the address bits, and the don't care bits from the SI pin. On the low to high transition of the $\overline{CS}$ pin, the 264 bytes in the selected main memory page will be compared with the 264 bytes in buffer 1 or buffer 2. During this time (t_{XFR}), the status register will indicate that the part is busy. On completion of the compare operation, bit 6 of the status register is updated with the result of the compare.

Program

BUFFER WRITE: Data can be shifted in from the SI pin into either buffer 1 or buffer 2. To load data into either buffer, an 8-bit opcode, 84H for buffer 1 or 87H for buffer 2, is followed by 15 don't care bits and nine address bits (BFA8-BFA0). The nine address bits specify the first byte in the buffer to be written. The data is entered following the address bits. If the end of the data buffer is reached, the device will wrap around back to the beginning of the buffer. Data will continue to be loaded into the buffer until a low to high transition is detected on the $\overline{CS}$ pin.

BUFFER TO MAIN MEMORY PAGE PROGRAM WITH BUILT-IN ERASE: Data written into either buffer 1 or buffer 2 can be programmed into the main memory. An 8-bit opcode, 83H for buffer 1 or 86H for buffer 2, is followed by the five reserved bits, 10 address bits (PA9-PA0) that specify the page in the main memory to be written, and nine additional don't care bits. When a low to high transition occurs on the $\overline{CS}$ pin, the part will first erase the selected page in main memory to all 1s and then program the data stored in the buffer into the specified page in the main memory. Both the erase and the programming of the page are internally self timed and should take place in a maximum time of t_{EP}. During this time, the status register will indicate that the part is busy.

BUFFER TO MAIN MEMORY PAGE PROGRAM WITHOUT BUILT-IN ERASE: A previously erased page within main memory can be programmed with the contents of either buffer 1 or buffer 2. An 8-bit opcode, 88H for buffer 1 or 89H for buffer 2, is followed by the five reserved bits, 10 address bits (PA9-PA0) that specify the page in the main memory to be written, and nine additional don't care bits. When a low to high transition occurs on the $\overline{CS}$ pin, the part will program the data stored in the buffer into the specified page in the main memory. It is necessary that the page in main memory that is being programmed has been previously programmed to all 1s (erased state). The programming of the page is internally self timed and should take place in a maximum time of t_P. During this time, the status register will indicate that the part is busy.

MAIN MEMORY PAGE PROGRAM: This operation is a combination of the Buffer Write and Buffer to Main Memory Page Program with Built-In Erase operations. Data is first shifted into buffer 1 or buffer 2 from the SI pin and then programmed into a specified page in the main memory. An 8-bit opcode, 82H for buffer 1 or 85H for buffer 2, is followed by the five reserved bits and 19 address bits. The 10 most significant address bits (PA9-PA0) select the page in the main memory where data is to be written, and the next nine address bits (BFA8-BFA0) select the first byte in the buffer to be written. After all address bits are shifted in, the part will take data from the SI pin and store it in one of the data buffers. If the end of the buffer is reached, the device will wrap around back to the beginning of the buffer. When there is a low to high transition on the $\overline{CS}$ pin, the part will first erase the selected page in main memory to all 1s and then program the data stored in the buffer into the specified page in the main memory. Both the erase and the programming of the page are internally self timed and should take place in a maximum of time t_{EP}. During this time, the status register will indicate that the part is busy.

AUTO PAGE REWRITE: This mode is only needed if multiple bytes within a page or multiple pages of data are modified in a random fashion. This mode is a combination of two operations: Main Memory Page to Buffer Transfer and Buffer to Main Memory Page Program with Built-In Erase. A page of data is first transferred from the main memory to buffer 1 or buffer 2, and then the same data (from buffer 1 or buffer 2) is programmed back into its original page of

main memory. An 8-bit opcode, 58H for buffer 1 or 59H for buffer 2, is followed by the five reserved bits, 10 address bits (PA9-PA0) that specify the page in main memory to be rewritten, and nine additional don't care bits. When a low to high transition occurs on the $\overline{CS}$ pin, the part will first transfer data from the page in main memory to a buffer and then program the data from the buffer back into same page of main memory. The operation is internally self-timed and should take place in a maximum time of t_{EP}. During this time, the status register will indicate that the part is busy.

If the main memory is programmed or reprogrammed sequentially page by page, then the programming algorithm shown in Figure 1 is recommended. Otherwise, if multiple bytes in a page or several pages are programmed randomly in the main memory, then the programming algorithm shown in Figure 2 is recommended.

STATUS REGISTER: The status register can be used to determine the device's ready/busy status, the result of a Main Memory Page to Buffer Compare operation, or the device density. To read the status register, an opcode of 57H must be loaded into the device. After the last bit of the opcode is shifted in, the eight bits of the status register, starting with the MSB (bit 7), will be shifted out on the SO pin during the next eight clock cycles. The five most-significant bits of the status register will contain device information, while the remaining three least-significant bits are reserved for future use and will have undefined values. After bit 0 of the status register has been shifted out, the sequence will repeat itself (as long as $\overline{CS}$ remains low and SCK is being toggled) starting again with bit 7. The data in the status register is constantly updated, so each repeating sequence will output new data.

Ready/busy status is indicated using bit 7 of the status register. If bit 7 is a 1, then the device is not busy and is ready to accept the next command. If bit 7 is a 0, then the device is in a busy state. The user can continuously poll bit 7 of the status register by stopping SCK once bit 7 has been output. The status of bit 7 will continue to be output on the SO pin, and once the device is no longer busy, the state of SO will change from 0 to 1. There are six operations which can cause the device to be in a busy state: Main Memory Page to Buffer Transfer, Main Memory Page to Buffer Compare, Buffer to Main Memory Page Program with Built-In Erase, Buffer to Main Memory Page Program without Built-In Erase, Main Memory Page Program, and Auto Page Rewrite.

The result of the most recent Main Memory Page to Buffer Compare operation is indicated using bit 6 of the status register. If bit 6 is a 0, then the data in the main memory page matches the data in the buffer. If bit 6 is a 1, then at least one bit of the data in the main memory page does not match the data in the buffer.

The device density is indicated using bits 5, 4, and 3 of the status register. For the AT45DB021, the three bits are 0, 1, and 0. The decimal value of these three binary bits does not equate to the device density; the three bits represent a combinational code relating to differing densities of Serial DataFlash devices, allowing a total of eight different density configurations.

Read/Program Mode Summary

The modes listed above can be separated into two groups — modes which make use of the flash memory array (Group A) and modes which do not make use of the flash memory array (Group B).

Group A modes consist of:

1. Main memory page read
2. Main memory page to buffer 1 (or 2) transfer
3. Main memory page to buffer 1 (or 2) compare
4. Buffer 1 (or 2) to main memory page program with built-in erase
5. Buffer 1 (or 2) to main memory page program without built-in erase
6. Main memory page program
7. Auto page rewrite

Group B modes consist of:

1. Buffer 1 (or 2) read
2. Buffer 1 (or 2) write
3. Status read

If a Group A mode is in progress (not fully completed) then another mode in Group A should not be started. However, during this time in which a Group A mode is in progress, modes in Group B can be started.

This gives the Serial DataFlash the ability to virtually accommodate a continuous data stream. While data is being programmed into main memory from buffer 1, data can be loaded into buffer 2 (or vice versa). See application note AN-4 ("Using Atmel's Serial DataFlash") for more details.

HARDWARE PAGE WRITE PROTECT: If the $\overline{WP}$ pin is held low, the first 256 pages of the main memory cannot be reprogrammed. The only way to reprogram the first 256 pages is to first drive the protect pin high and then use the program commands previously mentioned.

Status Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RDY/$\overline{BUSY}$	COMP	0	1	0	X	X	X

RESET: A low state on the reset pin ($\overline{\text{RESET}}$) will terminate the operation in progress and reset the internal state machine to an idle state. The device will remain in the reset condition as long as a low level is present on the $\overline{\text{RESET}}$ pin. Normal operation can resume once the $\overline{\text{RESET}}$ pin is brought back to a high level.

The device also incorporates an internal power-on reset circuit; therefore, there are no restrictions on the $\overline{\text{RESET}}$ pin during power-on sequences.

READY/$\overline{\text{BUSY}}$: This open drain output pin will be driven low when the device is busy in an internally self-timed operation. This pin, which is normally in a high state (through an external pull-up resistor), will be pulled low during programming operations, compare operations, and during page-to-buffer transfers.

The busy status indicates that the Flash memory array and one of the buffers cannot be accessed; read and write operations to the other buffer can still be performed.

Power On/Reset State

When power is first applied to the device, or when recovering from a reset condition, the device will default to SPI mode 3. In addition, the SO pin will be in a high impedance state, and a high to low transition on the $\overline{\text{CS}}$ pin will be required to start a valid instruction. The SPI mode will be automatically selected on every falling edge of $\overline{\text{CS}}$ by sampling the inactive clock state.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC and AC Operating Range

		AT45DB021
Operating Temperature (Case)	Com.	0°C to 70°C
	Ind.	-40°C to 85°C
V_{CC} Power Supply[1]		2.7V to 3.6V

Note: 1. After power is applied and V_{CC} is at the minimum specified data sheet value, the system should wait 20 ms before an operational mode is started.

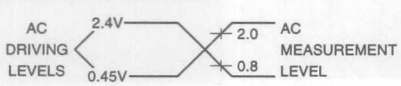
DC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{SB}	Standby Current	$\overline{CS}$, $\overline{RESET}$, $\overline{WP}$ = V_{IH}, all inputs at CMOS levels		5	15	µA
I_{CC1}	Active Current, Read Operation	f = 5 MHz; I_{OUT} = 0 mA; V_{CC} = 3.6V		4	10	mA
I_{CC2}	Active Current, Program/ Erase Operation	V_{CC} = 3.6V		15	35	mA
I_{LI}	Input Load Current	V_{IN} = CMOS Levels			1	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = CMOS levels			1	µA
V_{IL}	Input Low Voltage				0.6	V
V_{IH}	Input High Voltage		2.0			V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA; V_{CC} = 2.7V			0.4	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA	V_{CC} - 0.2V			V

AC Characteristics

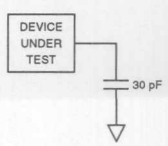
Symbol	Parameter	Min	Typ	Max	Units
f_{SCK}	SCK Frequency			5	MHz
t_{WH}	SCK High Time	80			ns
t_{WL}	SCK Low Time	80			ns
t_{CS}	Minimum $\overline{CS}$ High Time	350			ns
t_{CSS}	$\overline{CS}$ Setup Time	350			ns
t_{CSH}	$\overline{CS}$ Hold Time	350			ns
t_{CSB}	$\overline{CS}$ High to RDY/$\overline{BUSY}$ Low			200	ns
t_{SU}	Data In Setup Time	15			ns
t_H	Data In Hold Time	35			ns
t_{HO}	Output Hold Time	0			ns
t_{DIS}	Output Disable Time			100	ns
t_V	Output Valid			120	ns
t_{XFR}	Page to Buffer Transfer/Compare Time		120	250	µs
t_{EP}	Page Erase and Programming Time		10	20	ms
t_P	Page Programming Time		7	14	ms
t_{RST}	$\overline{RESET}$ Pulse Width	10			µs
t_{REC}	$\overline{RESET}$ Recovery Time			1	µs

Input Test Waveforms and Measurement Levels



t_R, t_F < 20 ns (10% to 90%)

Output Test Load

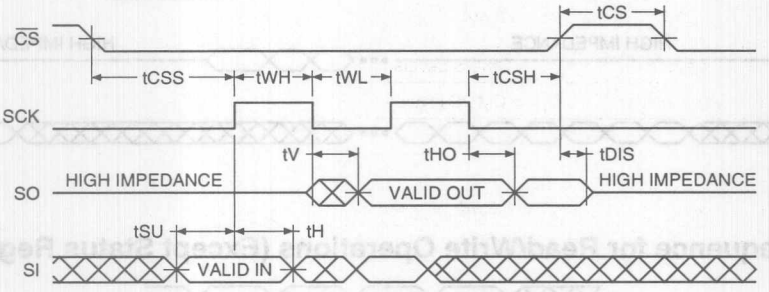


AC Waveforms

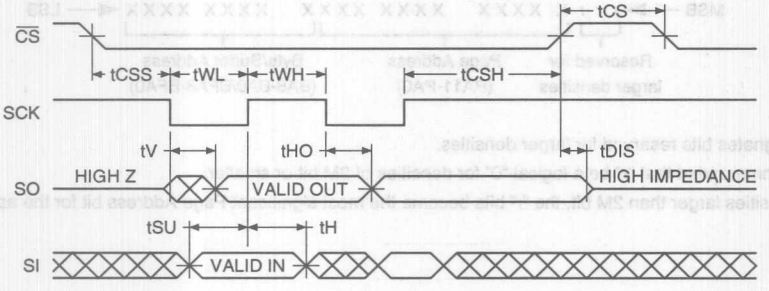
Two different timing diagrams are shown below. Waveform 1 shows the SCK signal being low when $\overline{CS}$ makes a high-to-low transition, and Waveform 2 shows the SCK signal being high when $\overline{CS}$ makes a high-to-low transition. Both waveforms show valid timing diagrams. The setup and hold times for the SI signal are referenced to the low-to-high transition on the SCK signal.

Waveform 1 shows timing that is also compatible with SPI Mode 0, and Waveform 2 shows timing that is compatible with SPI Mode 3.

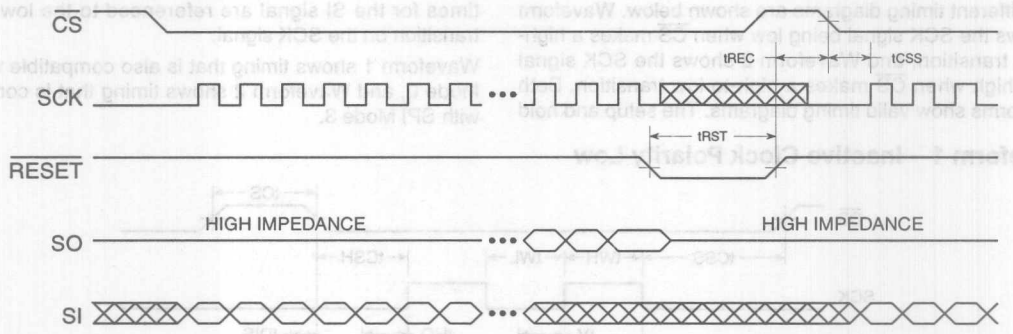
Waveform 1 – Inactive Clock Polarity Low



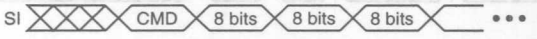
Waveform 2 – Inactive Clock Polarity High

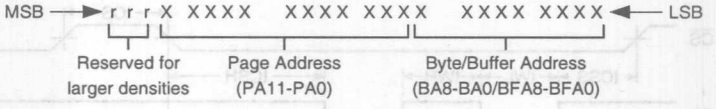


Reset Timing (Inactive Clock Polarity Low Shown)



Command Sequence for Read/Write Operations (Except Status Register Read)

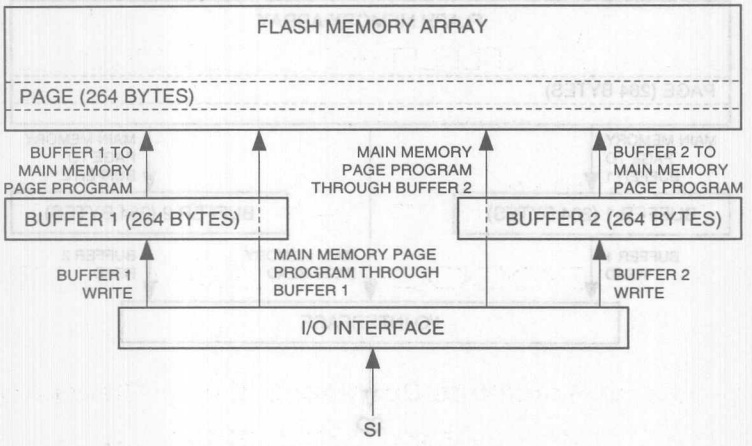




Notes:
1. "r" designates bits reserved for larger densities.
2. It is recommended that "r" be a logical "0" for densities of 2M bit or smaller.
3. For densities larger than 2M bit, the "r" bits become the most significant Page Address bit for the appropriate density.

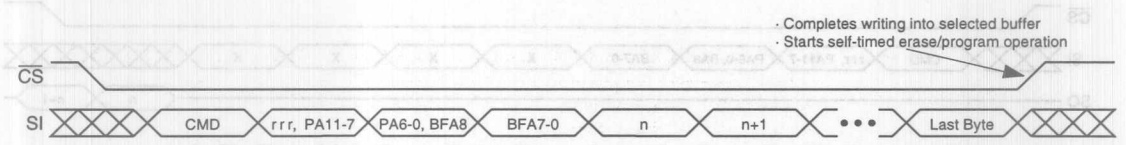
Write Operations

The following block diagram and waveforms illustrate the various write sequences available.

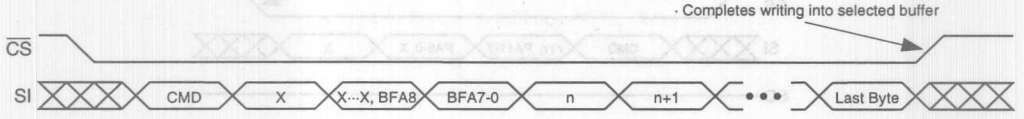


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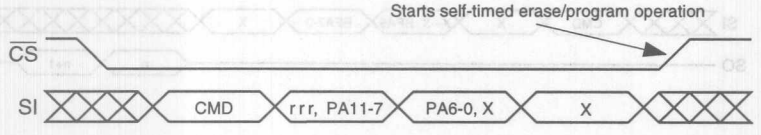
Main Memory Page Program through Buffers



Buffer Write



Buffer to Main Memory Page Program (Data from Buffer Programmed into Flash Page)

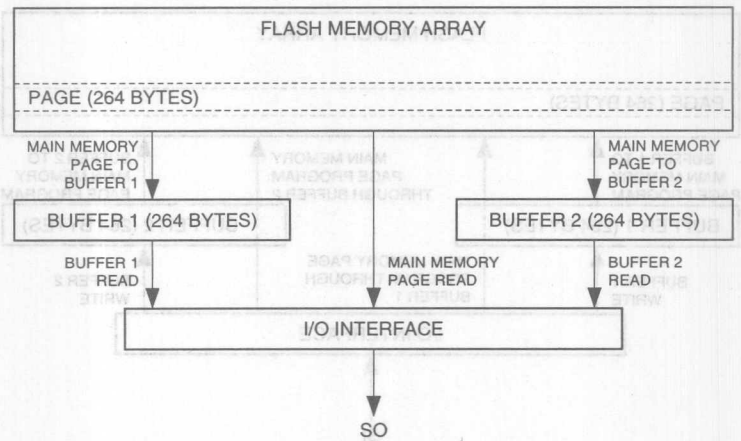


Each transition represents 8 bits and 8 clock cycles

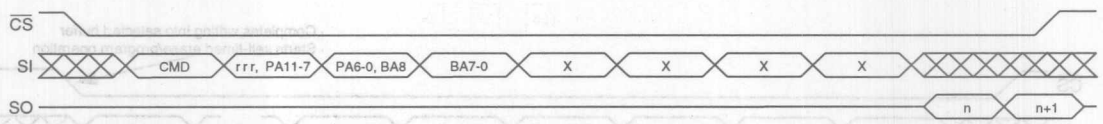
n = 1st byte written
n+1 = 2nd byte written

Read Operations

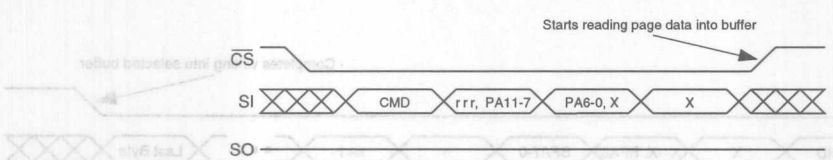
The following block diagram and waveforms illustrate the various read sequences available.



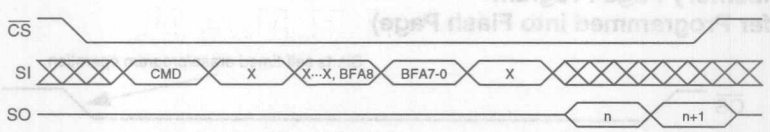
Main Memory Page Read



Main Memory Page to Buffer Transfer (Data from Flash Page Read into Buffer)



Buffer Read

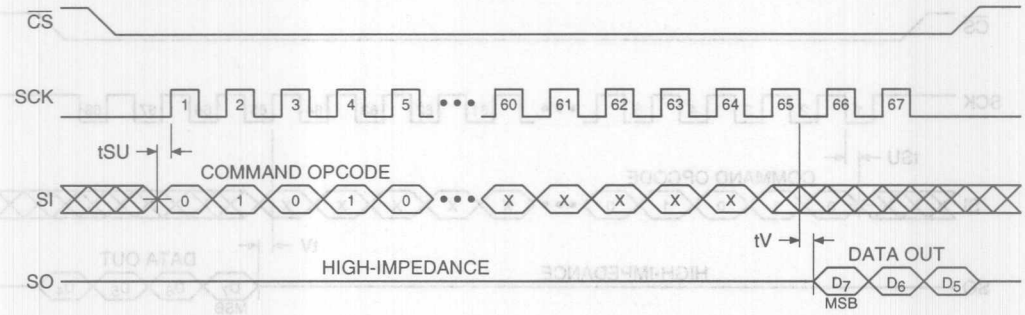


Each transition represents 8 bits and 8 clock cycles

n = 1st byte read
n+1 = 2nd byte read

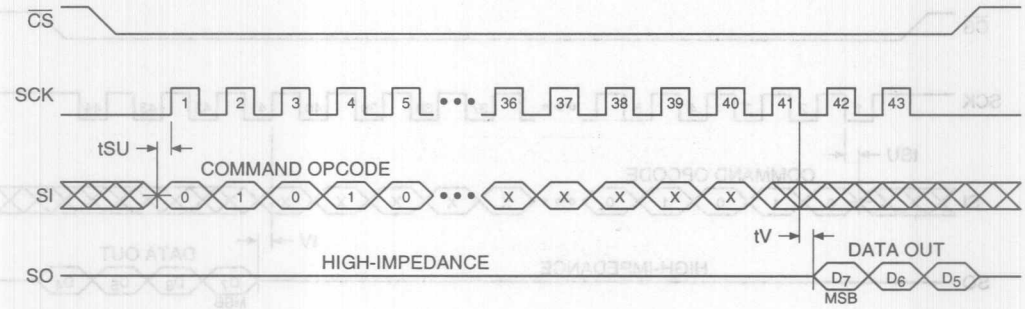
Detailed Bit-Level Read Timing – Inactive Clock Polarity Low

Main Memory Page Read

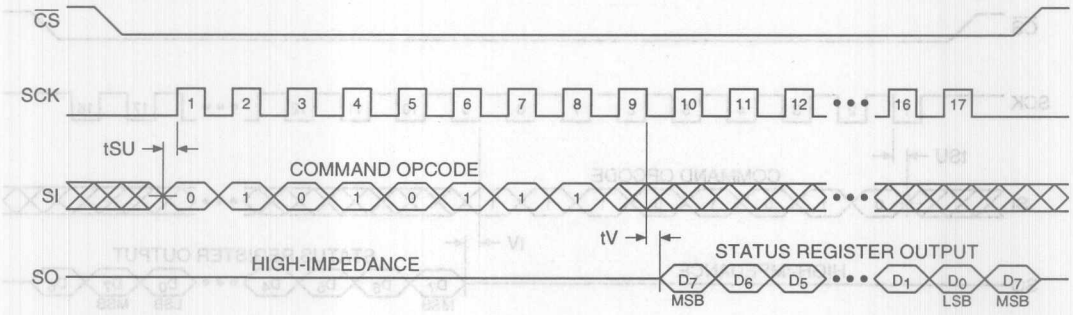


4

Buffer Read

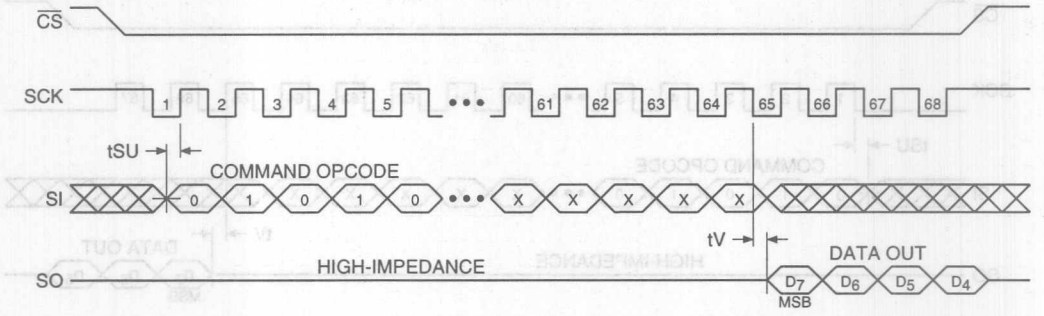


Status Register Read

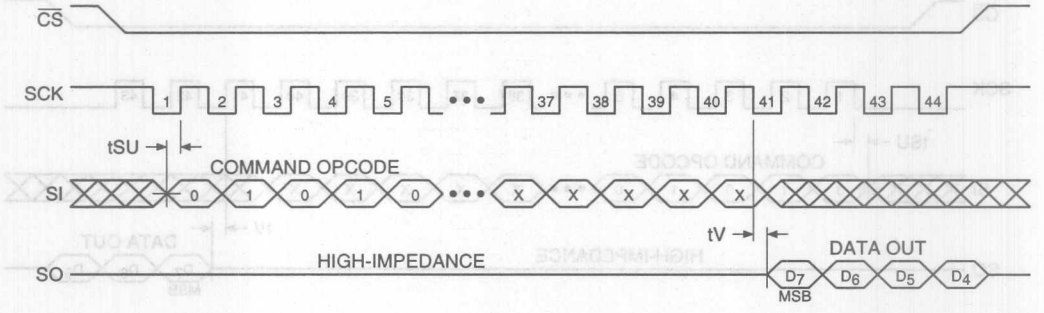

CS
SCK
1 2 3 4 5 6 7 8 9 10 11 12 ••• 16 17
tSU
COMMAND OPCODE
SI
0 1 0 1 0 1 1 1 ••• ••• •••

Detailed Bit-Level Read Timing – Inactive Clock Polarity High

Main Memory Page Read



Buffer Read



Status Register Read

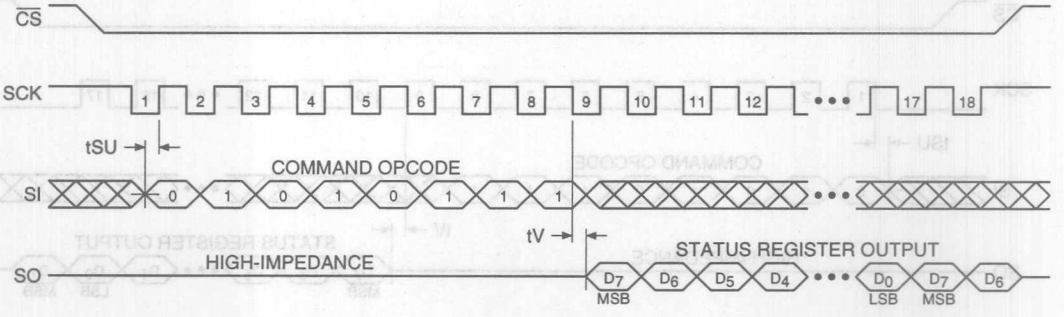


Table 1.

Main Memory Page Read	Buffer 1 Read	Buffer 2 Read	Main Memory Page to Buffer 1 Transfer	Main Memory Page to Buffer 2 Transfer	Main Memory Page to Buffer 1 Compare	Main Memory Page to Buffer 2 Compare	Buffer 1 Write	Buffer 2 Write
Opcode								
52H	54H	56H	53H	55H	60H	61H	84H	87H
0	0	0	0	0	0	0	1	1
1	1	1	1	1	1	1	0	0
0	0	0	0	0	1	1	0	0
1	1	1	1	1	0	0	0	0
0	0	0	0	0	0	0	0	0
0	1	1	0	1	0	0	1	1
1	0	1	1	0	0	0	0	1
0	0	0	1	1	0	1	0	1
r	X	X	r	r	r	r	X	X
r	X	X	r	r	r	r	X	X
r	X	X	r	r	r	r	X	X
r	X	X	r	r	r	r	X	X
r	X	X	r	r	r	r	X	X
PA9	X	X	PA9	PA9	PA9	PA9	X	X
PA8	X	X	PA8	PA8	PA8	PA8	X	X
PA7	X	X	PA7	PA7	PA7	PA7	X	X
PA6	X	X	PA6	PA6	PA6	PA6	X	X
PA5	X	X	PA5	PA5	PA5	PA5	X	X
PA4	X	X	PA4	PA4	PA4	PA4	X	X
PA3	X	X	PA3	PA3	PA3	PA3	X	X
PA2	X	X	PA2	PA2	PA2	PA2	X	X
PA1	X	X	PA1	PA1	PA1	PA1	X	X
PA0	X	X	PA0	PA0	PA0	PA0	X	X
BA8	BFA8	BFA8	X	X	X	X	BFA8	BFA8
BA7	BFA7	BFA7	X	X	X	X	BFA7	BFA7
BA6	BFA6	BFA6	X	X	X	X	BFA6	BFA6
BA5	BFA5	BFA5	X	X	X	X	BFA5	BFA5
BA4	BFA4	BFA4	X	X	X	X	BFA4	BFA4
BA3	BFA3	BFA3	X	X	X	X	BFA3	BFA3
BA2	BFA2	BFA2	X	X	X	X	BFA2	BFA2
BA1	BFA1	BFA1	X	X	X	X	BFA1	BFA1
BA0	BFA0	BFA0	X	X	X	X	BFA0	BFA0
X	X	X						
X	X	X						
X	X	X						
X	X	X						
X	X	X						
X	X	X						
X	X	X						
X	X	X						
•								
•								
•								
X (64th bit)								

X (Don't Care)
r (reserved bits)

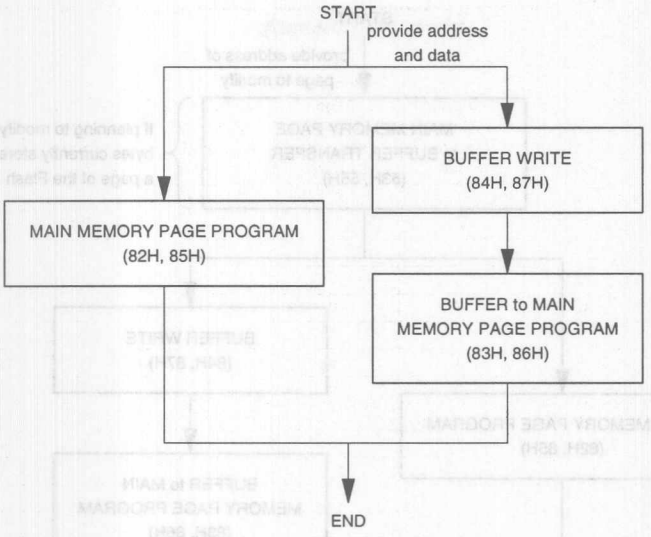
4

Table 2.

Buffer 1 to Main Memory Page Program with Built-In Erase	Buffer 2 to Main Memory Page Program with Built-In Erase	Buffer 1 to Main Memory Page Program without Built-In Erase	Buffer 2 to Main Memory Page Program without Built-In Erase	Main Memory Page Program Through Buffer 1	Main Memory Page Program Through Buffer 2	Auto Page Rewrite Through Buffer 1	Auto Page Rewrite Through Buffer 2	Status Register
Opcode								
83H	86H	88H	89H	82H	85H	58H	59H	57H
1	1	1	1	1	1	0	0	0
0	0	0	0	0	0	1	1	1
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1	1
0	0	1	1	0	0	1	1	0
0	1	0	0	0	1	0	0	1
1	1	0	0	1	0	0	0	1
1	0	0	1	0	1	0	1	1
r	r	r	r	r	r	r	r	
r	r	r	r	r	r	r	r	
r	r	r	r	r	r	r	r	
r	r	r	r	r	r	r	r	
r	r	r	r	r	r	r	r	
PA9	PA9	PA9	PA9	PA9	PA9	PA9	PA9	
PA8	PA8	PA8	PA8	PA8	PA8	PA8	PA8	
PA7	PA7	PA7	PA7	PA7	PA7	PA7	PA7	
PA6	PA6	PA6	PA6	PA6	PA6	PA6	PA6	
PA5	PA5	PA5	PA5	PA5	PA5	PA5	PA5	
PA4	PA4	PA4	PA4	PA4	PA4	PA4	PA4	
PA3	PA3	PA3	PA3	PA3	PA3	PA3	PA3	
PA2	PA2	PA2	PA2	PA2	PA2	PA2	PA2	
PA1	PA1	PA1	PA1	PA1	PA1	PA1	PA1	
PA0	PA0	PA0	PA0	PA0	PA0	PA0	PA0	
X	X	X	X	BA8	BA8	X	X	
X	X	X	X	BA7	BA7	X	X	
X	X	X	X	BA6	BA6	X	X	
X	X	X	X	BA5	BA5	X	X	
X	X	X	X	BA4	BA4	X	X	
X	X	X	X	BA3	BA3	X	X	
X	X	X	X	BA2	BA2	X	X	
X	X	X	X	BA1	BA1	X	X	
X	X	X	X	BA0	BA0	X	X	

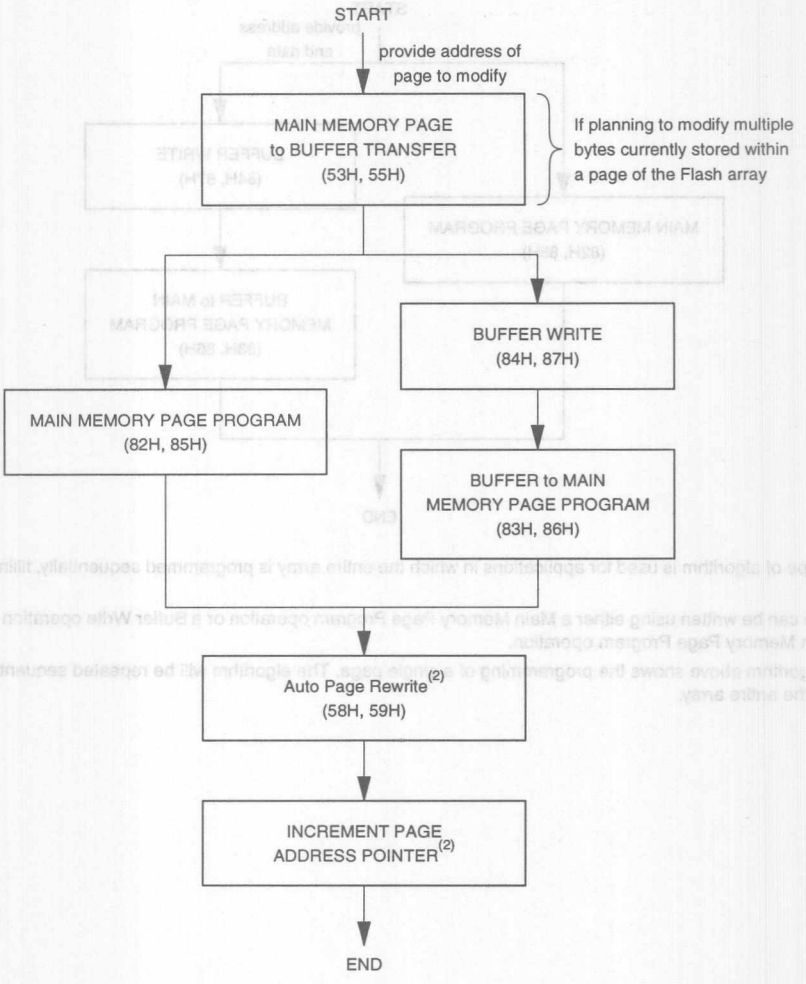
(Don't Care)
r (reserved bits)

Figure 1. Algorithm for Programming or Reprogramming of the Entire Array Sequentially



Notes:
1. This type of algorithm is used for applications in which the entire array is programmed sequentially, filling the array page-by-page.
2. A page can be written using either a Main Memory Page Program operation or a Buffer Write operation followed by a Buffer to Main Memory Page Program operation.
3. The algorithm above shows the programming of a single page. The algorithm will be repeated sequentially for each page within the entire array.

Figure 2. Algorithm for Randomly Modifying Data



Notes:
1. To preserve data integrity, each page of the DataFlash memory array must be updated/rewritten at least once within every 10,000 cumulative page erase/program operations.
2. A Page Address Pointer must be maintained to indicate which page is to be rewritten. The Auto Page Rewrite command must use the address specified by the Page Address Pointer.
3. Other algorithms can be used to rewrite portions of the Flash array. Low power applications may choose to wait until 10,000 cumulative page erase/program operations have accumulated before rewriting all pages of the Flash array. See application note AN-4 ("Using Atmel's Serial DataFlash") for more details.

Ordering Information

f_{SCK} (MHz)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
5	10	0.015	AT45DB021-JC AT45DB021-RC AT45DB021-TC	32J 28R 28T	Commercial (0°C to 70°C)
5	10	0.015	AT45DB021-JI AT45DB021-RI AT45DB021-TI	32J 28R 28T	Industrial (-40°C to 85°C)

4

Package Type	
32J	32-Lead, Plastic J-Leaded Chip Carrier Package (PLCC)
28R	28-Lead, 0.330" Wide, Plastic Gull-Wing Small Outline Package (SOIC)
28T	28-Lead, Plastic Thin Small Outline Package (TSOP)

Features

- Single 2.7V - 3.6V Supply
- Serial Interface Architecture
- Page Program Operation
  - Single Cycle Reprogram (Erase and Program)
  - 2048 Pages (264 Bytes/Page) Main Memory
- Two 264-Byte SRAM Data Buffers – Allows Receiving of Data While Reprogramming of Nonvolatile Memory
- Internal Program and Control Timer
- Fast Page Program Time – 7 ms Typical
- 120 µs Typical Page to Buffer Transfer Time
- Low Power Dissipation
  - 4 mA Active Read Current Typical
  - 8 µA CMOS Standby Current Typical
- 5 MHz Max Clock Frequency
- Hardware Data Protection Feature
- Serial Peripheral Interface (SPI) Compatible – Modes 0 and 3
- CMOS and TTL Compatible Inputs and Outputs
- Commercial and Industrial Temperature Ranges

4-Megabit 2.7-volt Only Serial DataFlash®

4

AT45DB041

Description

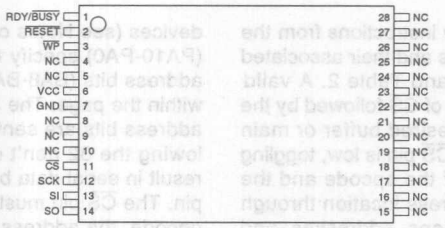
The AT45DB041 is a 2.7-volt only, serial interface Flash memory suitable for in-system reprogramming. Its 4,325,376 bits of memory are organized as 2048 pages of 264-bytes each. In addition to the main memory, the AT45DB041 also contains two SRAM data buffers of 264-bytes each. The buffers allow receiving of data while a page in the main memory is being reprogrammed. Unlike conventional Flash memories that are accessed randomly with multiple address lines and a parallel interface,

(continued)

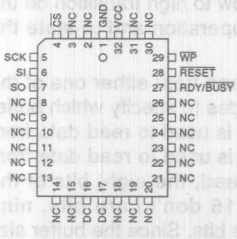
Pin Configurations

Pin Name	Function
$\overline{CS}$	Chip Select
SCK	Serial Clock
SI	Serial Input
SO	Serial Output
$\overline{WP}$	Hardware Page Write Protect Pin
$\overline{RESET}$	Chip Reset
RDY/$\overline{BUSY}$	Ready/Busy

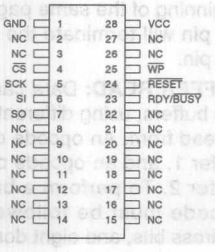
TSOP Top View
Type 1



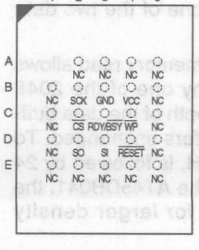
PLCC



SOIC



CBGA Top View
Through Package



Note: PLCC package pins 16 and 17 are DON'T CONNECT.

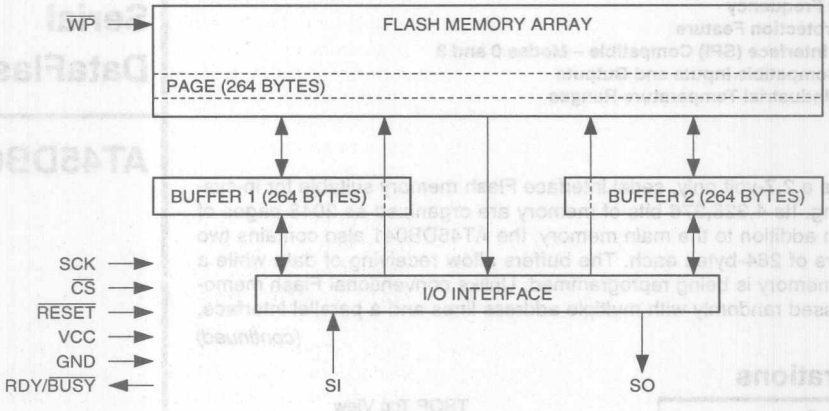
Rev. 0669D–07/98

the DataFlash uses a serial interface to sequentially access its data. The simple serial interface facilitates hardware layout, increases system reliability, minimizes switching noise, and reduces package size and active pin count. The device is optimized for use in many commercial and industrial applications where high density, low pin count, low voltage, and low power are essential. Typical applications for the DataFlash are digital voice storage, image storage, and data storage. The device operates at clock frequencies up to 5 MHz with a typical active read current consumption of 4 mA.

To allow for simple in-system reprogrammability, the AT45DB041 does not require high input voltages for programming. The device operates from a single power supply, 2.7V to 3.6V, for both the program and read operations. The AT45DB041 is enabled through the chip select pin ($\overline{CS}$) and accessed via a three-wire interface consisting of the Serial Input (SI), Serial Output (SO), and the Serial Clock (SCK).

All programming cycles are self-timed, and no separate erase cycle is required before programming.

Block Diagram



Device Operation

The device operation is controlled by instructions from the host processor. The list of instructions and their associated opcodes are contained in Table 1 and Table 2. A valid instruction starts with the falling edge of $\overline{CS}$ followed by the appropriate 8-bit opcode and the desired buffer or main memory address location. While the $\overline{CS}$ pin is low, toggling the SCK pin controls the loading of the opcode and the desired buffer or main memory address location through the SI (serial input) pin. All instructions, addresses, and data are transferred with the most significant bit (MSB) first.

Read

By specifying the appropriate opcode, data can be read from the main memory or from either one of the two data buffers.

MAIN MEMORY PAGE READ: A main memory read allows the user to read data directly from any one of the 2048 pages in the main memory, bypassing both of the data buffers and leaving the contents of the buffers unchanged. To start a page read, the 8-bit opcode, 52H, is followed by 24 address bits and 32 don't care bits. In the AT45DB041, the first four address bits are reserved for larger density devices (see Notes on page 46), the next 11 address bits (PA10-PA0) specify the page address, and the next nine address bits (BA8-BA0) specify the starting byte address within the page. The 32 don't care bits which follow the 24 address bits are sent to initialize the read operation. Following the 32 don't care bits, additional pulses on SCK result in serial data being output on the SO (serial output) pin. The $\overline{CS}$ pin must remain low during the loading of the opcode, the address bits, and the reading of data. When the end of a page in main memory is reached during a main memory page read, the device will continue reading at the beginning of the same page. A low to high transition on the $\overline{CS}$ pin will terminate the read operation and tri-state the SO pin.

BUFFER READ: Data can be read from either one of the two buffers, using different opcodes to specify which buffer to read from. An opcode of 54H is used to read data from buffer 1, and an opcode of 56H is used to read data from buffer 2. To perform a buffer read, the eight bits of the opcode must be followed by 15 don't care bits, nine address bits, and eight don't care bits. Since the buffer size

is 264-bytes, nine address bits (BFA8-BFA0) are required to specify the first byte of data to be read from the buffer. The $\overline{CS}$ pin must remain low during the loading of the opcode, the address bits, the don't care bits, and the reading of data. When the end of a buffer is reached, the device will continue reading back at the beginning of the buffer. A low to high transition on the $\overline{CS}$ pin will terminate the read operation and tri-state the SO pin.

MAIN MEMORY PAGE TO BUFFER TRANSFER: A page of data can be transferred from the main memory to either buffer 1 or buffer 2. An 8-bit opcode, 53H for buffer 1 and 55H for buffer 2, is followed by the four reserved bits, 11 address bits (PA10-PA0) which specify the page in main memory that is to be transferred, and nine don't care bits. The $\overline{CS}$ pin must be low while toggling the SCK pin to load the opcode, the address bits, and the don't care bits from the SI pin. The transfer of the page of data from the main memory to the buffer will begin when the $\overline{CS}$ pin transitions from a low to a high state. During the transfer of a page of data (t_{XFR}), the status register can be read to determine whether the transfer has been completed or not.

MAIN MEMORY PAGE TO BUFFER COMPARE: A page of data in main memory can be compared to the data in buffer 1 or buffer 2. An 8-bit opcode, 60H for buffer 1 and 61H for buffer 2, is followed by 24 address bits consisting of the four reserved bits, 11 address bits (PA10-PA0) which specify the page in the main memory that is to be compared to the buffer, and nine don't care bits. The loading of the opcode and the address bits is the same as described previously. The $\overline{CS}$ pin must be low while toggling the SCK pin to load the opcode, the address bits, and the don't care bits from the SI pin. On the low to high transition of the $\overline{CS}$ pin, the 264 bytes in the selected main memory page will be compared with the 264 bytes in buffer 1 or buffer 2. During this time (t_{XFR}), the status register will indicate that the part is busy. On completion of the compare operation, bit 6 of the status register is updated with the result of the compare.

Program

BUFFER WRITE: Data can be shifted in from the SI pin into either buffer 1 or buffer 2. To load data into either buffer, an 8-bit opcode, 84H for buffer 1 or 87H for buffer 2, is followed by 15 don't care bits and nine address bits (BFA8-BFA0). The nine address bits specify the first byte in the buffer to be written. The data is entered following the address bits. If the end of the data buffer is reached, the device will wrap around back to the beginning of the buffer. Data will continue to be loaded into the buffer until a low to high transition is detected on the $\overline{CS}$ pin.

BUFFER TO MAIN MEMORY PAGE PROGRAM WITH BUILT-IN ERASE: Data written into either buffer 1 or buffer 2 can be programmed into the main memory. An 8-bit opcode, 83H for buffer 1 or 86H for buffer 2, is followed by the four reserved bits, 11 address bits (PA10-PA0) that specify the page in the main memory to be written, and nine additional don't care bits. When a low to high transition occurs on the $\overline{CS}$ pin, the part will first erase the selected page in main memory to all 1s and then program the data stored in the buffer into the specified page in the main memory. Both the erase and the programming of the page are internally self timed and should take place in a maximum time of t_{EP}. During this time, the status register will indicate that the part is busy.

BUFFER TO MAIN MEMORY PAGE PROGRAM WITHOUT BUILT-IN ERASE: A previously erased page within main memory can be programmed with the contents of either buffer 1 or buffer 2. An 8-bit opcode, 88H for buffer 1 or 89H for buffer 2, is followed by the four reserved bits, 11 address bits (PA10-PA0) that specify the page in the main memory to be written, and nine additional don't care bits. When a low to high transition occurs on the $\overline{CS}$ pin, the part will program the data stored in the buffer into the specified page in the main memory. It is necessary that the page in main memory that is being programmed has been previously programmed to all 1s (erased state). The programming of the page is internally self timed and should take place in a maximum time of t_P. During this time, the status register will indicate that the part is busy.

MAIN MEMORY PAGE PROGRAM: This operation is a combination of the Buffer Write and Buffer to Main Memory Page Program with Built-In Erase operations. Data is first shifted into buffer 1 or buffer 2 from the SI pin and then programmed into a specified page in the main memory. An 8-bit opcode, 82H for buffer 1 or 85H for buffer 2, is followed by the four reserved bits and 20 address bits. The 11 most significant address bits (PA10-PA0) select the page in the main memory where data is to be written, and the next nine address bits (BFA8-BFA0) select the first byte in the buffer to be written. After all address bits are shifted in, the part will take data from the SI pin and store it in one of the data buffers. If the end of the buffer is reached, the device will wrap around back to the beginning of the buffer. When there is a low to high transition on the $\overline{CS}$ pin, the part will first erase the selected page in main memory to all 1s and then program the data stored in the buffer into the specified page in the main memory. Both the erase and the programming of the page are internally self timed and should take place in a maximum of time t_{EP}. During this time, the status register will indicate that the part is busy.

AUTO PAGE REWRITE: This mode is only needed if multiple bytes within a page or multiple pages of data are modified in a random fashion. This mode is a combination of two operations: Main Memory Page to Buffer Transfer and Buffer to Main Memory Page Program with Built-In Erase. A page of data is first transferred from the main memory to buffer 1 or buffer 2, and then the same data (from buffer 1 or buffer 2) is programmed back into its original page of

main memory. An 8-bit opcode, 58H for buffer 1 or 59H for buffer 2, is followed by the four reserved bits, 11 address bits (PA10-PA0) that specify the page in main memory to be rewritten, and nine additional don't care bits. When a low to high transition occurs on the $\overline{CS}$ pin, the part will first transfer data from the page in main memory to a buffer and then program the data from the buffer back into same page of main memory. The operation is internally self-timed and should take place in a maximum time of t_{EP}. During this time, the status register will indicate that the part is busy.

If the main memory is programmed or reprogrammed sequentially page by page, then the programming algorithm shown in Figure 1 is recommended. Otherwise, if multiple bytes in a page or several pages are programmed randomly in the main memory, then the programming algorithm shown in Figure 2 is recommended.

STATUS REGISTER: The status register can be used to determine the device's ready/busy status, the result of a Main Memory Page to Buffer Compare operation, or the device density. To read the status register, an opcode of 57H must be loaded into the device. After the last bit of the opcode is shifted in, the eight bits of the status register, starting with the MSB (bit 7), will be shifted out on the SO pin during the next eight clock cycles. The five most-significant bits of the status register will contain device information, while the remaining three least-significant bits are reserved for future use and will have undefined values. After bit 0 of the status register has been shifted out, the sequence will repeat itself (as long as $\overline{CS}$ remains low and SCK is being toggled) starting again with bit 7. The data in the status register is constantly updated, so each repeating sequence will output new data.

Ready/busy status is indicated using bit 7 of the status register. If bit 7 is a 1, then the device is not busy and is ready to accept the next command. If bit 7 is a 0, then the device is in a busy state. The user can continuously poll bit 7 of the status register by stopping SCK once bit 7 has been output. The status of bit 7 will continue to be output on the SO pin, and once the device is no longer busy, the state of SO will change from 0 to 1. There are six operations which can cause the device to be in a busy state: Main Memory Page to Buffer Transfer, Main Memory Page to Buffer Compare, Buffer to Main Memory Page Program with Built-In Erase, Buffer to Main Memory Page Program without Built-In Erase, Main Memory Page Program, and Auto Page Rewrite.

The result of the most recent Main Memory Page to Buffer Compare operation is indicated using bit 6 of the status register. If bit 6 is a 0, then the data in the main memory page matches the data in the buffer. If bit 6 is a 1, then at least one bit of the data in the main memory page does not match the data in the buffer.

The device density is indicated using bits 5, 4, and 3 of the status register. For the AT45DB041, the three bits are 0, 1, and 1. The decimal value of these three binary bits does not equate to the device density; the three bits represent a combinational code relating to differing densities of Serial DataFlash devices, allowing a total of eight different density configurations.

Read/Program Mode Summary

The modes listed above can be separated into two groups — modes which make use of the flash memory array (Group A) and modes which do not make use of the flash memory array (Group B).

Group A modes consist of:

1. Main memory page read
2. Main memory page to buffer 1 (or 2) transfer
3. Main memory page to buffer 1 (or 2) compare
4. Buffer 1 (or 2) to main memory page program with built-in erase
5. Buffer 1 (or 2) to main memory page program without built-in erase
6. Main memory page program
7. Auto page rewrite

Group B modes consist of:

1. Buffer 1 (or 2) read
2. Buffer 1 (or 2) write
3. Status read

If a Group A mode is in progress (not fully completed) then another mode in Group A should not be started. However, during this time in which a Group A mode is in progress, modes in Group B can be started.

This gives the Serial DataFlash the ability to virtually accommodate a continuous data stream. While data is being programmed into main memory from buffer 1, data can be loaded into buffer 2 (or vice versa). See application note AN-4 ("Using Atmel's Serial DataFlash") for more details.

HARDWARE PAGE WRITE PROTECT: If the $\overline{WP}$ pin is held low, the first 256 pages of the main memory cannot be reprogrammed. The only way to reprogram the first 256 pages is to first drive the protect pin high and then use the program commands previously mentioned.

Status Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RDY/$\overline{BUSY}$	COMP	0	1	1	X	X	X

RESET: A low state on the reset pin ($\overline{\text{RESET}}$) will terminate the operation in progress and reset the internal state machine to an idle state. The device will remain in the reset condition as long as a low level is present on the $\overline{\text{RESET}}$ pin. Normal operation can resume once the $\overline{\text{RESET}}$ pin is brought back to a high level.

The device also incorporates an internal power-on reset circuit; therefore, there are no restrictions on the $\overline{\text{RESET}}$ pin during power-on sequences.

READY/$\overline{\text{BUSY}}$: This open drain output pin will be driven low when the device is busy in an internally self-timed operation. This pin, which is normally in a high state (through an external pull-up resistor), will be pulled low during programming operations, compare operations, and during page-to-buffer transfers.

The busy status indicates that the Flash memory array and one of the buffers cannot be accessed; read and write operations to the other buffer can still be performed.

Power On/Reset State

When power is first applied to the device, or when recovering from a reset condition, the device will default to SPI mode 3. In addition, the SO pin will be in a high impedance state, and a high to low transition on the $\overline{\text{CS}}$ pin will be required to start a valid instruction. The SPI mode will be automatically selected on every falling edge of $\overline{\text{CS}}$ by sampling the inactive clock state.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC and AC Operating Range

		AT45DB041
Operating Temperature (Case)	Com.	0°C to 70°C
	Ind.	-40°C to 85°C
V_{CC} Power Supply[1]		2.7V to 3.6V

Note: 1. After power is applied and V_{CC} is at the minimum specified data sheet value, the system should wait 20 ms before an operational mode is started.

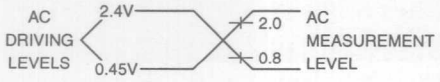
DC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{SB}	Standby Current	$\overline{CS}$, $\overline{RESET}$, $\overline{WP}$ = V_{IH}, all inputs at CMOS levels		8	20	µA
I_{CC1}	Active Current, Read Operation	f = 5 MHz; I_{OUT} = 0 mA; V_{CC} = 3.6V		4	10	mA
I_{CC2}	Active Current, Program/Erase Operation	V_{CC} = 3.6V		15	35	mA
I_{LI}	Input Load Current	V_{IN} = CMOS levels			1	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = CMOS levels			1	µA
V_{IL}	Input Low Voltage				0.6	V
V_{IH}	Input High Voltage		2.0			V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA; V_{CC} = 2.7V			0.4	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA	V_{CC} - 0.2V			V

AC Characteristics

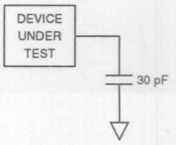
Symbol	Parameter	Min	Typ	Max	Units
f_{SCK}	SCK Frequency			5	MHz
t_{WH}	SCK High Time	80			ns
t_{WL}	SCK Low Time	80			ns
t_{CS}	Minimum $\overline{CS}$ High Time	350			ns
t_{CSS}	$\overline{CS}$ Setup Time	350			ns
t_{CSH}	$\overline{CS}$ Hold Time	350			ns
t_{CSB}	$\overline{CS}$ High to RDY/$\overline{BUSY}$ Low			200	ns
t_{SU}	Data In Setup Time	15			ns
t_H	Data In Hold Time	35			ns
t_{HO}	Output Hold Time	0			ns
t_{DIS}	Output Disable Time			100	ns
t_V	Output Valid			120	ns
t_{XFR}	Page to Buffer Transfer/Compare Time		120	250	µs
t_{EP}	Page Erase and Programming Time		10	20	ms
t_P	Page Programming Time		7	14	ms
t_{RST}	$\overline{RESET}$ Pulse Width	10			µs
t_{REC}	$\overline{RESET}$ Recovery Time			1	µs

Input Test Waveforms and Measurement Levels



t_R, t_F < 20 ns (10% to 90%)

Output Test Load

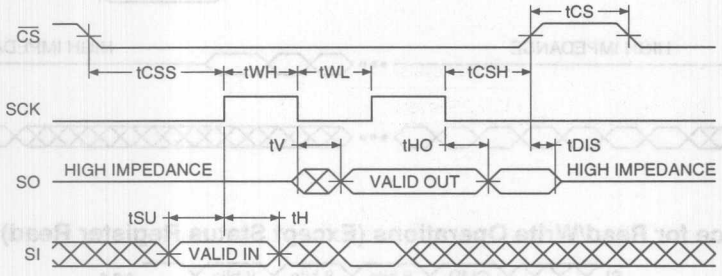


AC Waveforms

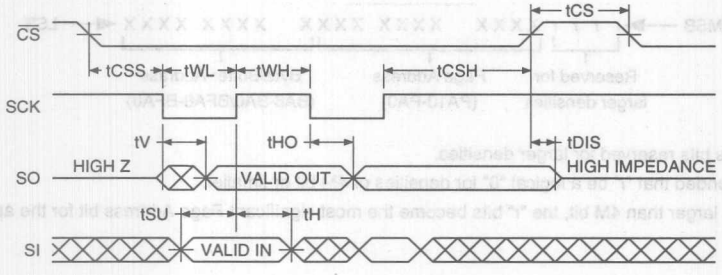
Two different timing diagrams are shown below. Waveform 1 shows the SCK signal being low when $\overline{CS}$ makes a high-to-low transition, and Waveform 2 shows the SCK signal being high when $\overline{CS}$ makes a high-to-low transition. Both waveforms show valid timing diagrams. The setup and hold times for the SI signal are referenced to the low-to-high transition on the SCK signal.

Waveform 1 shows timing that is also compatible with SPI Mode 0, and Waveform 2 shows timing that is compatible with SPI Mode 3.

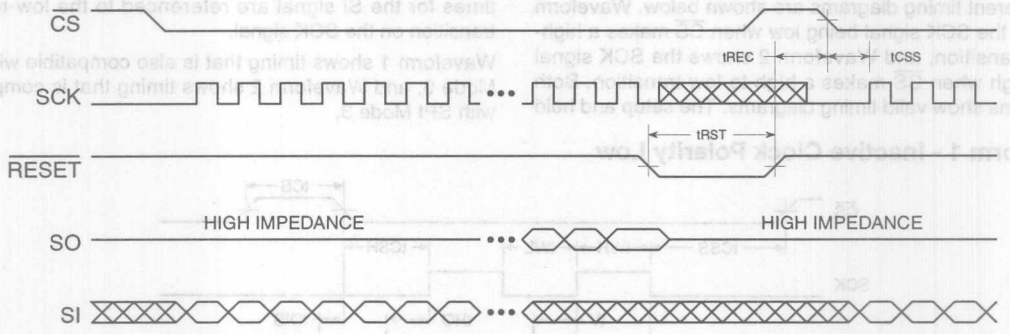
Waveform 1 - Inactive Clock Polarity Low



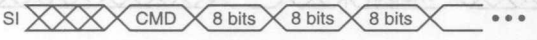
Waveform 2 - Inactive Clock Polarity High

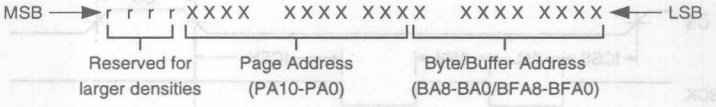


Reset Timing (Inactive Clock Polarity Low Shown)



Command Sequence for Read/Write Operations (Except Status Register Read)

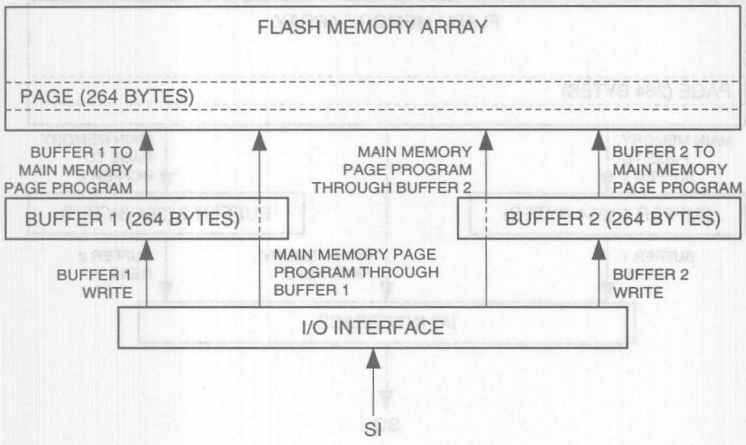




Notes:
1. "r" designates bits reserved for larger densities.
2. It is recommended that "r" be a logical "0" for densities of 4M bit or smaller.
3. For densities larger than 4M bit, the "r" bits become the most significant Page Address bit for the appropriate density.

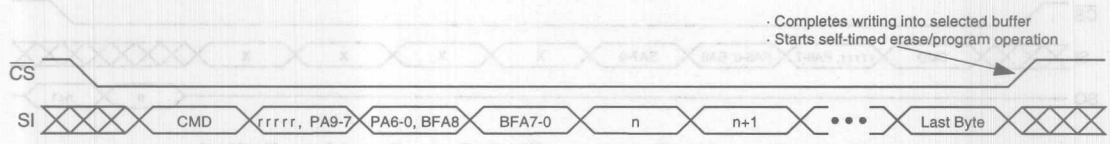
Write Operations

The following block diagram and waveforms illustrate the various write sequences available.

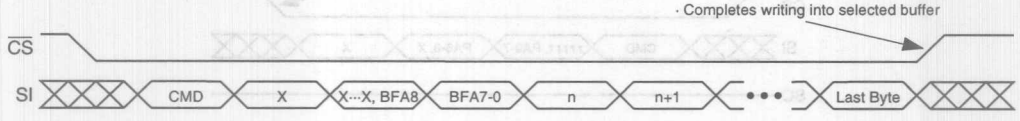


4

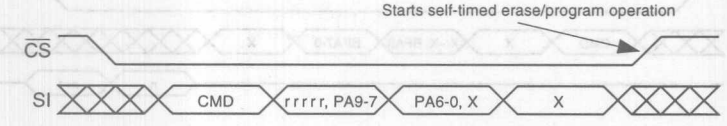
Main Memory Page Program through Buffers



Buffer Write



Buffer to Main Memory Page Program (Data from Buffer Programmed into Flash Page)

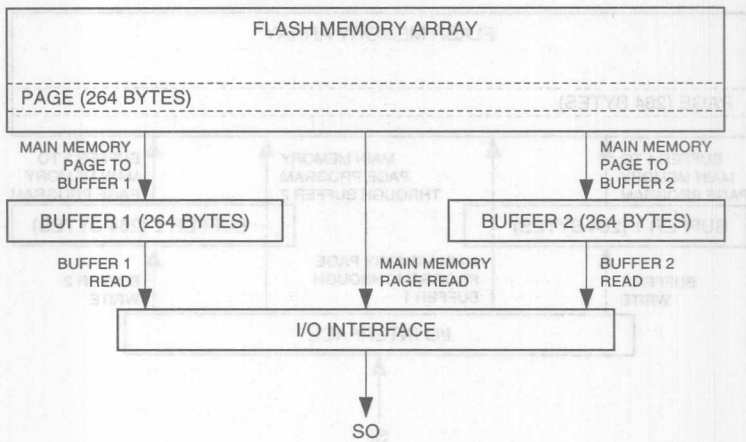


Each transition represents 8 bits and 8 clock cycles

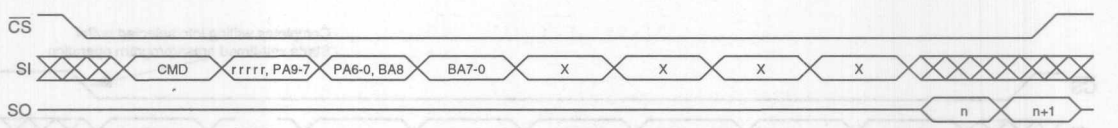
n = 1st byte read
n+1 = 2nd byte read

Read Operations

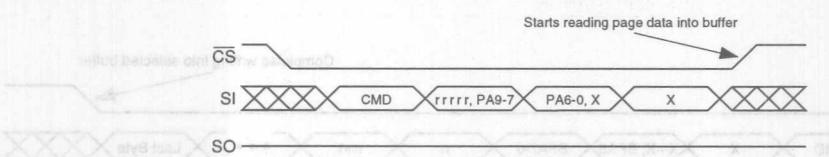
The following block diagram and waveforms illustrate the various read sequences available.



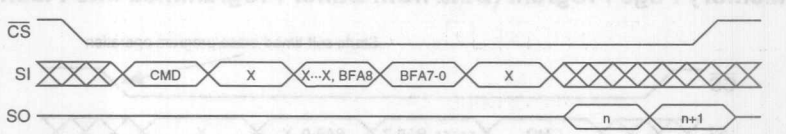
Main Memory Page Read



Main Memory Page to Buffer Transfer (Data from Flash Page Read into Buffer)



Buffer Read

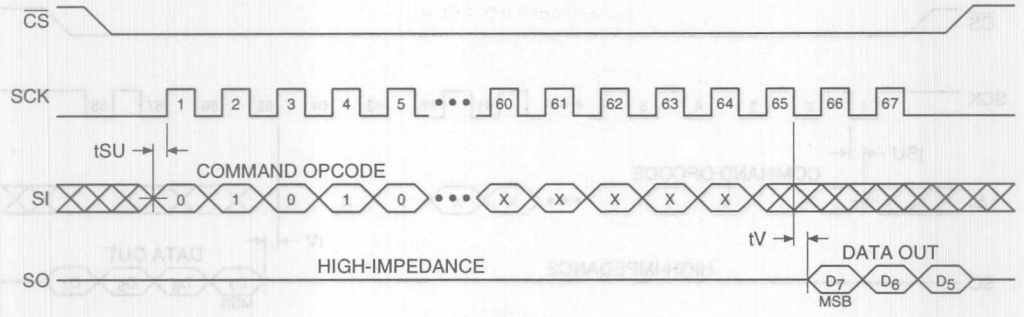


Each transition represents 8 bits and 8 clock cycles

n = 1st byte written
n+1 = 2nd byte written

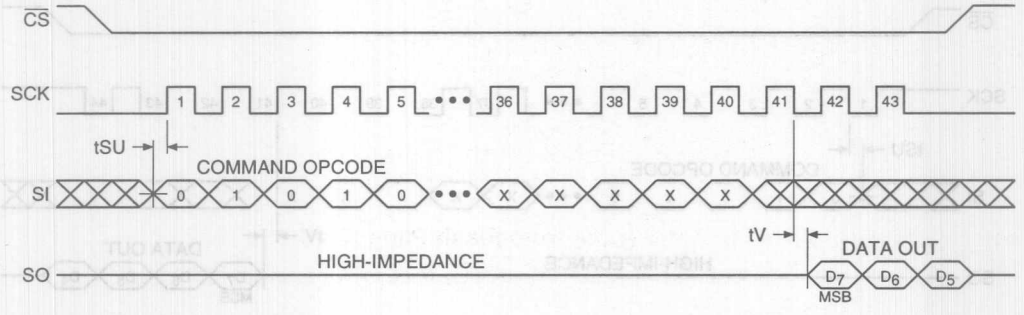
Detailed Bit-Level Read Timing – Inactive Clock Polarity Low

Main Memory Page Read

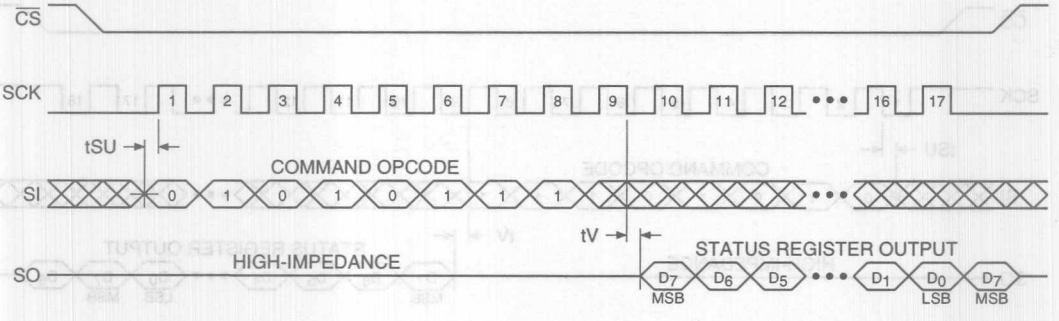


4

Buffer Read

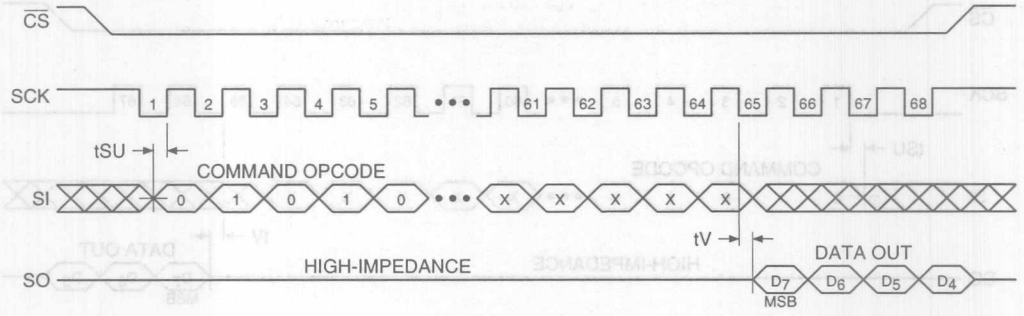


Status Register Read

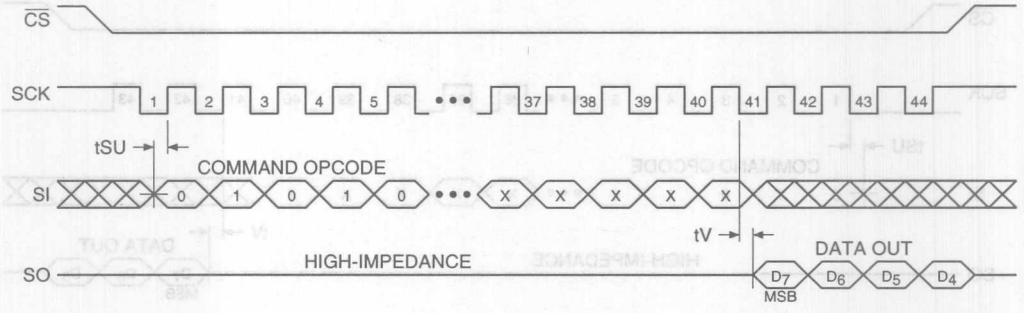


Detailed Bit-Level Read Timing – Inactive Clock Polarity High

Main Memory Page Read



Buffer Read



Status Register Read

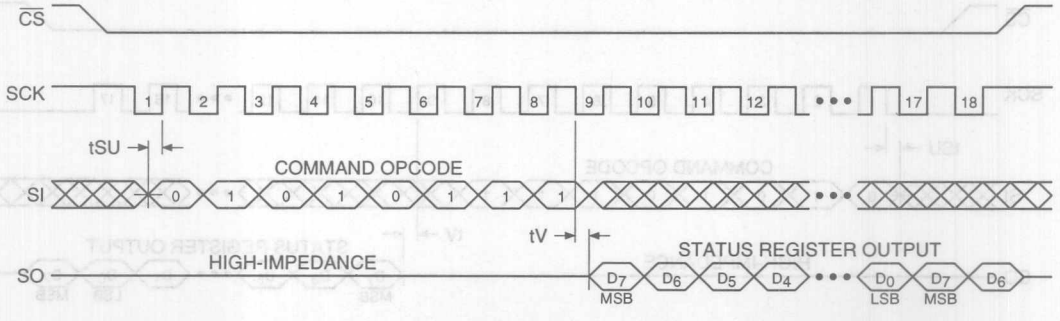


Table 1.

Main Memory Page Read	Buffer 1 Read	Buffer 2 Read	Main Memory Page to Buffer 1 Transfer	Main Memory Page to Buffer 2 Transfer	Main Memory Page to Buffer 1 Compare	Main Memory Page to Buffer 2 Compare	Buffer 1 Write	Buffer 2 Write
Opcode								
52H	54H	56H	53H	55H	60H	61H	84H	87H
0	0	0	0	0	0	0	1	1
1	1	1	1	1	1	1	0	0
0	0	0	0	0	1	1	0	0
1	1	1	1	1	0	0	0	0
0	0	0	0	0	0	0	0	0
0	1	1	0	1	0	0	1	1
1	0	1	1	0	0	0	0	1
0	0	0	1	1	0	1	0	1
r	X	X	r	r	r	r	X	X
r	X	X	r	r	r	r	X	X
r	X	X	r	r	r	r	X	X
r	X	X	r	r	r	r	X	X
PA10	X	X	PA10	PA10	PA10	PA10	X	X
PA9	X	X	PA9	PA9	PA9	PA9	X	X
PA8	X	X	PA8	PA8	PA8	PA8	X	X
PA7	X	X	PA7	PA7	PA7	PA7	X	X
PA6	X	X	PA6	PA6	PA6	PA6	X	X
PA5	X	X	PA5	PA5	PA5	PA5	X	X
PA4	X	X	PA4	PA4	PA4	PA4	X	X
PA3	X	X	PA3	PA3	PA3	PA3	X	X
PA2	X	X	PA2	PA2	PA2	PA2	X	X
PA1	X	X	PA1	PA1	PA1	PA1	X	X
PA0	X	X	PA0	PA0	PA0	PA0	X	X
BA8	BFA8	BFA8	X	X	X	X	BFA8	BFA8
BA7	BFA7	BFA7	X	X	X	X	BFA7	BFA7
BA6	BFA6	BFA6	X	X	X	X	BFA6	BFA6
BA5	BFA5	BFA5	X	X	X	X	BFA5	BFA5
BA4	BFA4	BFA4	X	X	X	X	BFA4	BFA4
BA3	BFA3	BFA3	X	X	X	X	BFA3	BFA3
BA2	BFA2	BFA2	X	X	X	X	BFA2	BFA2
BA1	BFA1	BFA1	X	X	X	X	BFA1	BFA1
BA0	BFA0	BFA0	X	X	X	X	BFA0	BFA0
X	X	X						
X	X	X						
X	X	X						
X	X	X						
X	X	X						
X	X	X						
X	X	X						
X	X	X						
•								
•								
•								
X (64th bit)								

X (Don't Care)
r (reserved bits)

4

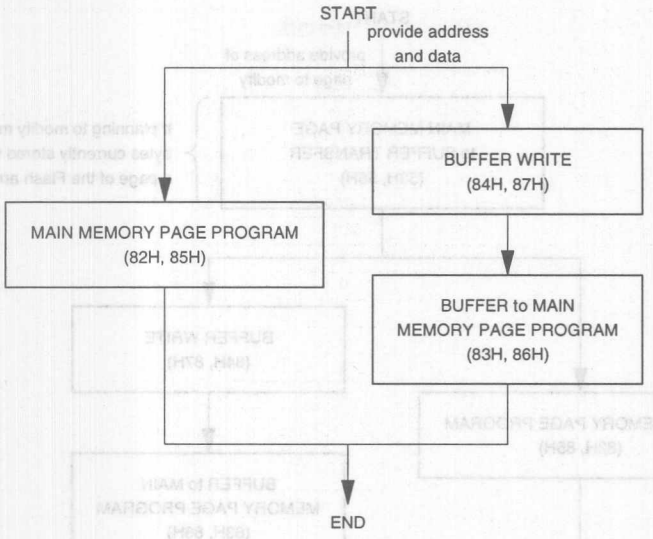
Table 2.

Buffer 1 to Main Memory Page Program with Built-In Erase	Buffer 2 to Main Memory Page Program with Built-In Erase	Buffer 1 to Main Memory Page Program without Built-In Erase	Buffer 2 to Main Memory Page Program without Built-In Erase	Main Memory Page Program Through Buffer 1	Main Memory Page Program Through Buffer 2	Auto Page Rewrite Through Buffer 1	Auto Page Rewrite Through Buffer 2	Status Register
Opcode								
83H	86H	88H	89H	82H	85H	58H	59H	57H
1	1	1	1	1	1	0	0	0
0	0	0	0	0	0	1	1	1
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1	1
0	0	1	1	0	0	1	1	0
0	1	0	0	0	1	0	0	1
1	1	0	0	1	0	0	0	1
1	0	0	1	0	1	0	1	1
r	r	r	r	r	r	r	r	
r	r	r	r	r	r	r	r	
r	r	r	r	r	r	r	r	
r	r	r	r	r	r	r	r	
PA10	PA10	PA10	PA10	PA10	PA10	PA10	PA10	
PA9	PA9	PA9	PA9	PA9	PA9	PA9	PA9	
PA8	PA8	PA8	PA8	PA8	PA8	PA8	PA8	
PA7	PA7	PA7	PA7	PA7	PA7	PA7	PA7	
PA6	PA6	PA6	PA6	PA6	PA6	PA6	PA6	
PA5	PA5	PA5	PA5	PA5	PA5	PA5	PA5	
PA4	PA4	PA4	PA4	PA4	PA4	PA4	PA4	
PA3	PA3	PA3	PA3	PA3	PA3	PA3	PA3	
PA2	PA2	PA2	PA2	PA2	PA2	PA2	PA2	
PA1	PA1	PA1	PA1	PA1	PA1	PA1	PA1	
PA0	PA0	PA0	PA0	PA0	PA0	PA0	PA0	
X	X	X	X	BA8	BA8	X	X	
X	X	X	X	BA7	BA7	X	X	
X	X	X	X	BA6	BA6	X	X	
X	X	X	X	BA5	BA5	X	X	
X	X	X	X	BA4	BA4	X	X	
X	X	X	X	BA3	BA3	X	X	
X	X	X	X	BA2	BA2	X	X	
X	X	X	X	BA1	BA1	X	X	
X	X	X	X	BA0	BA0	X	X	

X (Don't Care)

r (reserved bits)

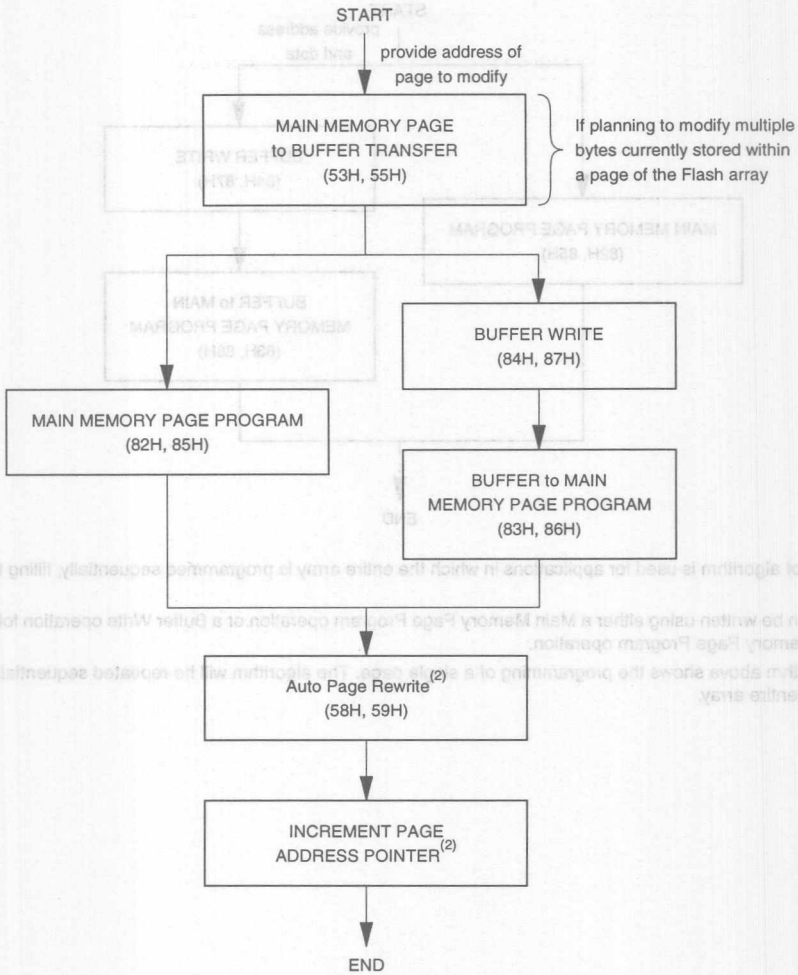
Figure 1. Algorithm for Programming or Reprogramming of the Entire Array Sequentially



Notes:
1. This type of algorithm is used for applications in which the entire array is programmed sequentially, filling the array page-by-page.
2. A page can be written using either a Main Memory Page Program operation or a Buffer Write operation followed by a Buffer to Main Memory Page Program operation.
3. The algorithm above shows the programming of a single page. The algorithm will be repeated sequentially for each page within the entire array.

4

Figure 2. Algorithm for Randomly Modifying Data



Notes:
1. To preserve data integrity, each page of the DataFlash memory array must be updated/rewritten at least once within every 10,000 cumulative page erase/program operations.
2. A Page Address Pointer must be maintained to indicate which page is to be rewritten. The Auto Page Rewrite command must use the address specified by the Page Address Pointer.
3. Other algorithms can be used to rewrite portions of the Flash array. Low power applications may choose to wait until 10,000 cumulative page erase/program operations have accumulated before rewriting all pages of the Flash array. See application note AN-4 ("Using Atmel's Serial DataFlash") for more details.

Ordering Information

f_{SCK} (MHz)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
5	10	0.02	AT45DB041-JC AT45DB041-RC AT45DB041-TC AT45DB041-CC	32J 28R 28T 24C1	Commercial (0°C to 70°C)
5	10	0.02	AT45DB041-JI AT45DB041-RI AT45DB041-TI AT45DB041-CI	32J 28R 28T 24C1	Industrial (-40°C to 85°C)

4

Package Type	
32J	32-Lead, Plastic J-Leaded Chip Carrier Package (PLCC)
28R	28-Lead, 0.330" Wide, Plastic Gull-Wing Small Outline Package (SOIC)
28T	28-Lead, Plastic Thin Small Outline Package (TSOP)
24C1	24-Ball, 5 x 5 Array Plastic Chip-Scale Ball Grid Array (CBGA)

f_{OSC} (MHz)	I_{CC} (mA) Active	I_{CC} (mA) Standby	Ordering Code	Package	Operation Range
5	10	0.02	AT45DB041-JC AT45DB041-RC AT45DB041-TC AT45DB041-CC	32J 28R 28T 24C1	Commercial (0°C to 70°C)
5	10	0.02	AT45DB041-JI AT45DB041-RI AT45DB041-TI AT45DB041-CI	32J 28R 28T 24C1	Industrial (-40°C to 85°C)

Package	Package Type
32J	32-Lead, Plastic J-Leaded Chip Carrier Package (PLCC)
28R	28-Lead, 0.330" Wide, Plastic Gull-Wing Small Outline Package (SOIC)
28T	28-Lead, Plastic Thin Small Outline Package (TSOP)
24C1	24-Ball, 5 x 5 Array Plastic Chip-Scale Ball Grid Array (CBGA)

Features

- Single 2.7V - 3.6V Supply
- Sequential Access, Parallel I/O Architecture
- Page Program Operation
  - Single Cycle Reprogram (Erase and Program)
  - 4096 Pages (264 Bytes/Page) Main Memory
- Two 264-Byte Data Buffers – Allows Receiving of Data while Reprogramming of Nonvolatile Memory
- Internal Program and Control Timer
- Fast Page Program Time – 7 ms Typical
- 120 µs Typical Page to Buffer Transfer Time
- Low Power Dissipation
  - 4 mA Active Read Current Typical
  - 2 µA CMOS Standby Current Typical
- 2 MHz Max Clock Frequency
- Hardware Data Protection Feature
- Synchronous Clocking (Two Modes)
- CMOS and TTL Compatible Inputs and Outputs
- Commercial and Industrial Temperature Ranges

Description

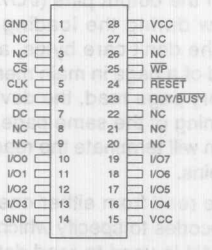
The AT45DB080 is a 2.7-volt only, sequential access, parallel interface Flash memory suitable for in-system reprogramming. Its 8,650,752 bits of memory are organized as 4096 pages of 264-bytes each. In addition to the main memory, the AT45DB080 also contains two data buffers of 264-bytes each. The buffers allow receiving of data while a page in the main memory is being reprogrammed. Unlike conventional Flash memories that are accessed randomly with multiple address lines and a parallel interface,

(continued)

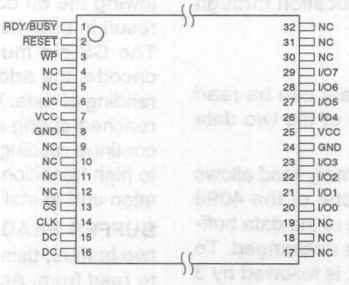
Pin Configurations

Pin Name	Function
$\overline{CS}$	Chip Select
CLK	Clock
I/O7-I/O0	Input/Output
$\overline{WP}$	Hardware Page Write Protect Pin
$\overline{RESET}$	Chip Reset
RDY/$\overline{BUSY}$	Ready/Busy

SOIC



TSOP Top View
Type 1



Note: SOIC pins 6 and 7 and TSOP pins 15 and 16 are DON'T CONNECT.

8-Megabit 2.7-volt Only Sequential Access Parallel I/O DataFlash®

4

AT45DB080 Preliminary

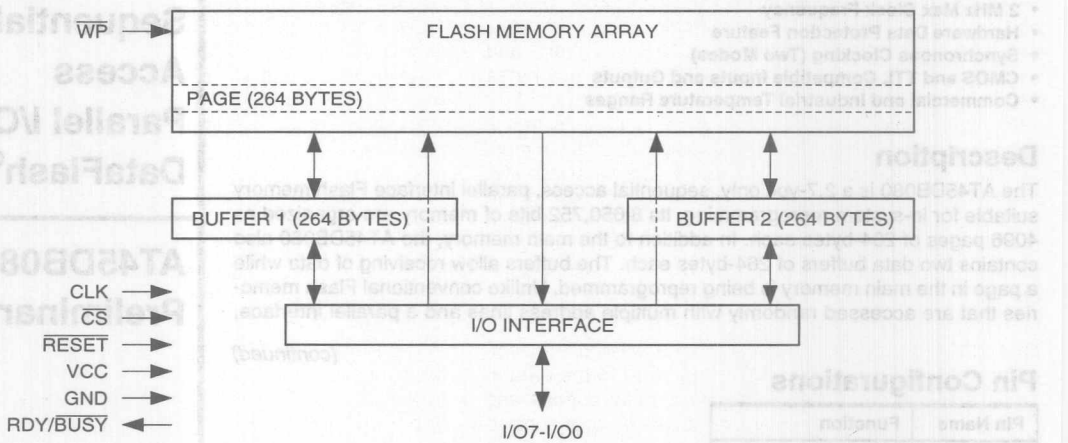
Rev. 1075B–06/98

the DataFlash uses a parallel interface to sequentially access its data. The simple sequential access facilitates hardware layout, increases system reliability, minimizes switching noise, and reduces package size and active pin count. The device is optimized for use in many commercial and industrial applications where high density, low pin count, low voltage, and low power are essential. Typical applications for the DataFlash are digital voice storage, image storage, and data storage. The device operates at clock frequencies up to 2 MHz with a typical active read current consumption of 4 mA.

To allow for simple in-system reprogrammability, the AT45DB080 does not require high input voltages for programming. The device operates from a single power supply, 2.7V to 3.6V, for both the program and read operations. The AT45DB080 is enabled through the chip select pin ($\overline{CS}$) and accessed via an interface consisting of the parallel input/output (I/O7-I/O0) pins and the clock (CLK) pin.

All programming cycles are self-timed, and no separate erase cycle is required before programming.

Block Diagram



Device Operation

The device operation is controlled by instructions from the host processor. The list of instructions and their associated opcodes are contained in Table 1 and Table 2. A valid instruction starts with the falling edge of $\overline{CS}$ followed by the appropriate 1-byte opcode and the desired buffer or main memory address location. While the $\overline{CS}$ pin is low, toggling the CLK pin controls the loading of the opcode and the desired buffer or main memory address location through the input pins (I/O7-I/O0).

Read

By specifying the appropriate opcode, data can be read from the main memory or from either one of the two data buffers.

MAIN MEMORY PAGE READ: A main memory read allows the user to read data directly from any one of the 4096 pages in the main memory, bypassing both of the data buffers and leaving the contents of the buffers unchanged. To start a page read, the 1-byte opcode, 52H, is followed by 3 address bytes (which comprise the 24 page and byte address bits) and 60 don't care bytes. In the AT45DB080, the first three address bits are reserved for larger density devices (see Notes on page 64), the next 12 address bits (PA11-PA0) specify the page address, and the next nine address bits (BA8-BA0) specify the starting byte address within the page. The 60 don't care bytes which follow the 3 address bytes are sent to initialize the read operation. Following the 60 don't care bytes, additional pulses on CLK result in data being output on the output pins (I/O7-I/O0). The $\overline{CS}$ pin must remain low during the loading of the opcode, the address bytes, the don't care bytes, and the reading of data. When the end of a page in main memory is reached during a main memory page read, the device will continue reading at the beginning of the same page. A low to high transition on the $\overline{CS}$ pin will terminate the read operation and tri-state the output pins.

BUFFER READ: Data can be read from either one of the two buffers, using different opcodes to specify which buffer to read from. An opcode of 54H is used to read data from buffer 1, and an opcode of 56H is used to read data from

buffer 2. To perform a buffer read, the 1-byte opcode must be followed by the three address bytes comprised of 15 don't care bits and nine address bits. Following the three address bytes, an additional don't care byte must be clocked in to initialize the read operation. Since the buffer size is 264-bytes, nine address bits (BFA8-BFA0) are required to specify the first byte of data to be read from the buffer. The $\overline{CS}$ pin must remain low during the loading of the opcode, the address bytes, the don't care bytes, and the reading of data. When the end of a buffer is reached, the device will continue reading back at the beginning of the buffer. A low to high transition on the $\overline{CS}$ pin will terminate the read operation and tri-state the output pins.

MAIN MEMORY PAGE TO BUFFER TRANSFER: A page of data can be transferred from the main memory to either buffer 1 or buffer 2. A 1-byte opcode, 53H for buffer 1 and 55H for buffer 2, is followed by the three address bytes comprised of the three reserved bits, 12 address bits (PA11-PA0) which specify the page in main memory that is to be transferred, and nine don't care bits. The $\overline{CS}$ pin must be low while toggling the CLK pin to load the opcode and the address bytes from the input pins. The transfer of the page of data from the main memory to the buffer will begin when the $\overline{CS}$ pin transitions from a low to a high state. During the transfer of a page of data (t_{XFR}), the status register can be read to determine whether the transfer has been completed or not.

MAIN MEMORY PAGE TO BUFFER COMPARE: A page of data in main memory can be compared to the data in buffer 1 or buffer 2. A 1-byte opcode, 60H for buffer 1 and 61H for buffer 2, is followed by three address bytes consisting of three reserved bits, 12 address bits (PA11-PA0) which specify the page in the main memory that is to be compared to the buffer, and nine don't care bits. The loading of the opcode and the address bits is the same as described previously. The $\overline{CS}$ pin must be low while toggling the CLK pin to load the opcode and the address bytes from the input pins. On the low to high transition of the $\overline{CS}$ pin, the 264 bytes in the selected main memory page will be compared with the 264 bytes in buffer 1 or buffer 2. During this time (t_{XFR}), the status register will indicate that the part is busy. On completion of the compare operation, bit 6 of the status register is updated with the result of the compare.

Program

BUFFER WRITE: Data can be clocked in from the input pins into either buffer 1 or buffer 2. To load data into either buffer, a 1-byte opcode, 84H for buffer 1 or 87H for buffer 2, is followed by the three address bytes comprised of 15 don't care bits and nine address bits (BFA8-BFA0). The nine address bits specify the first byte in the buffer to be written. The data is entered following the address bits. If the end of the data buffer is reached, the device will wrap around back to the beginning of the buffer. Data will continue to be loaded into the buffer until a low to high transition is detected on the $\overline{CS}$ pin.

BUFFER TO MAIN MEMORY PAGE PROGRAM WITH BUILT-IN ERASE: Data written into either buffer 1 or buffer 2 can be programmed into the main memory. A 1-byte opcode, 83H for buffer 1 or 86H for buffer 2, is followed by the three address bytes consisting of three reserved bits, 12 address bits (PA11-PA0) that specify the page in the main memory to be written, and nine additional don't care bits. When a low-to-high transition occurs on the $\overline{CS}$ pin, the part will first erase the selected page in main memory to all 1s and then program the data stored in the buffer into the specified page in the main memory. Both the erase and the programming of the page are internally self timed and should take place in a maximum time of t_{EP}. During this time, the status register will indicate that the part is busy.

BUFFER TO MAIN MEMORY PAGE PROGRAM WITHOUT BUILT-IN ERASE: A previously erased page within main memory can be programmed with the contents of either buffer 1 or buffer 2. A 1-byte opcode, 88H for buffer 1 or 89H for buffer 2, is followed by three address bytes consisting of three reserved bits, 12 address bits (PA11-PA0) that specify the page in the main memory to be written, and nine additional don't care bits. When a low to high transition occurs on the $\overline{CS}$ pin, the part will program the data stored in the buffer into the specified page in the main memory. It is necessary that the page in main memory that is being programmed has been previously programmed to all 1s (erased state). The programming of the page is internally self timed and should take place in a maximum time of t_P. During this time, the status register will indicate that the part is busy.

MAIN MEMORY PAGE PROGRAM: This operation is a combination of the Buffer Write and Buffer to Main Memory Page Program with Built-In Erase operations. Data is first clocked into buffer 1 or buffer 2 from the input pins and then programmed into a specified page in the main memory. A 1-byte opcode, 82H for buffer 1 or 85H for buffer 2, is followed by three address bytes comprised of three reserved bits and 21 address bits. The 12 most significant address bits (PA11-PA0) select the page in the main memory where data is to be written, and the next nine address bits (BFA8-BFA0) select the first byte in the buffer to be written. After all address bytes are clocked in, the part will take data from the input pins and store it in one of the data buffers. If the end of the buffer is reached, the device will wrap around back to the beginning of the buffer. When there is a low to high transition on the $\overline{CS}$ pin, the part will first erase the selected page in main memory to all 1s and then program the data stored in the buffer into the specified page in the main memory. Both the erase and the programming of the page are internally self timed and should take

place in a maximum of time t_{EP}. During this time, the status register will indicate that the part is busy.

AUTO PAGE REWRITE: This mode is only needed if multiple bytes within a page or multiple pages of data are modified in a random fashion. This mode is a combination of two operations: Main Memory Page to Buffer Transfer and Buffer to Main Memory Page Program with Built-In Erase. A page of data is first transferred from the main memory to buffer 1 or buffer 2, and then the same data (from buffer 1 or buffer 2) is programmed back into its original page of main memory. A 1-byte opcode, 58H for buffer 1 or 59H for buffer 2, is followed by the three address bytes comprised of three reserved bits, 12 address bits (PA11-PA0) that specify the page in main memory to be rewritten, and nine additional don't care bits. When a low to high transition occurs on the $\overline{CS}$ pin, the part will first transfer data from the page in main memory to a buffer and then program the data from the buffer back into same page of main memory. The operation is internally self-timed and should take place in a maximum time of t_{EP}. During this time, the status register will indicate that the part is busy.

If the main memory is programmed or reprogrammed sequentially page by page, then the programming algorithm shown in Figure 1 is recommended. Otherwise, if multiple bytes in a page or several pages are programmed randomly in the main memory, then the programming algorithm shown in Figure 2 is recommended.

STATUS REGISTER: The status register can be used to determine the device's ready/busy status, the result of a Main Memory Page to Buffer Compare operation, or the device density. To read the status register, an opcode of 57H must be loaded into the device. After the opcode is clocked in, the 1-byte status register will be clocked out on the output pins during the next clock cycle. The five most-significant bits of the status register will contain device information, while the remaining three least-significant bits are reserved for future use and will have undefined values. After the one byte of the status register has been clocked out, the sequence will repeat itself (as long as $\overline{CS}$ remains low and CLK is being toggled). The data in the status register is constantly updated, so each repeating sequence will output new data.

Ready/busy status is indicated using bit 7 of the status register. If bit 7 is a 1, then the device is not busy and is ready to accept the next command. If bit 7 is a 0, then the device is in a busy state. The user can continuously poll bit 7 of the status register on I/O7 by stopping CLK once bit 7 has been output on I/O7. The status of bit 7 will continue to be output on the I/O7 pin, and once the device is no longer busy, the state of I/O7 will change from 0 to 1. There are six operations which can cause the device to be in a busy state: Main Memory Page to Buffer Transfer, Main Memory Page to Buffer Compare, Buffer to Main Memory Page Program with Built-In Erase, Buffer to Main Memory Page Program without Built-In Erase, Main Memory Page Program, and Auto Page Rewrite.

The result of the most recent Main Memory Page to Buffer Compare operation is indicated using bit 6 of the status register. If bit 6 is a 0, then the data in the main memory page matches the data in the buffer. If bit 6 is a 1, then at least one bit of the data in the main memory page does not match the data in the buffer.

The device density is indicated using bits 5, 4, and 3 of the status register. For the AT45DB080, the three bits are 1, 0, and 0. The decimal value of these three binary bits does not equate to the device density; the three bits represent a combinational code relating to differing densities of Serial DataFlash devices, allowing a total of eight different density configurations.

Status Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RDY/$\overline{BUSY}$	COMP	1	0	0	X	X	X

Read/Program Mode Summary

The modes listed above can be separated into two groups — modes which make use of the flash memory array (Group A) and modes which do not make use of the flash memory array (Group B).

Group A modes consist of:

1. Main memory page read
2. Main memory page to buffer 1 (or 2) transfer
3. Main memory page to buffer 1 (or 2) compare
4. Buffer 1 (or 2) to main memory page program with built-in erase
5. Buffer 1 (or 2) to main memory page program without built-in erase
6. Main memory page program
7. Auto page rewrite

Group B modes consist of:

1. Buffer 1 (or 2) read
2. Buffer 1 (or 2) write
3. Status read

If a Group A mode is in progress (not fully completed) then another mode in Group A should not be started. However, during this time in which a Group A mode is in progress, modes in Group B can be started.

This gives the Serial DataFlash the ability to virtually accommodate a continuous data stream. While data is being programmed into main memory from buffer 1, data can be loaded into buffer 2 (or vice versa). See application note AN-4 ("Using Atmel's Serial DataFlash") for more details.

HARDWARE PAGE WRITE PROTECT: If the $\overline{WP}$ pin is held low, the first 256 pages of the main memory cannot be reprogrammed. The only way to reprogram the first 256 pages is to first drive the protect pin high and then use the program commands previously mentioned. The $\overline{WP}$ pin is internally pulled high; therefore, in low pin count applications, connection of the $\overline{WP}$ pin is not necessary if this pin and feature will not be utilized. However, it is recommended that the $\overline{WP}$ pin be driven high externally whenever possible.

$\overline{RESET}$: A low state on the reset pin ($\overline{RESET}$) will terminate the operation in progress and reset the internal state machine to an idle state. The device will remain in the reset condition as long as a low level is present on the $\overline{RESET}$ pin. Normal operation can resume once the $\overline{RESET}$ pin is brought back to a high level.

The device incorporates an internal power-on reset circuit, so there are no restrictions on the $\overline{RESET}$ pin during power-on sequences. The $\overline{RESET}$ pin is also internally pulled high; therefore, in low pin count applications, connection of the $\overline{RESET}$ pin is not necessary if this pin and feature will not be utilized. However, it is recommended that the $\overline{RESET}$ pin be driven high externally whenever possible.

READY/$\overline{BUSY}$: This open drain output pin will be driven low when the device is busy in an internally self-timed operation. This pin, which is normally in a high state (through an external pull-up resistor), will be pulled low during programming operations, compare operations, and during page-to-buffer transfers.

The busy status indicates that the Flash memory array and one of the buffers cannot be accessed; read and write operations to the other buffer can still be performed.

Power On/Reset State

When power is first applied to the device, or when recovering from a reset condition, the device will default to the "Inactive Clock Polarity High" mode. In addition, the output pins (I/O_7 - I/O_0) will be in a high impedance state, and a high to low transition on the $\overline{CS}$ pin will be required to start a valid instruction. The Clock Polarity mode will be automatically selected on every falling edge of $\overline{CS}$ by sampling the inactive clock state.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC and AC Operating Range

		AT45DB081
Operating Temperature (Case)	Com.	0°C to 70°C
	Ind.	-40°C to 85°C
V_{CC} Power Supply[1]		2.7V to 3.6V

Note: 1. After power is applied and V_{CC} is at the minimum specified data sheet value, the system should wait 20 ms before an operational mode is started.

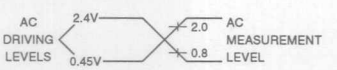
DC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{SB}	Standby Current	$\overline{CS}$, $\overline{RESET}$, $\overline{WP}$ = V_{IH}, all inputs at CMOS levels		2	10	µA
I_{CC1}	Active Current, Read Operation	f = 2 MHz; I_{OUT} = 0 mA; V_{CC} = 3.6V		4	10	mA
I_{CC2}	Active Current, Program/Erase Operation			15	35	mA
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}			1	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}			1	µA
V_{IL}	Input Low Voltage				0.6	V
V_{IH}	Input High Voltage		2.0			V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA; V_{CC} = 2.7V			0.4	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA	V_{CC} - 0.2V			V

AC Characteristics

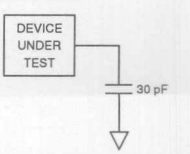
Symbol	Parameter	Min	Typ	Max	Units
f_{SCK}	SCK Frequency			2	MHz
t_{WH}	SCK High Time	200			ns
t_{WL}	SCK Low Time	200			ns
t_{CS}	Minimum $\overline{CS}$ High Time	250			ns
t_{CSS}	$\overline{CS}$ Setup Time	250			ns
t_{CSH}	$\overline{CS}$ Hold Time	250			ns
t_{CSB}	$\overline{CS}$ High to RDY/$\overline{BUSY}$ Low			200	ns
t_{SU}	Data In Setup Time	20			ns
t_H	Data In Hold Time	50			ns
t_{HO}	Output Hold Time	0			ns
t_{DIS}	Output Disable Time			150	ns
t_V	Output Valid			180	ns
t_{XFR}	Page to Buffer Transfer/Compare Time		120	250	µs
t_{EP}	Page Erase and Programming Time		10	20	ms
t_P	Page Programming Time		7	14	ms
t_{RST}	$\overline{RESET}$ Pulse Width	10			µs
t_{REC}	$\overline{RESET}$ Recovery Time			1	µs

Input Test Waveforms and Measurement Levels



t_R, t_F < 20 ns (10% to 90%)

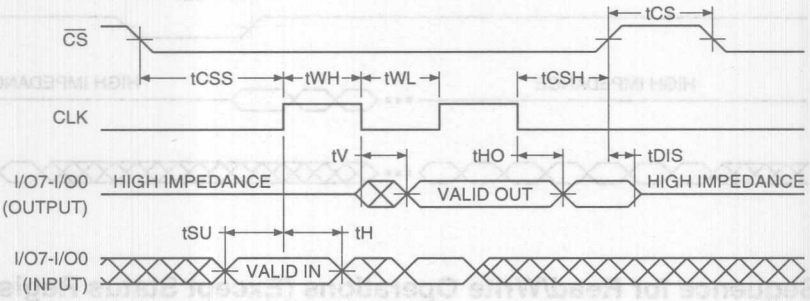
Output Test Load



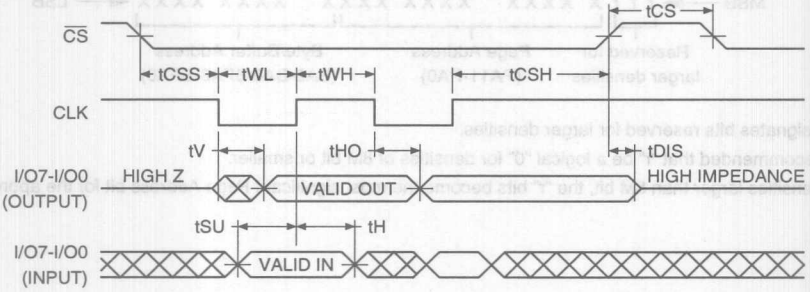
AC Waveforms

Two different timing diagrams are shown below. Waveform 1 shows the CLK signal being low when $\overline{CS}$ makes a high-to-low transition, and Waveform 2 shows the CLK signal being high when $\overline{CS}$ makes a high-to-low transition. Both waveforms show valid timing diagrams. The setup and hold times for the SI signal are referenced to the low-to-high transition on the CLK signal.

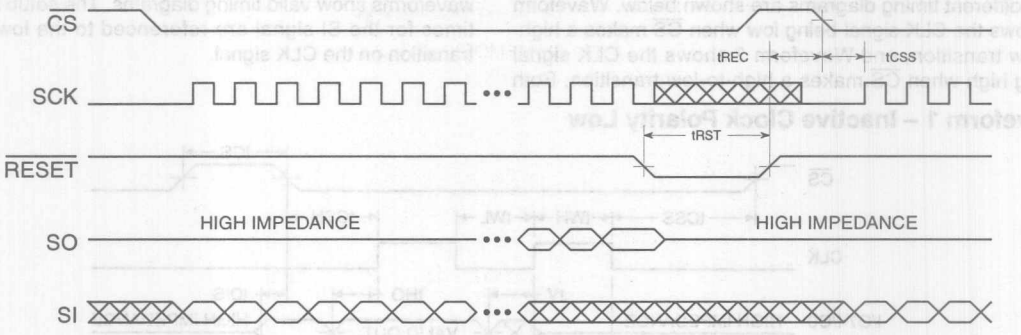
Waveform 1 – Inactive Clock Polarity Low



Waveform 2 – Inactive Clock Polarity High

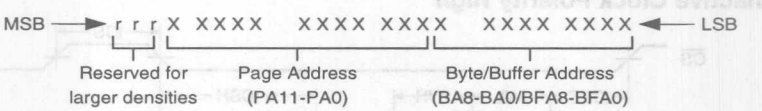


Reset Timing (Inactive Clock Polarity Low Shown)



Command Sequence for Read/Write Operations (Except Status Register Read)

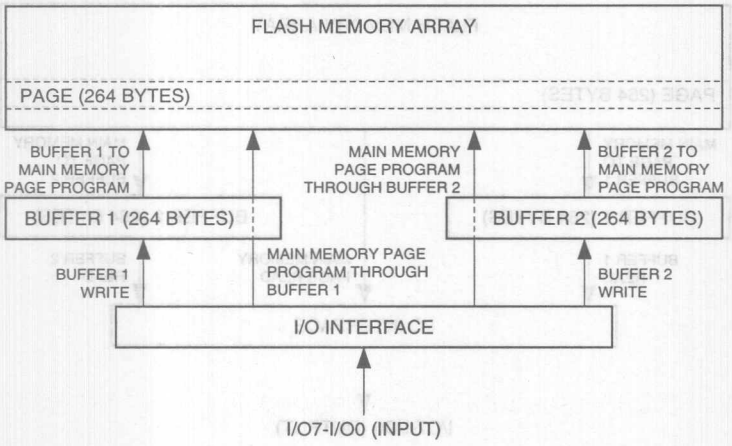




Notes: 1. "r" designates bits reserved for larger densities.
2. It is recommended that "r" be a logical "0" for densities of 8M bit or smaller.
3. For densities larger than 8M bit, the "r" bits become the most significant Page Address bit for the appropriate density.

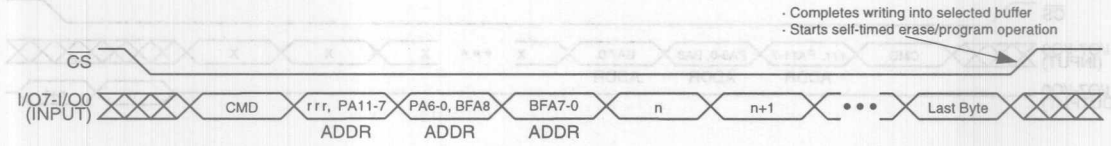
Write Operations

The following block diagram and waveforms illustrate the various write sequences available.

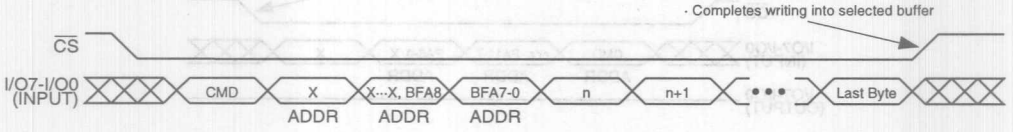


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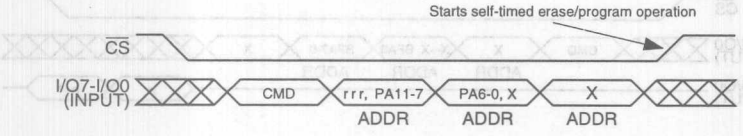
Main Memory Page Program through Buffers



Buffer Write



Buffer to Main Memory Page Program (Data from Buffer Programmed into Flash Page)

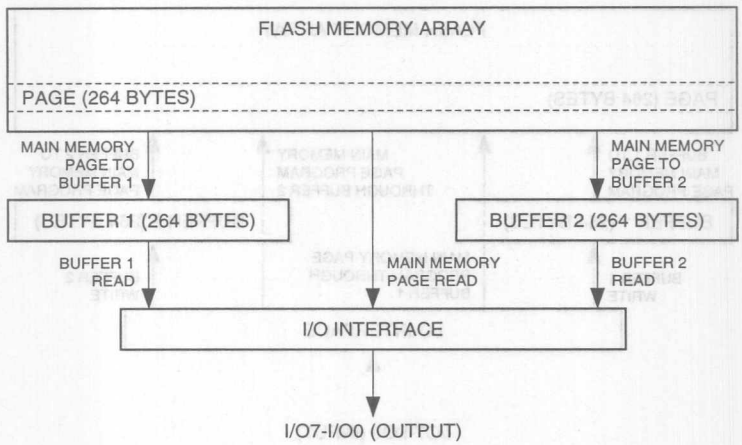


Each transition represents 8 bits and 1 clock cycle

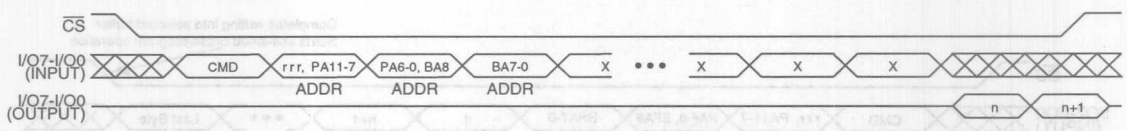
n = 1st byte written
n+1 = 2nd byte written

Read Operations

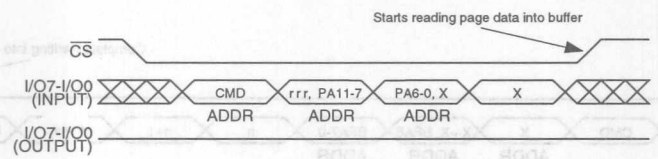
The following block diagram and waveforms illustrate the various read sequences available.



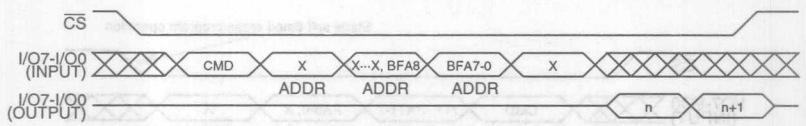
Main Memory Page Read

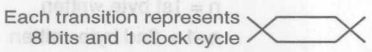


Main Memory Page to Buffer Transfer (Data from Flash Page Read into Buffer)



Buffer Read

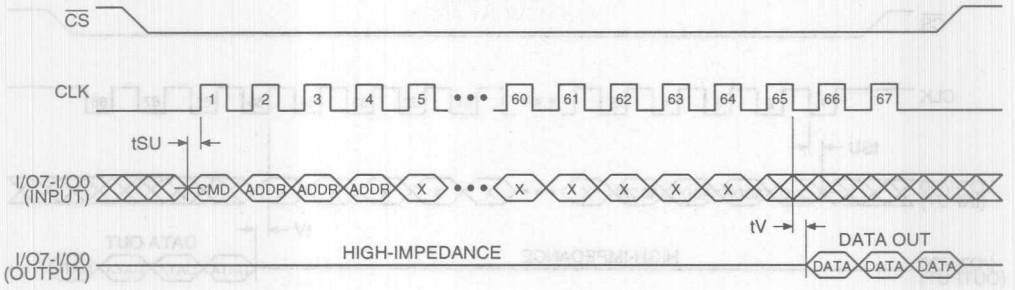




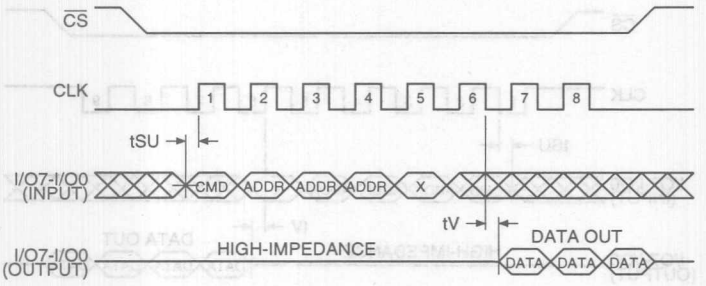
n = 1st byte written
n+1 = 2nd byte written

Detailed Read Timing – Inactive Clock Polarity Low

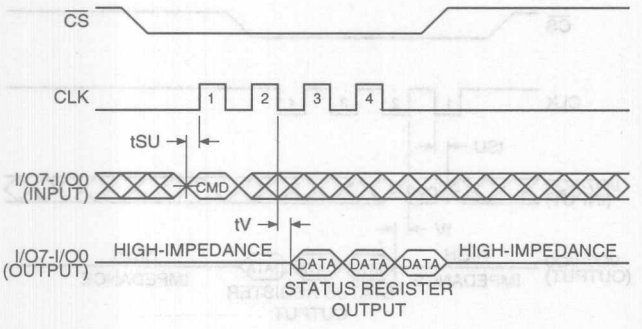
Main Memory Page Read



Buffer Read

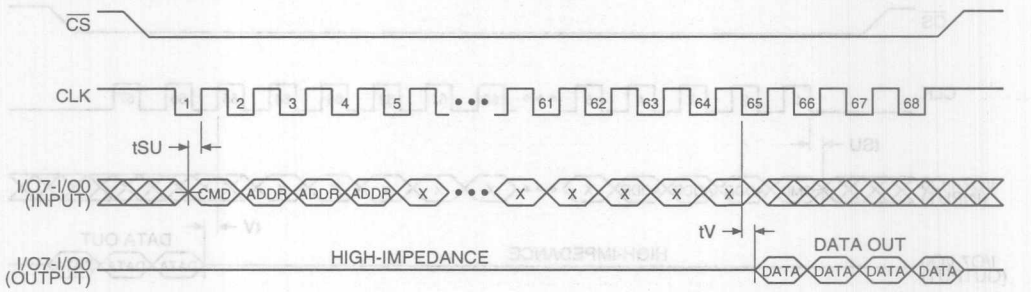


Status Register Read

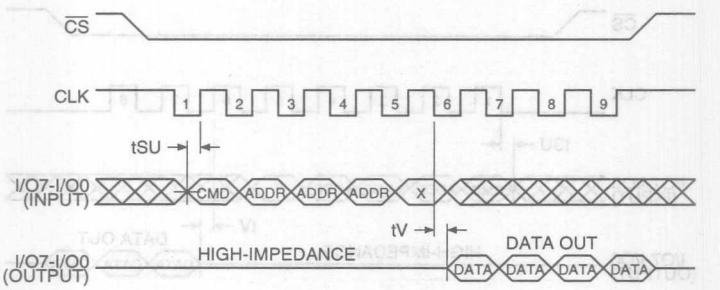


Detailed Read Timing – Inactive Clock Polarity High

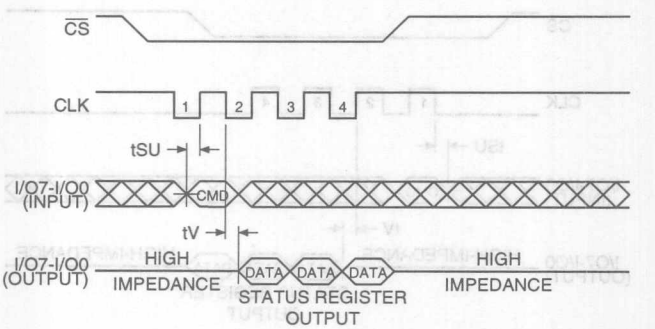
Main Memory Page Read



Buffer Read



Status Register Read



X (Don't Care)
r (reserved bits)

Table 1.

CLK	I/O	Main Memory Page Read	Buffer 1 Read	Buffer 2 Read	Main Memory Page to Buffer 1 Transfer	Main Memory Page to Buffer 2 Transfer	Main Memory Page to Buffer 1 Compare	Main Memory Page to Buffer 2 Compare	Buffer 1 Write	Buffer 2 Write
		Opcode								
		52H	54H	56H	53H	55H	60H	61H	84H	87H
1	7	0	0	0	0	0	0	0	1	1
	6	1	1	1	1	1	1	1	0	0
	5	0	0	0	0	0	1	1	0	0
	4	1	1	1	1	1	0	0	0	0
	3	0	0	0	0	0	0	0	0	0
	2	0	1	1	0	1	0	0	1	1
	1	1	0	1	1	0	0	0	0	1
	0	0	0	0	1	1	0	1	0	1
2	7	r	X	X	r	r	r	r	X	X
	6	r	X	X	r	r	r	r	X	X
	5	r	X	X	r	r	r	r	X	X
	4	PA11	X	X	PA11	PA11	PA11	PA11	X	X
	3	PA10	X	X	PA10	PA10	PA10	PA10	X	X
	2	PA9	X	X	PA9	PA9	PA9	PA9	X	X
	1	PA8	X	X	PA8	PA8	PA8	PA8	X	X
	0	PA7	X	X	PA7	PA7	PA7	PA7	X	X
3	7	PA6	X	X	PA6	PA6	PA6	PA6	X	X
	6	PA5	X	X	PA5	PA5	PA5	PA5	X	X
	5	PA4	X	X	PA4	PA4	PA4	PA4	X	X
	4	PA3	X	X	PA3	PA3	PA3	PA3	X	X
	3	PA2	X	X	PA2	PA2	PA2	PA2	X	X
	2	PA1	X	X	PA1	PA1	PA1	PA1	X	X
	1	PA0	X	X	PA0	PA0	PA0	PA0	X	X
	0	BA8	BFA8	BFA8	X	X	X	X	BFA8	BFA8
4	7	BA7	BFA7	BFA7	X	X	X	X	BFA7	BFA7
	6	BA6	BFA6	BFA6	X	X	X	X	BFA6	BFA6
	5	BA5	BFA5	BFA5	X	X	X	X	BFA5	BFA5
	4	BA4	BFA4	BFA4	X	X	X	X	BFA4	BFA4
	3	BA3	BFA3	BFA3	X	X	X	X	BFA3	BFA3
	2	BA2	BFA2	BFA2	X	X	X	X	BFA2	BFA2
	1	BA1	BFA1	BFA1	X	X	X	X	BFA1	BFA1
	0	BA0	BFA0	BFA0	X	X	X	X	BFA0	BFA0
5	7	X	X	X						
	6	X	X	X						
	5	X	X	X						
	4	X	X	X						
	3	X	X	X						
	2	X	X	X						
	1	X	X	X						
	0	X	X	X						
• • •		• • •								
64	7	X								
	6	X								
	5	X								
	4	X								
	3	X								
	2	X								
	1	X								
	0	X								

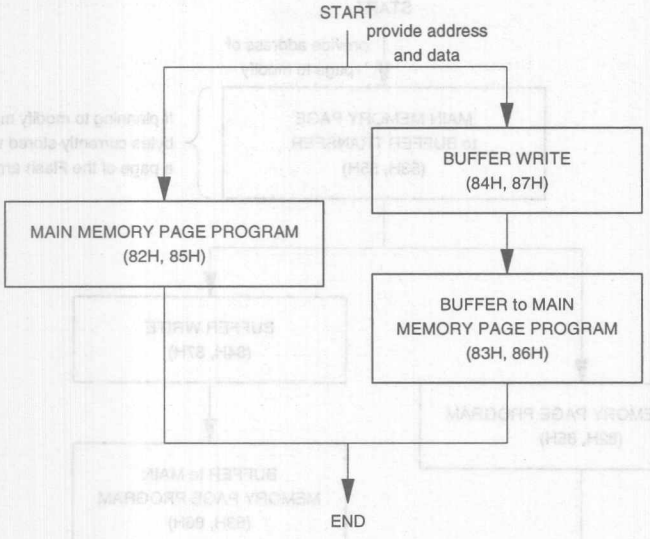
X (Don't Care)
r (reserved bits)

4

Table 2.

		Buffer 1 to Main Memory Page Program with Built-In Erase	Buffer 2 to Main Memory Page Program with Built-In Erase	Buffer 1 to Main Memory Page Program without Built-In Erase	Buffer 2 to Main Memory Page Program without Built-In Erase	Main Memory Page Program Through Buffer 1	Main Memory Page Program Through Buffer 2	Auto Page Rewrite Through Buffer 1	Auto Page Rewrite Through Buffer 2	Status Register
		Opcode								
CLK	I/O	83H	86H	88H	89H	82H	85H	58H	59H	57H
1	7	1	1	1	1	1	1	0	0	0
	6	0	0	0	0	0	0	1	1	1
	5	0	0	0	0	0	0	0	0	0
	4	0	0	0	0	0	0	1	1	1
	3	0	0	1	1	0	0	1	1	0
	2	0	1	0	0	0	1	0	0	1
	1	1	1	0	0	1	0	0	0	1
	0	1	0	0	1	0	1	0	1	1
2	7	r	r	r	r	r	r	r	r	
	6	r	r	r	r	r	r	r	r	
	5	r	r	r	r	r	r	r	r	
	4	PA11	PA11	PA11	PA11	PA11	PA11	PA11	PA11	
	3	PA10	PA10	PA10	PA10	PA10	PA10	PA10	PA10	
	2	PA9	PA9	PA9	PA9	PA9	PA9	PA9	PA9	
	1	PA8	PA8	PA8	PA8	PA8	PA8	PA8	PA8	
	0	PA7	PA7	PA7	PA7	PA7	PA7	PA7	PA7	
3	7	PA6	PA6	PA6	PA6	PA6	PA6	PA6	PA6	
	6	PA5	PA5	PA5	PA5	PA5	PA5	PA5	PA5	
	5	PA4	PA4	PA4	PA4	PA4	PA4	PA4	PA4	
	4	PA3	PA3	PA3	PA3	PA3	PA3	PA3	PA3	
	3	PA2	PA2	PA2	PA2	PA2	PA2	PA2	PA2	
	2	PA1	PA1	PA1	PA1	PA1	PA1	PA1	PA1	
	1	PA0	PA0	PA0	PA0	PA0	PA0	PA0	PA0	
	0	X	X	X	X	BA8	BA8	X	X	
4	7	X	X	X	X	BA7	BA7	X	X	
	6	X	X	X	X	BA6	BA6	X	X	
	5	X	X	X	X	BA5	BA5	X	X	
	4	X	X	X	X	BA4	BA4	X	X	
	3	X	X	X	X	BA3	BA3	X	X	
	2	X	X	X	X	BA2	BA2	X	X	
	1	X	X	X	X	BA1	BA1	X	X	
	0	X	X	X	X	BA0	BA0	X	X	

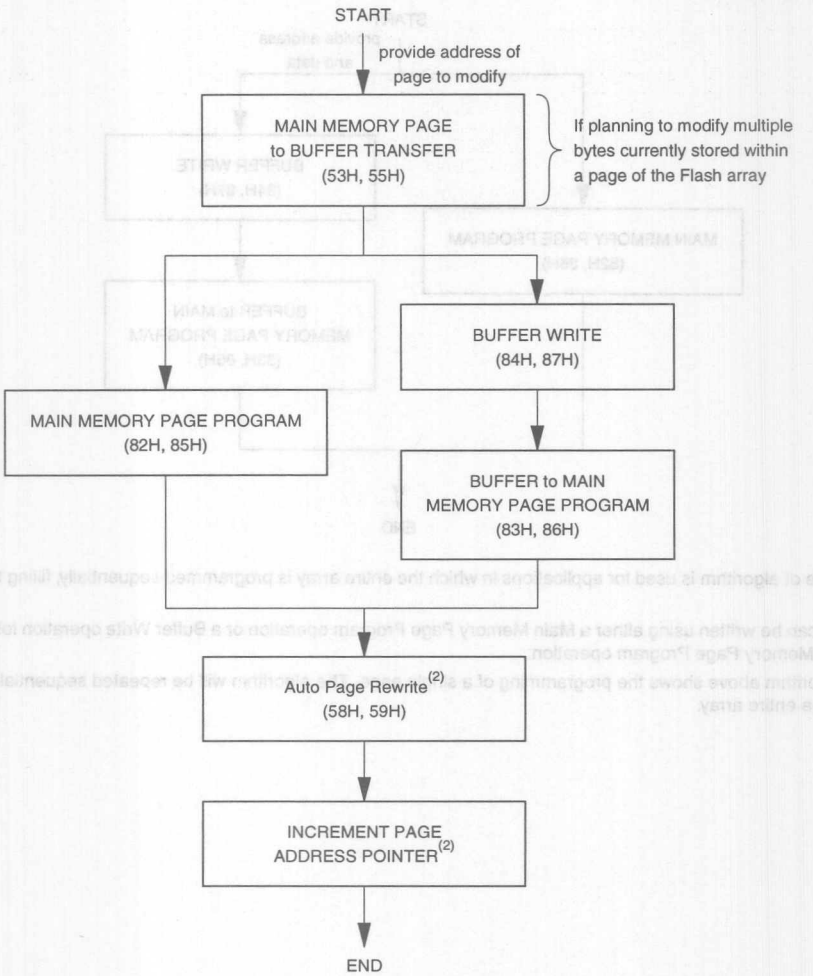
Figure 1. Algorithm for Programming or Reprogramming of the Entire Array Sequentially



Notes:
1. This type of algorithm is used for applications in which the entire array is programmed sequentially, filling the array page-by-page.
2. A page can be written using either a Main Memory Page Program operation or a Buffer Write operation followed by a Buffer to Main Memory Page Program operation.
3. The algorithm above shows the programming of a single page. The algorithm will be repeated sequentially for each page within the entire array.

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Figure 2. Algorithm for Randomly Modifying Data



Note:
1. To preserve data integrity, each page of the DataFlash memory array must be updated/rewritten at least once within every 10,000 cumulative page erase/program operations.
2. A Page Address Pointer must be maintained to indicate which page is to be rewritten. The Auto Page Rewrite command must use the address specified by the Page Address Pointer.
3. Other algorithms can be used to rewrite portions of the Flash array. Low power applications may choose to wait until 10,000 cumulative page erase/program operations have accumulated before rewriting all pages of the Flash array. See application note AN-4 ("Using Atmel's Serial DataFlash") for more details.

Ordering Information

f_{SCK} (MHz)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
2	10	0.01	AT45DB080-RC AT45DB080-TC	28R 32T	Commercial (0°C to 70°C)
2	10	0.01	AT45DB080-RI AT45DB080-TI	28R 32T	Industrial (-40°C to 85°C)

4

Package Type	
28R	28-Lead, 0.330" Wide, Plastic Gull-Wing Small Outline Package (SOIC)
32T	32-Lead, Plastic Thin Small Outline Package (TSOP)

Features

- Single 2.7V - 3.6V Supply
- Serial Interface Architecture
- Page Program Operation
  - Single Cycle Reprogram (Erase and Program)
  - 4096 Pages (264 Bytes/Page) Main Memory
- Two 264-Byte SRAM Data Buffers – Allows Receiving of Data while Reprogramming of Nonvolatile Memory
- Internal Program and Control Timer
- Fast Page Program Time – 7 ms Typical
- 120 µs Typical Page to Buffer Transfer Time
- Low Power Dissipation
  - 4 mA Active Read Current Typical
  - 2 µA CMOS Standby Current Typical
- 10 MHz Max Clock Frequency
- Hardware Data Protection Feature
- Serial Peripheral Interface (SPI) Compatible – Modes 0 and 3
- CMOS and TTL Compatible Inputs and Outputs
- Commercial and Industrial Temperature Ranges

Description

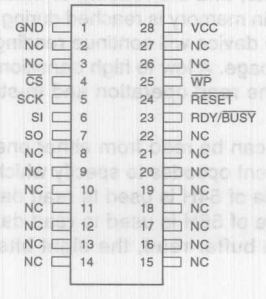
The AT45DB081 is a 2.7-volt only, serial interface Flash memory suitable for in-system reprogramming. Its 8,650,752 bits of memory are organized as 4096 pages of 264-bytes each. In addition to the main memory, the AT45DB081 also contains two SRAM data buffers of 264-bytes each. The buffers allow receiving of data while a page in the main memory is being reprogrammed. Unlike conventional Flash memories that are accessed randomly with multiple address lines and a parallel interface, the DataFlash uses a serial interface to sequentially access its data. The simple serial

(continued)

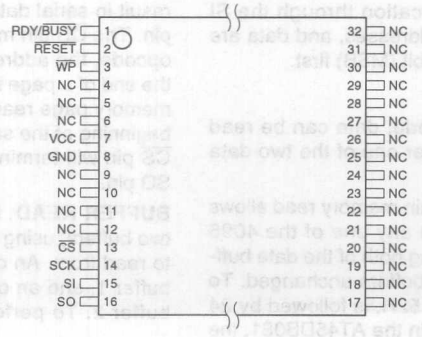
Pin Configurations

Pin Name	Function
$\overline{CS}$	Chip Select
SCK	Serial Clock
SI	Serial Input
SO	Serial Output
$\overline{WP}$	Hardware Page Write Protect Pin
$\overline{RESET}$	Chip Reset
RDY/$\overline{BUSY}$	Ready/Busy

SOIC



TSOP Top View
Type 1



8-Megabit 2.7-volt Only Serial DataFlash®

4

AT45DB081

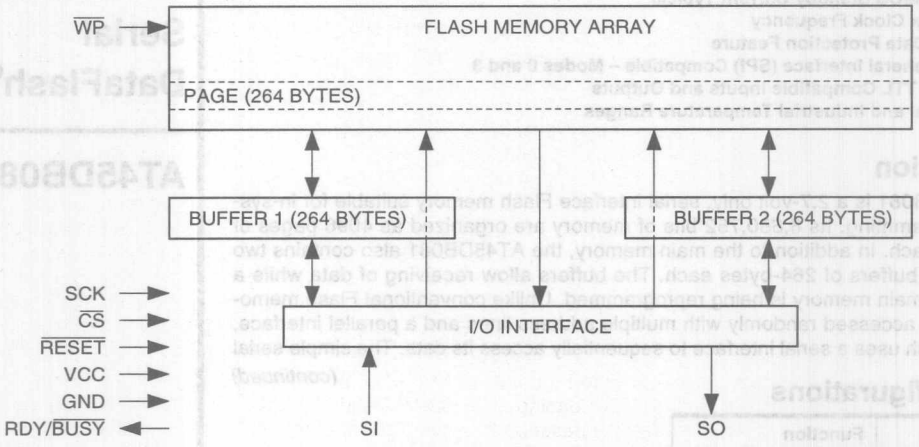
Rev. 0870B–10/98

interface facilitates hardware layout, increases system reliability, minimizes switching noise, and reduces package size and active pin count. The device is optimized for use in many commercial and industrial applications where high density, low pin count, low voltage, and low power are essential. Typical applications for the DataFlash are digital voice storage, image storage, and data storage. The device operates at clock frequencies up to 10 MHz with a typical active read current consumption of 4 mA.

To allow for simple in-system reprogrammability, the AT45DB081 does not require high input voltages for programming. The device operates from a single power supply, 2.7V to 3.6V, for both the program and read operations. The AT45DB081 is enabled through the chip select pin ($\overline{CS}$) and accessed via a three-wire interface consisting of the Serial Input (SI), Serial Output (SO), and the Serial Clock (SCK).

All programming cycles are self-timed, and no separate erase cycle is required before programming.

Block Diagram



Device Operation

The device operation is controlled by instructions from the host processor. The list of instructions and their associated opcodes are contained in Tables 1 and 2. A valid instruction starts with the falling edge of $\overline{CS}$ followed by the appropriate 8-bit opcode and the desired buffer or main memory address location. While the $\overline{CS}$ pin is low, toggling the SCK pin controls the loading of the opcode and the desired buffer or main memory address location through the SI (serial input) pin. All instructions, addresses, and data are transferred with the most significant bit (MSB) first.

Read

By specifying the appropriate opcode, data can be read from the main memory or from either one of the two data buffers.

MAIN MEMORY PAGE READ: A main memory read allows the user to read data directly from any one of the 4096 pages in the main memory, bypassing both of the data buffers and leaving the contents of the buffers unchanged. To start a page read, the 8-bit opcode, 52H, is followed by 24 address bits and 32 don't care bits. In the AT45DB081, the first three address bits are reserved for larger density devices (see Notes on page 82), the next 12 address bits (PA11-PA0) specify the page address, and the next nine address bits (BA8-BA0) specify the starting byte address within the page. The 32 don't care bits which follow the 24 address bits are sent to initialize the read operation. Following the 32 don't care bits, additional pulses on SCK result in serial data being output on the SO (serial output) pin. The $\overline{CS}$ pin must remain low during the loading of the opcode, the address bits, and the reading of data. When the end of a page in main memory is reached during a main memory page read, the device will continue reading at the beginning of the same page. A low to high transition on the $\overline{CS}$ pin will terminate the read operation and tri-state the SO pin.

BUFFER READ: Data can be read from either one of the two buffers, using different opcodes to specify which buffer to read from. An opcode of 54H is used to read data from buffer 1, and an opcode of 56H is used to read data from buffer 2. To perform a buffer read, the eight bits of the

opcode must be followed by 15 don't care bits, nine address bits, and eight don't care bits. Since the buffer size is 264-bytes, nine address bits (BFA8-BFA0) are required to specify the first byte of data to be read from the buffer. The $\overline{CS}$ pin must remain low during the loading of the opcode, the address bits, the don't care bits, and the reading of data. When the end of a buffer is reached, the device will continue reading back at the beginning of the buffer. A low to high transition on the $\overline{CS}$ pin will terminate the read operation and tri-state the SO pin.

MAIN MEMORY PAGE TO BUFFER TRANSFER: A page of data can be transferred from the main memory to either buffer 1 or buffer 2. An 8-bit opcode, 53H for buffer 1 and 55H for buffer 2, is followed by the three reserved bits, 12 address bits (PA11-PA0) which specify the page in main memory that is to be transferred, and nine don't care bits. The $\overline{CS}$ pin must be low while toggling the SCK pin to load the opcode, the address bits, and the don't care bits from the SI pin. The transfer of the page of data from the main memory to the buffer will begin when the $\overline{CS}$ pin transitions from a low to a high state. During the transfer of a page of data (t_{XFR}), the status register can be read to determine whether the transfer has been completed or not.

MAIN MEMORY PAGE TO BUFFER COMPARE: A page of data in main memory can be compared to the data in buffer 1 or buffer 2. An 8-bit opcode, 60H for buffer 1 and 61H for buffer 2, is followed by 24 address bits consisting of the three reserved bits, 12 address bits (PA11-PA0) which specify the page in the main memory that is to be compared to the buffer, and nine don't care bits. The loading of the opcode and the address bits is the same as described previously. The $\overline{CS}$ pin must be low while toggling the SCK pin to load the opcode, the address bits, and the don't care bits from the SI pin. On the low to high transition of the $\overline{CS}$ pin, the 264 bytes in the selected main memory page will be compared with the 264 bytes in buffer 1 or buffer 2. During this time (t_{XFR}), the status register will indicate that the part is busy. On completion of the compare operation, bit 6 of the status register is updated with the result of the compare.

Program

BUFFER WRITE: Data can be shifted in from the SI pin into either buffer 1 or buffer 2. To load data into either buffer, an 8-bit opcode, 84H for buffer 1 or 87H for buffer 2, is followed by 15 don't care bits and nine address bits (BFA8-BFA0). The nine address bits specify the first byte in the buffer to be written. The data is entered following the address bits. If the end of the data buffer is reached, the device will wrap around back to the beginning of the buffer. Data will continue to be loaded into the buffer until a low to high transition is detected on the $\overline{CS}$ pin.

BUFFER TO MAIN MEMORY PAGE PROGRAM WITH BUILT-IN ERASE: Data written into either buffer 1 or buffer 2 can be programmed into the main memory. An 8-bit opcode, 83H for buffer 1 or 86H for buffer 2, is followed by the three reserved bits, 12 address bits (PA11-PA0) that specify the page in the main memory to be written, and nine additional don't care bits. When a low to high transition occurs on the $\overline{CS}$ pin, the part will first erase the selected page in main memory to all 1s and then program the data stored in the buffer into the specified page in the main memory. Both the erase and the programming of the page are internally self timed and should take place in a maximum time of t_{EP}. During this time, the status register will indicate that the part is busy.

BUFFER TO MAIN MEMORY PAGE PROGRAM WITHOUT BUILT-IN ERASE: A previously erased page within main memory can be programmed with the contents of either buffer 1 or buffer 2. An 8-bit opcode, 88H for buffer 1 or 89H for buffer 2, is followed by the three reserved bits, 12 address bits (PA11-PA0) that specify the page in the main memory to be written, and nine additional don't care bits. When a low to high transition occurs on the $\overline{CS}$ pin, the part will program the data stored in the buffer into the specified page in the main memory. It is necessary that the page in main memory that is being programmed has been previously programmed to all 1s (erased state). The programming of the page is internally self timed and should take place in a maximum time of t_P. During this time, the status register will indicate that the part is busy.

MAIN MEMORY PAGE PROGRAM: This operation is a combination of the Buffer Write and Buffer to Main Memory Page Program with Built-In Erase operations. Data is first shifted into buffer 1 or buffer 2 from the SI pin and then programmed into a specified page in the main memory. An 8-bit opcode, 82H for buffer 1 or 85H for buffer 2, is followed by the three reserved bits and 21 address bits. The 12 most significant address bits (PA11-PA0) select the page in the main memory where data is to be written, and the next nine address bits (BFA8-BFA0) select the first byte in the buffer to be written. After all address bits are shifted in, the part will take data from the SI pin and store it in one of the data buffers. If the end of the buffer is reached, the device will wrap around back to the beginning of the buffer. When there is a low to high transition on the $\overline{CS}$ pin, the part will first erase the selected page in main memory to all 1s and then program the data stored in the buffer into the specified page in the main memory. Both the erase and the programming of the page are internally self timed and should take place in a maximum of time t_{EP}. During this time, the status register will indicate that the part is busy.

AUTO PAGE REWRITE: This mode is only needed if multiple bytes within a page or multiple pages of data are modified in a random fashion. This mode is a combination of two operations: Main Memory Page to Buffer Transfer and

Buffer to Main Memory Page Program with Built-In Erase. A page of data is first transferred from the main memory to buffer 1 or buffer 2, and then the same data (from buffer 1 or buffer 2) is programmed back into its original page of main memory. An 8-bit opcode, 58H for buffer 1 or 59H for buffer 2, is followed by the three reserved bits, 12 address bits (PA11-PA0) that specify the page in main memory to be rewritten, and nine additional don't care bits. When a low to high transition occurs on the $\overline{CS}$ pin, the part will first transfer data from the page in main memory to a buffer and then program the data from the buffer back into same page of main memory. The operation is internally self-timed and should take place in a maximum time of t_{EP}. During this time, the status register will indicate that the part is busy.

If the main memory is programmed or reprogrammed sequentially page by page, then the programming algorithm shown in Figure 1 is recommended. Otherwise, if multiple bytes in a page or several pages are programmed randomly in the main memory, then the programming algorithm shown in Figure 2 is recommended.

STATUS REGISTER: The status register can be used to determine the device's ready/busy status, the result of a Main Memory Page to Buffer Compare operation, or the device density. To read the status register, an opcode of 57H must be loaded into the device. After the last bit of the opcode is shifted in, the eight bits of the status register, starting with the MSB (bit 7), will be shifted out on the SO pin during the next eight clock cycles. The five most-significant bits of the status register will contain device information, while the remaining three least-significant bits are reserved for future use and will have undefined values. After bit 0 of the status register has been shifted out, the sequence will repeat itself (as long as $\overline{CS}$ remains low and SCK is being toggled) starting again with bit 7. The data in the status register is constantly updated, so each repeating sequence will output new data.

Ready/busy status is indicated using bit 7 of the status register. If bit 7 is a 1, then the device is not busy and is ready to accept the next command. If bit 7 is a 0, then the device is in a busy state. The user can continuously poll bit 7 of the status register by stopping SCK once bit 7 has been output. The status of bit 7 will continue to be output on the SO pin, and once the device is no longer busy, the state of SO will change from 0 to 1. There are six operations which can cause the device to be in a busy state: Main Memory Page to Buffer Transfer, Main Memory Page to Buffer Compare, Buffer to Main Memory Page Program with Built-In Erase, Buffer to Main Memory Page Program without Built-In Erase, Main Memory Page Program, and Auto Page Rewrite.

The result of the most recent Main Memory Page to Buffer Compare operation is indicated using bit 6 of the status register. If bit 6 is a 0, then the data in the main memory page matches the data in the buffer. If bit 6 is a 1, then at least one bit of the data in the main memory page does not match the data in the buffer.

The device density is indicated using bits 5, 4, and 3 of the status register. For the AT45DB081, the three bits are 1, 0, and 0. The decimal value of these three binary bits does not equate to the device density; the three bits represent a combinational code relating to differing densities of Serial DataFlash devices, allowing a total of eight different density configurations.

Read/Program Mode Summary

The modes listed above can be separated into two groups — modes which make use of the flash memory array (Group A) and modes which do not make use of the flash memory array (Group B).

Group A modes consist of:

1. Main memory page read
2. Main memory page to buffer 1 (or 2) transfer
3. Main memory page to buffer 1 (or 2) compare
4. Buffer 1 (or 2) to main memory page program with built-in erase
5. Buffer 1 (or 2) to main memory page program without built-in erase
6. Main memory page program
7. Auto page rewrite

Group B modes consist of:

1. Buffer 1 (or 2) read
2. Buffer 1 (or 2) write
3. Status read

If a Group A mode is in progress (not fully completed) then another mode in Group A should not be started. However, during this time in which a Group A mode is in progress, modes in Group B can be started.

This gives the Serial DataFlash the ability to virtually accommodate a continuous data stream. While data is being programmed into main memory from buffer 1, data can be loaded into buffer 2 (or vice versa). See application note AN-4 ("Using Atmel's Serial DataFlash") for more details.

Status Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RDY/$\overline{BUSY}$	COMP	1	0	0	X	X	X

HARDWARE PAGE WRITE PROTECT: If the $\overline{WP}$ pin is held low, the first 256 pages of the main memory cannot be reprogrammed. The only way to reprogram the first 256 pages is to first drive the protect pin high and then use the program commands previously mentioned. The $\overline{WP}$ pin is internally pulled high; therefore, connection of the $\overline{WP}$ pin is not necessary if this pin and feature will not be utilized. However, it is recommended that the $\overline{WP}$ pin be driven high externally whenever possible.

$\overline{RESET}$: A low state on the reset pin ($\overline{RESET}$) will terminate the operation in progress and reset the internal state machine to an idle state. The device will remain in the reset condition as long as a low level is present on the $\overline{RESET}$ pin. Normal operation can resume once the $\overline{RESET}$ pin is brought back to a high level.

The device also incorporates an internal power-on reset circuit, so there are no restrictions on the $\overline{RESET}$ pin during power-on sequences. The $\overline{RESET}$ pin is also internally pulled high; therefore, connection of the $\overline{RESET}$ pin is not necessary if this pin and feature will not be utilized. However, it is recommended that the $\overline{RESET}$ pin be driven high externally whenever possible.

READY/$\overline{BUSY}$: This open drain output pin will be driven low when the device is busy in an internally self-timed operation. This pin, which is normally in a high state (through an external pull-up resistor), will be pulled low during programming operations, compare operations, and during page-to-buffer transfers.

The busy status indicates that the Flash memory array and one of the buffers cannot be accessed; read and write operations to the other buffer can still be performed.

Power On/Reset State

When power is first applied to the device, or when recovering from a reset condition, the device will default to SPI mode 3. In addition, the SO pin will be in a high imipedance state, and a high to low transition on the $\overline{CS}$ pin will be required to start a valid instruction. The SPI mode will be automatically selected on every falling edge of the $\overline{CS}$ by sampling the inactive clock state.

4

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC and AC Operating Range

		AT45DB081
Operating Temperature (Case)	Com.	0°C to 70°C
	Ind.	-40°C to 85°C
V_{CC} Power Supply[1]		2.7V to 3.6V

Note: 1. After power is applied and V_{CC} is at the minimum specified data sheet value, the system should wait 20 ms before an operational mode is started.

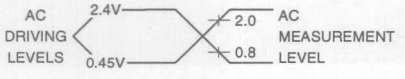
DC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{SB}	Standby Current	$\overline{CS}$, $\overline{RESET}$, $\overline{WP}$ = V_{IH}, all inputs at CMOS levels		2	10	µA
I_{CC1}	Active Current, Read Operation	f = 10 MHz; I_{OUT} = 0 mA; V_{CC} = 3.6V		4	10	mA
I_{CC2}	Active Current, Program/Erase Operation	V_{CC} = 3.6V		15	35	mA
I_{LI}	Input Load Current	V_{IN} = CMOS levels			1	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = CMOS levels			1	µA
V_{IL}	Input Low Voltage				0.6	V
V_{IH}	Input High Voltage		2.0			V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA; V_{CC} = 2.7V			0.4	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA	V_{CC} - 0.2V			V

AC Characteristics

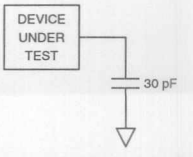
Symbol	Parameter	Min	Typ	Max	Units
f_{SCK}	SCK Frequency			10	MHz
t_{WH}	SCK High Time	40			ns
t_{WL}	SCK Low Time	40			ns
t_{CS}	Minimum $\overline{CS}$ High Time	250			ns
t_{CSS}	$\overline{CS}$ Setup Time	250			ns
t_{CSH}	$\overline{CS}$ Hold Time	250			ns
t_{CSB}	$\overline{CS}$ High to RDY/$\overline{BUSY}$ Low			200	ns
t_{SU}	Data In Setup Time	10			ns
t_H	Data In Hold Time	25			ns
t_{HO}	Output Hold Time	0			ns
t_{DIS}	Output Disable Time			75	ns
t_V	Output Valid			80	ns
t_{XFR}	Page to Buffer Transfer/Compare Time		120	200	µs
t_{EP}	Page Erase and Programming Time		10	20	ms
t_P	Page Programming Time		7	14	ms
t_{RST}	$\overline{RESET}$ Pulse Width	10			µs
t_{REC}	$\overline{RESET}$ Recovery Time			1	µs

Input Test Waveforms and Measurement Levels



t_R, t_F < 20 ns (10% to 90%)

Output Test Load

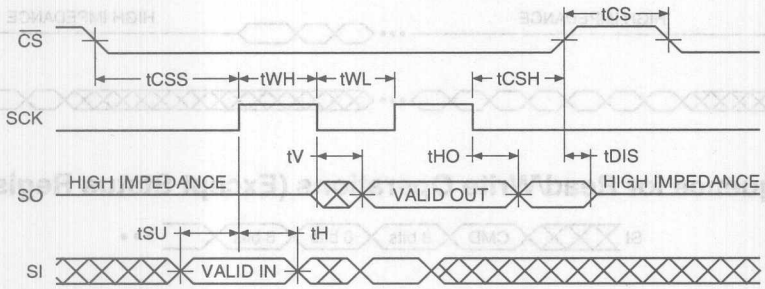


AC Waveforms

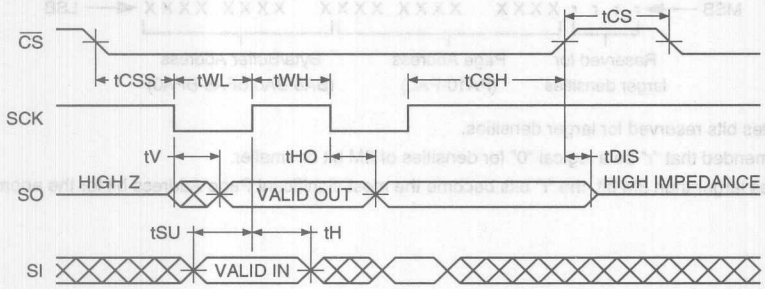
Two different timing diagrams are shown below. Waveform 1 shows the SCK signal being low when $\overline{CS}$ makes a high-to-low transition, and Waveform 2 shows the SCK signal being high when $\overline{CS}$ makes a high-to-low transition. Both waveforms show valid timing diagrams. The setup and hold times for the SI signal are referenced to the low-to-high transition on the SCK signal.

Waveform 1 shows timing that is also compatible with SPI Mode 0, and Waveform 2 shows timing that is compatible with SPI Mode 3.

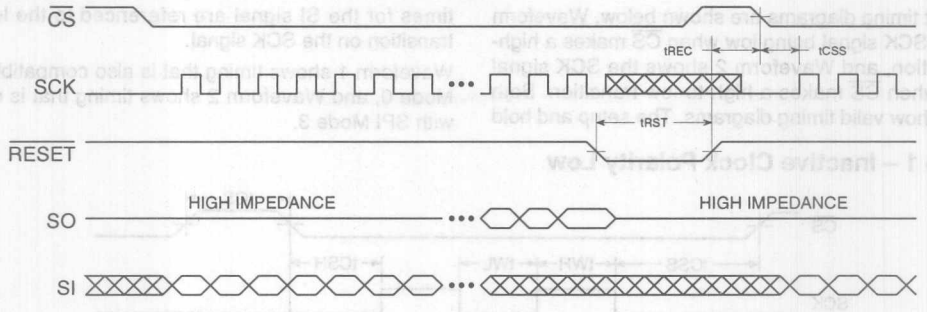
Waveform 1 – Inactive Clock Polarity Low



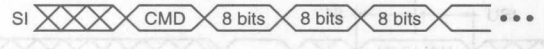
Waveform 2 – Inactive Clock Polarity High

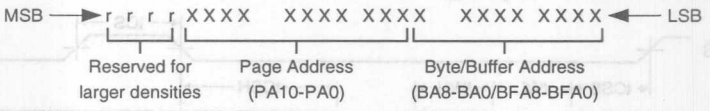


Reset Timing (Inactive Clock Polarity Low Shown)



Command Sequence for Read/Write Operations (Except Status Register Read)

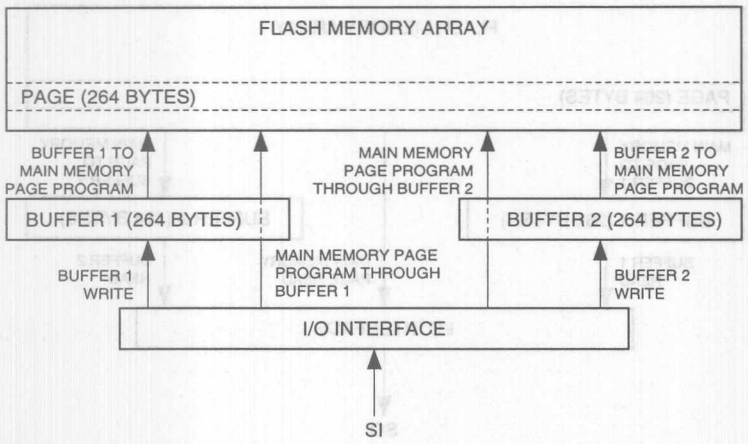




Notes:
1. "r" designates bits reserved for larger densities.
2. It is recommended that "r" be a logical "0" for densities of 8M bit or smaller.
3. For densities larger than 8M bit, the "r" bits become the most significant Page Address bit for the appropriate density.

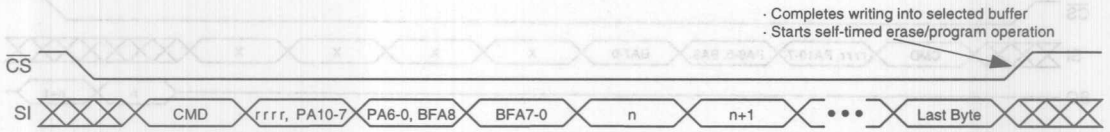
Write Operations

The following block diagram and waveforms illustrate the various write sequences available.

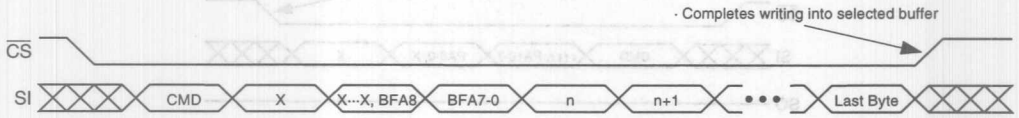


4

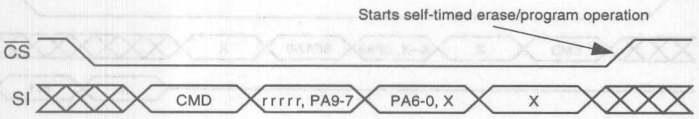
Main Memory Page Program through Buffers



Buffer Write



Buffer to Main Memory Page Program (Data from Buffer Programmed into Flash Page)

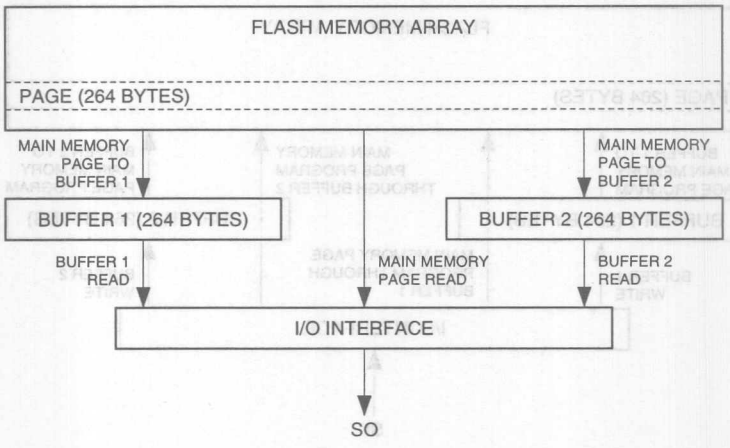


Each transition represents 8 bits and 8 clock cycles

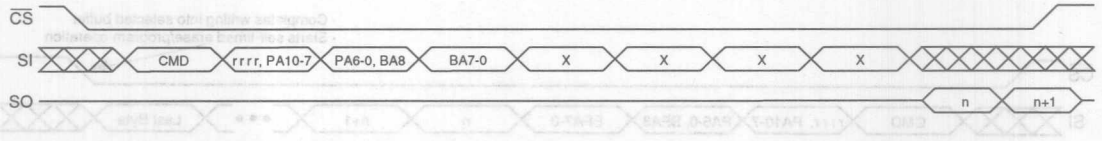
n = 1st byte read
n+1 = 2nd byte read

Read Operations

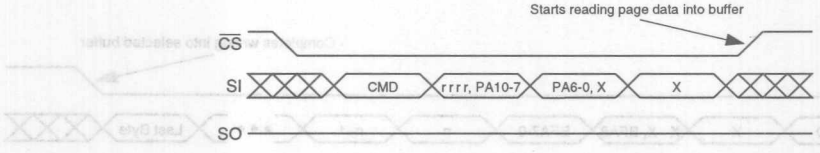
The following block diagram and waveforms illustrate the various read sequences available.



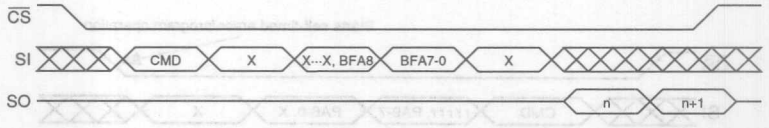
Main Memory Page Read



Main Memory Page to Buffer Transfer (Data from Flash Page Read into Buffer)



Buffer Read

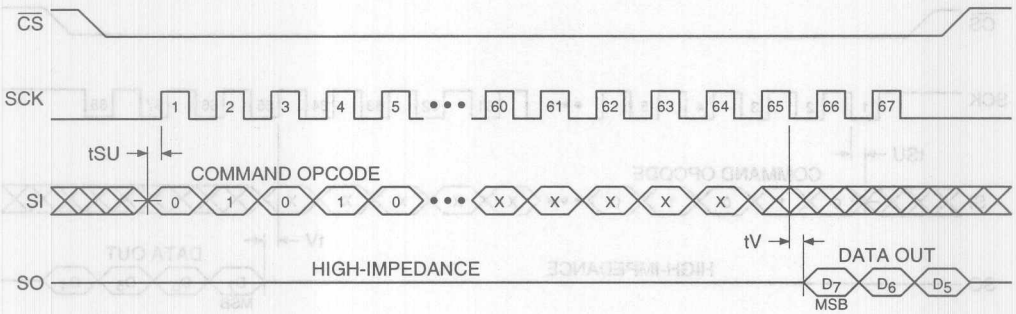


Each transition represents 8 bits and 8 clock cycles

n = 1st byte read
n+1 = 2nd byte read

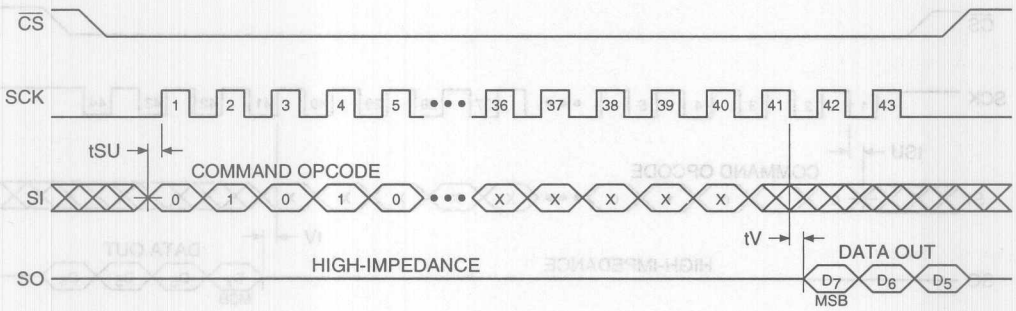
Detailed Bit-Level Read Timing – Inactive Clock Polarity Low

Main Memory Page Read

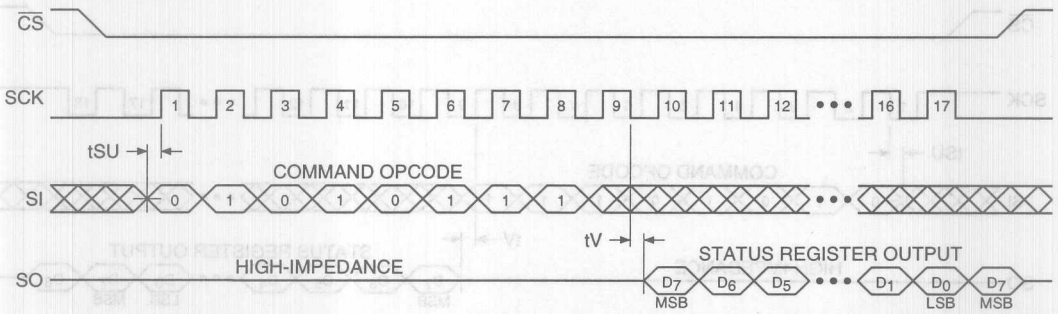


4

Buffer Read

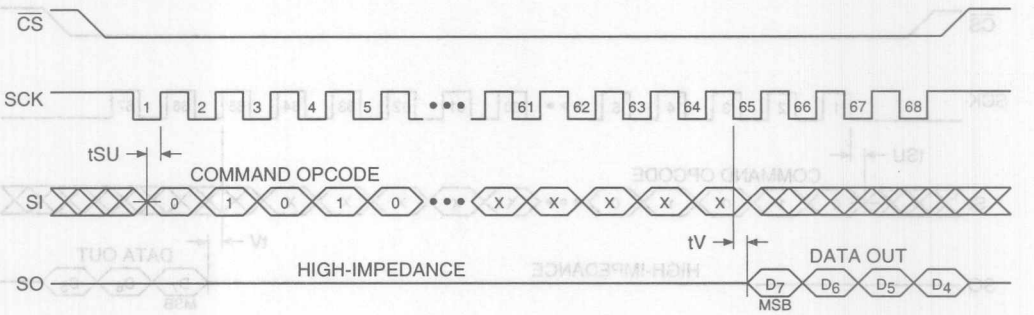


Status Register Read

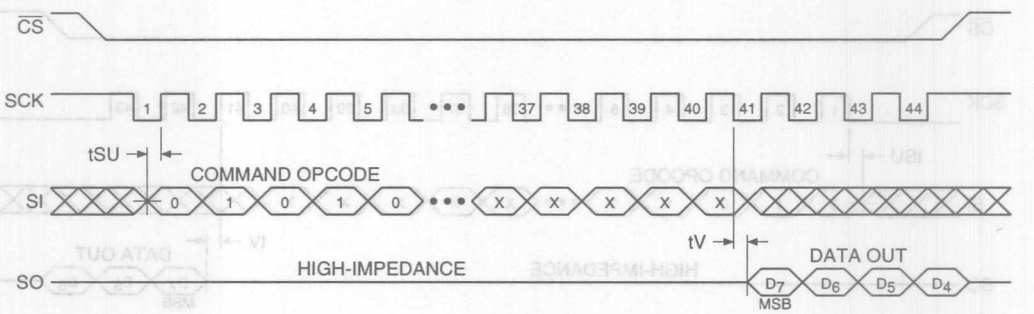


Detailed Bit-Level Read Timing – Inactive Clock Polarity High

Main Memory Page Read



Buffer Read



Status Register Read

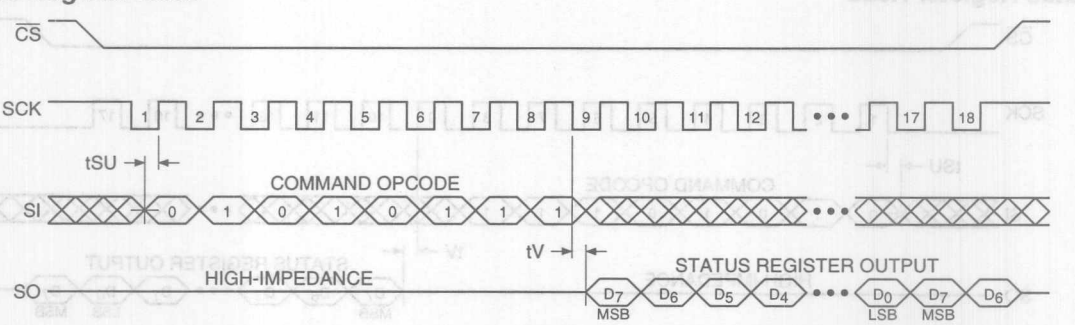


Table 1.

Main Memory Page Read	Buffer 1 Read	Buffer 2 Read	Main Memory Page to Buffer 1 Transfer	Main Memory Page to Buffer 2 Transfer	Main Memory Page to Buffer 1 Compare	Main Memory Page to Buffer 2 Compare	Buffer 1 Write	Buffer 2 Write
				Opcode				
52H	54H	56H	53H	55H	60H	61H	84H	87H
0	0	0	0	0	0	0	1	1
1	1	1	1	1	1	1	0	0
0	0	0	0	0	1	1	0	0
1	1	1	1	1	0	0	0	0
0	0	0	0	0	0	0	0	0
0	1	1	0	1	0	0	1	1
1	0	1	1	0	0	0	0	1
0	0	0	1	1	0	1	0	1
r	X	X	r	r	r	r	X	X
r	X	X	r	r	r	r	X	X
r	X	X	r	r	r	r	X	X
PA11	X	X	PA11	PA11	PA11	PA11	X	X
PA10	X	X	PA10	PA10	PA10	PA10	X	X
PA9	X	X	PA9	PA9	PA9	PA9	X	X
PA8	X	X	PA8	PA8	PA8	PA8	X	X
PA7	X	X	PA7	PA7	PA7	PA7	X	X
PA6	X	X	PA6	PA6	PA6	PA6	X	X
PA5	X	X	PA5	PA5	PA5	PA5	X	X
PA4	X	X	PA4	PA4	PA4	PA4	X	X
PA3	X	X	PA3	PA3	PA3	PA3	X	X
PA2	X	X	PA2	PA2	PA2	PA2	X	X
PA1	X	X	PA1	PA1	PA1	PA1	X	X
PA0	X	X	PA0	PA0	PA0	PA0	X	X
BA8	BFA8	BFA8	X	X	X	X	BFA8	BFA8
BA7	BFA7	BFA7	X	X	X	X	BFA7	BFA7
BA6	BFA6	BFA6	X	X	X	X	BFA6	BFA6
BA5	BFA5	BFA5	X	X	X	X	BFA5	BFA5
BA4	BFA4	BFA4	X	X	X	X	BFA4	BFA4
BA3	BFA3	BFA3	X	X	X	X	BFA3	BFA3
BA2	BFA2	BFA2	X	X	X	X	BFA2	BFA2
BA1	BFA1	BFA1	X	X	X	X	BFA1	BFA1
BA0	BFA0	BFA0	X	X	X	X	BFA0	BFA0
X	X	X						
X	X	X						
X	X	X						
X	X	X						
X	X	X						
X	X	X						
X	X	X						
X	X	X						
•								
•								
•								
X (64th bit)								

X (Don't Care)
r (reserved bits)

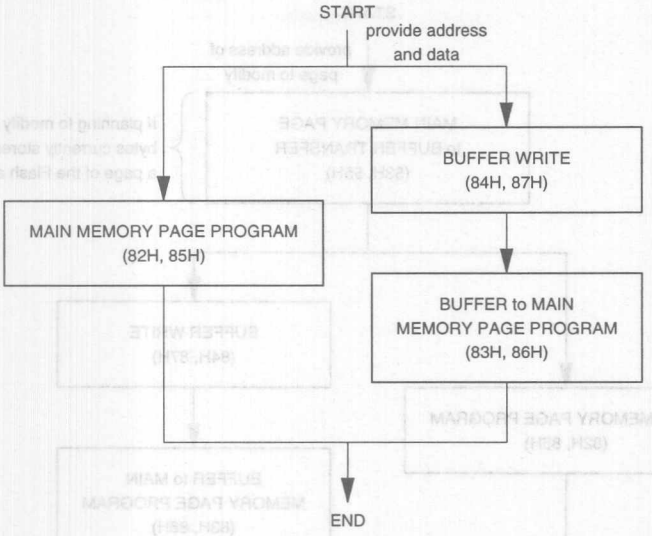
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Table 1.

Buffer 1 to Main Memory Page Program with Built-In Erase	Buffer 2 to Main Memory Page Program with Built-In Erase	Buffer 1 to Main Memory Page Program without Built-In Erase	Buffer 2 to Main Memory Page Program without Built-In Erase	Main Memory Page Program Through Buffer 1	Main Memory Page Program Through Buffer 2	Auto Page Rewrite Through Buffer 1	Auto Page Rewrite Through Buffer 2	Status Register
Opcode								
83H	86H	88H	89H	82H	85H	58H	59H	57H
1	1	1	1	1	1	0	0	0
0	0	0	0	0	0	1	1	1
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1	1
0	0	1	1	0	0	1	1	0
0	1	0	0	0	1	0	0	1
1	1	0	0	1	0	0	0	1
1	0	0	1	0	1	0	1	1
r	r	r	r	r	r	r	r	
r	r	r	r	r	r	r	r	
r	r	r	r	r	r	r	r	
PA11	PA11	PA11	PA11	PA11	PA11	PA11	PA11	
PA10	PA10	PA10	PA10	PA10	PA10	PA10	PA10	
PA9	PA9	PA9	PA9	PA9	PA9	PA9	PA9	
PA8	PA8	PA8	PA8	PA8	PA8	PA8	PA8	
PA7	PA7	PA7	PA7	PA7	PA7	PA7	PA7	
PA6	PA6	PA6	PA6	PA6	PA6	PA6	PA6	
PA5	PA5	PA5	PA5	PA5	PA5	PA5	PA5	
PA4	PA4	PA4	PA4	PA4	PA4	PA4	PA4	
PA3	PA3	PA3	PA3	PA3	PA3	PA3	PA3	
PA2	PA2	PA2	PA2	PA2	PA2	PA2	PA2	
PA1	PA1	PA1	PA1	PA1	PA1	PA1	PA1	
PA0	PA0	PA0	PA0	PA0	PA0	PA0	PA0	
X	X	X	X	BA8	BA8	X	X	
X	X	X	X	BA7	BA7	X	X	
X	X	X	X	BA6	BA6	X	X	
X	X	X	X	BA5	BA5	X	X	
X	X	X	X	BA4	BA4	X	X	
X	X	X	X	BA3	BA3	X	X	
X	X	X	X	BA2	BA2	X	X	
X	X	X	X	BA1	BA1	X	X	
X	X	X	X	BA0	BA0	X	X	

X (Don't Care)
r (reserved bits)

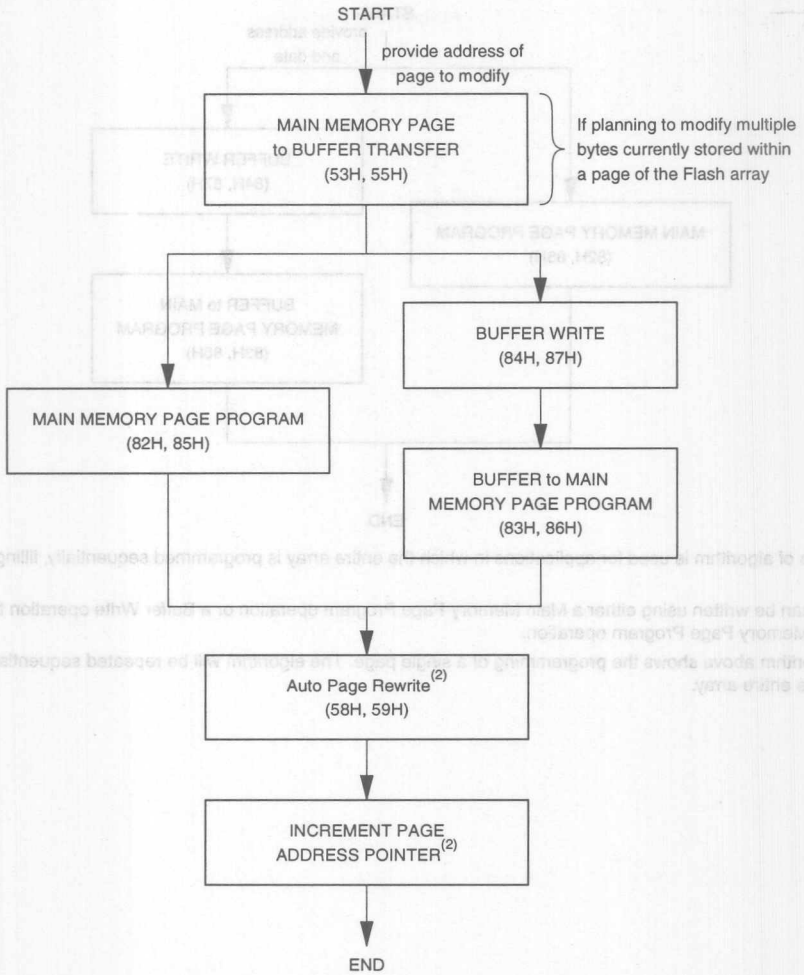
Figure 1. Algorithm for Programming or Reprogramming of the Entire Array Sequentially



Notes:
1. This type of algorithm is used for applications in which the entire array is programmed sequentially, filling the array page-by-page.
2. A page can be written using either a Main Memory Page Program operation or a Buffer Write operation followed by a Buffer to Main Memory Page Program operation.
3. The algorithm above shows the programming of a single page. The algorithm will be repeated sequentially for each page within the entire array.

4

Figure 2. Algorithm for Randomly Modifying Data



Notes:
1. To preserve data integrity, each page of the DataFlash memory array must be updated/rewritten at least once within every 10,000 cumulative page erase/program operations.
2. A Page Address Pointer must be maintained to indicate which page is to be rewritten. The Auto Page Rewrite command must use the address specified by the Page Address Pointer.
3. Other algorithms can be used to rewrite portions of the Flash array. Low power applications may choose to wait until 10,000 cumulative page erase/program operations have accumulated before rewriting all pages of the Flash array. See application note AN-4 ("Using Atmel's Serial DataFlash") for more details.

Ordering Information

f_{SCK} (MHz)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
10	10	0.01	AT45DB081-RC AT45DB081-TC	28R 32T	Commercial (0°C to 70°C)
10	10	0.01	AT45DB081-RI AT45DB081-TI	28R 32T	Industrial (-40°C to 85°C)

4

Package Type	
28R	28-Lead, 0.330" Wide, Plastic Gull-Wing Small Outline Package (SOIC)
32T	32-Lead, Plastic Thin Small Outline Package (TSOP)

Ordering Information

f_{SCK} (MHz)	I_{CC} (mA) Active	I_{CC} (mA) Standby	Ordering Code	Package	Operation Range
10	10	0.01	AT45DB081-RC AT45DB081-TC	28R 32T	Commercial (0°C to 70°C)
10	10	0.01	AT45DB081-RI AT45DB081-TI	28R 32T	Industrial (-40°C to 85°C)

Package	Package Type
28R	28-Lead, 0.330" Wide, Plastic Gull-Wing Small Outline Package (SOIC)
32T	32-Lead, Plastic Thin Small Outline Package (TSOP)

Features

- Single 2.7V - 3.6V Supply
- Serial Interface Architecture
- Page Program Operation
  - Single Cycle Reprogram (Erase and Program)
  - 4096 Pages (528 Bytes/Page) Main Memory
- Optional Page and Block Erase Operations
- Two 528-Byte SRAM Data Buffers – Allows Receiving of Data while Reprogramming of Nonvolatile Memory
- Internal Program and Control Timer
- Fast Page Program Time – 7 ms Typical
- 120 µs Typical Page to Buffer Transfer Time
- Low Power Dissipation
  - 4 mA Active Read Current Typical
  - 3 µA CMOS Standby Current Typical
- 13 MHz Max Clock Frequency
- Hardware Data Protection Feature
- Serial Peripheral Interface (SPI) Compatible – Modes 0 and 3
- CMOS and TTL Compatible Inputs and Outputs
- Commercial and Industrial Temperature Ranges

Description

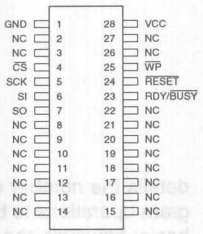
The AT45DB161 is a 2.7-volt only, serial interface Flash memory suitable for in-system reprogramming. Its 17,301,504 bits of memory are organized as 4096 pages of 528 bytes each. In addition to the main memory, the AT45DB161 also contains two SRAM data buffers of 528 bytes each. The buffers allow receiving of data while a page in the main memory is being reprogrammed. Unlike conventional Flash memo-

(continued)

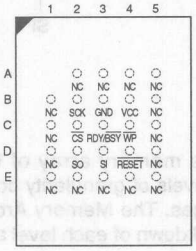
Pin Configurations

Pin Name	Function
$\overline{CS}$	Chip Select
SCK	Serial Clock
SI	Serial Input
SO	Serial Output
$\overline{WP}$	Hardware Page Write Protect Pin
$\overline{RESET}$	Chip Reset
RDY/$\overline{BUSY}$	Ready/Busy

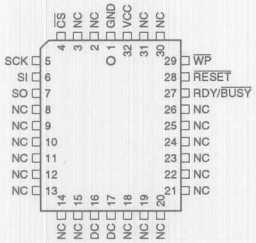
SOIC



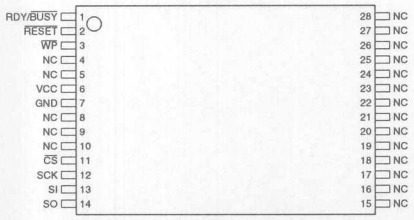
CBGA Top View Through Package



PLCC



TSOP Top View
Type 1



Note: PLCC package pins 16 and 17 are DON'T CONNECT

16-Megabit 2.7-volt Only Serial DataFlash®

4

AT45DB161 Preliminary

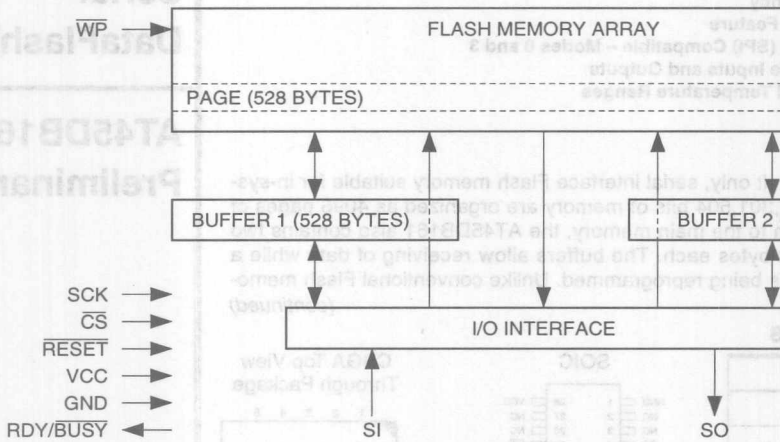
Rev. 0807C–07/98

ries that are accessed randomly with multiple address lines and a parallel interface, the DataFlash uses a serial interface to sequentially access its data. The simple serial interface facilitates hardware layout, increases system reliability, minimizes switching noise, and reduces package size and active pin count. The device is optimized for use in many commercial and industrial applications where high density, low pin count, low voltage, and low power are essential. Typical applications for the DataFlash are digital voice storage, image storage, and data storage. The device operates at clock frequencies up to 13 MHz with a typical active read current consumption of 4 mA.

To allow for simple in-system reprogrammability, the AT45DB161 does not require high input voltages for programming. The device operates from a single power supply, 2.7V to 3.6V, for both the program and read operations. The AT45DB161 is enabled through the chip select pin ($\overline{CS}$) and accessed via a three-wire interface consisting of the Serial Input (SI), Serial Output (SO), and the Serial Clock (SCK).

All programming cycles are self-timed, and no separate erase cycle is required before programming.

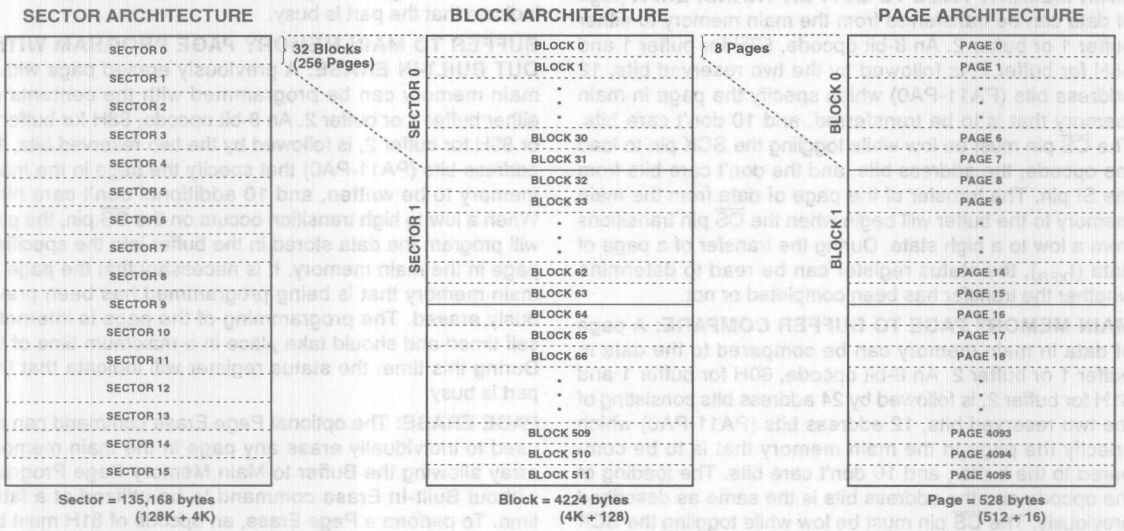
Block Diagram



Memory Array

To provide optimal flexibility, the memory array of the AT45DB161 is divided into three levels of granularity comprising of sectors, blocks, and pages. The Memory Architecture Diagram illustrates the breakdown of each level and details the number of pages per sector and block. All program operations to the DataFlash occur on a page by page basis; however, the optional erase operations can be performed at the block or page level.

Memory Architecture Diagram



Device Operation

The device operation is controlled by instructions from the host processor. The list of instructions and their associated opcodes are contained in Table 1 and Table 2. A valid instruction starts with the falling edge of $\overline{CS}$ followed by the appropriate 8-bit opcode and the desired buffer or main memory address location. While the $\overline{CS}$ pin is low, toggling the SCK pin controls the loading of the opcode and the desired buffer or main memory address location through the SI (serial input) pin. All instructions, addresses, and data are transferred with the most significant bit (MSB) first.

Read

By specifying the appropriate opcode, data can be read from the main memory or from either one of the two data buffers.

MAIN MEMORY PAGE READ: A main memory read allows the user to read data directly from any one of the 4096 pages in the main memory, bypassing both of the data buffers and leaving the contents of the buffers unchanged. To start a page read, the 8-bit opcode, 52H, is followed by 24 address bits and 32 don't care bits. In the AT45DB161, the first two address bits are reserved for larger density devices (see Notes on page 102), the next 12 address bits (PA11-PA0) specify the page address, and the next 10 address bits (BA9-BA0) specify the starting byte address within the page. The 32 don't care bits which follow the 24 address bits are sent to initialize the read operation. Following the 32 don't care bits, additional pulses on SCK result in serial data being output on the SO (serial output) pin. The $\overline{CS}$ pin must remain low during the loading of the opcode, the address bits, and the reading of data. When the end of a page in main memory is reached during a main memory page read, the device will continue reading at the beginning of the same page. A low to high transition on the $\overline{CS}$ pin will terminate the read operation and tri-state the SO pin.

BUFFER READ: Data can be read from either one of the two buffers, using different opcodes to specify which buffer to read from. An opcode of 54H is used to read data from buffer 1, and an opcode of 56H is used to read data from buffer 2. To perform a buffer read, the eight bits of the opcode must be followed by 14 don't care bits, 10 address bits, and eight don't care bits. Since the buffer size is 528-bytes, 10 address bits (BFA9-BFA0) are required to specify the first byte of data to be read from the buffer. The $\overline{CS}$ pin must remain low during the loading of the opcode, the address bits, the don't care bits, and the reading of data. When the end of a buffer is reached, the device will continue reading back at the beginning of the buffer. A low to

high transition on the $\overline{CS}$ pin will terminate the read operation and tri-state the SO pin.

MAIN MEMORY PAGE TO BUFFER TRANSFER: A page of data can be transferred from the main memory to either buffer 1 or buffer 2. An 8-bit opcode, 53H for buffer 1 and 55H for buffer 2, is followed by the two reserved bits, 12 address bits (PA11-PA0) which specify the page in main memory that is to be transferred, and 10 don't care bits. The $\overline{CS}$ pin must be low while toggling the SCK pin to load the opcode, the address bits, and the don't care bits from the SI pin. The transfer of the page of data from the main memory to the buffer will begin when the $\overline{CS}$ pin transitions from a low to a high state. During the transfer of a page of data (t_{XFR}), the status register can be read to determine whether the transfer has been completed or not.

MAIN MEMORY PAGE TO BUFFER COMPARE: A page of data in main memory can be compared to the data in buffer 1 or buffer 2. An 8-bit opcode, 60H for buffer 1 and 61H for buffer 2, is followed by 24 address bits consisting of the two reserved bits, 12 address bits (PA11-PA0) which specify the page in the main memory that is to be compared to the buffer, and 10 don't care bits. The loading of the opcode and the address bits is the same as described previously. The $\overline{CS}$ pin must be low while toggling the SCK pin to load the opcode, the address bits, and the don't care bits from the SI pin. On the low to high transition of the $\overline{CS}$ pin, the 528 bytes in the selected main memory page will be compared with the 528 bytes in buffer 1 or buffer 2. During this time (t_{XFR}), the status register will indicate that the part is busy. On completion of the compare operation, bit 6 of the status register is updated with the result of the compare.

Program

BUFFER WRITE: Data can be shifted in from the SI pin into either buffer 1 or buffer 2. To load data into either buffer, an 8-bit opcode, 84H for buffer 1 or 87H for buffer 2, is followed by 14 don't care bits and 10 address bits (BFA9-BFA0). The 10 address bits specify the first byte in the buffer to be written. The data is entered following the address bits. If the end of the data buffer is reached, the device will wrap around back to the beginning of the buffer. Data will continue to be loaded into the buffer until a low to high transition is detected on the $\overline{CS}$ pin.

BUFFER TO MAIN MEMORY PAGE PROGRAM WITH BUILT-IN ERASE: Data written into either buffer 1 or buffer 2 can be programmed into the main memory. An 8-bit opcode, 83H for buffer 1 or 86H for buffer 2, is followed by the two reserved bits, 12 address bits (PA11-PA0) that specify the page in the main memory to be written, and 10 additional don't care bits. When a low to high transition occurs on the $\overline{CS}$ pin, the part will first erase the selected page in main memory to all 1s and then program the data stored in the buffer into the specified page in the main memory. Both the erase and the programming of the page are internally self timed and should take place in a maximum time of t_{EP}. During this time, the status register will indicate that the part is busy.

BUFFER TO MAIN MEMORY PAGE PROGRAM WITHOUT BUILT-IN ERASE: A previously erased page within main memory can be programmed with the contents of either buffer 1 or buffer 2. An 8-bit opcode, 88H for buffer 1 or 89H for buffer 2, is followed by the two reserved bits, 12 address bits (PA11-PA0) that specify the page in the main memory to be written, and 10 additional don't care bits. When a low to high transition occurs on the $\overline{CS}$ pin, the part will program the data stored in the buffer into the specified page in the main memory. It is necessary that the page in main memory that is being programmed has been previously erased. The programming of the page is internally self timed and should take place in a maximum time of t_P. During this time, the status register will indicate that the part is busy.

PAGE ERASE: The optional Page Erase command can be used to individually erase any page in the main memory array allowing the Buffer to Main Memory Page Program without Built-In Erase command to be utilized at a later time. To perform a Page Erase, an opcode of 81H must be loaded into the device, followed by two reserved bits, 12 address bits (PA11-PA0), and 10 don't care bits. The 12 address bits are used to specify which page of the memory array is to be erased. When a low to high transition occurs on the $\overline{CS}$ pin, the part will erase the selected page to 1s. The erase operation is internally self-timed and should take place in a maximum time of t_{PE}. During this time, the status register will indicate that the part is busy.

BLOCK ERASE: A block of eight pages can be erased at one time allowing the Buffer to Main Memory Page Program without Built-In Erase command to be utilized to reduce programming times when writing large amounts of data to the device. To perform a Block Erase, an opcode of 50H must be loaded into the device, followed by two reserved bits, nine address bits (PA11-PA3), and 13 don't care bits. The nine address bits are used to specify which block of eight pages is to be erased. When a low to high transition occurs on the $\overline{CS}$ pin, the part will erase the selected block of eight pages to 1s. The erase operation is internally self-timed and should take place in a maximum time of t_{BE}. During this time, the status register will indicate that the part is busy.

Block Erase Addressing

PA11	PA10	PA9	PA8	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	Block
0	0	0	0	0	0	0	0	0	X	X	X	0
0	0	0	0	0	0	0	0	1	X	X	X	1
0	0	0	0	0	0	0	1	0	X	X	X	2
0	0	0	0	0	0	0	1	1	X	X	X	3
•	•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•	•
1	1	1	1	1	1	1	0	0	X	X	X	508
1	1	1	1	1	1	1	0	1	X	X	X	509
1	1	1	1	1	1	1	1	0	X	X	X	510
1	1	1	1	1	1	1	1	1	X	X	X	511

MAIN MEMORY PAGE PROGRAM: This operation is a combination of the Buffer Write and Buffer to Main Memory Page Program with Built-In Erase operations. Data is first shifted into buffer 1 or buffer 2 from the SI pin and then programmed into a specified page in the main memory. An 8-bit opcode, 82H for buffer 1 or 85H for buffer 2, is followed by the two reserved bits and 22 address bits. The 12 most significant address bits (PA11-PA0) select the page in the main memory where data is to be written, and the next 10 address bits (BFA9-BFA0) select the first byte in the buffer to be written. After all address bits are shifted in, the part will take data from the SI pin and store it in one of the data buffers. If the end of the buffer is reached, the device will wrap around back to the beginning of the buffer. When there is a low to high transition on the $\overline{CS}$ pin, the part will first erase the selected page in main memory to all 1s and then program the data stored in the buffer into the specified page in the main memory. Both the erase and the programming of the page are internally self timed and should take place in a maximum of time t_{EP}. During this time, the status register will indicate that the part is busy.

AUTO PAGE REWRITE: This mode is only needed if multiple bytes within a page or multiple pages of data are modified in a random fashion. This mode is a combination of two operations: Main Memory Page to Buffer Transfer and Buffer to Main Memory Page Program with Built-In Erase. A page of data is first transferred from the main memory to buffer 1 or buffer 2, and then the same data (from buffer 1 or buffer 2) is programmed back into its original page of main memory. An 8-bit opcode, 58H for buffer 1 or 59H for buffer 2, is followed by the two reserved bits, 12 address bits (PA11-PA0) that specify the page in main memory to be rewritten, and 10 additional don't care bits. When a low to high transition occurs on the $\overline{CS}$ pin, the part will first transfer data from the page in main memory to a buffer and then program the data from the buffer back into same page of main memory. The operation is internally self-timed and should take place in a maximum time of t_{EP}. During this time, the status register will indicate that the part is busy.

If a sector is programmed or reprogrammed sequentially page by page, then the programming algorithm shown in Figure 1 is recommended. Otherwise, if multiple bytes in a page or several pages are programmed randomly in a sector, then the programming algorithm shown in Figure 2 is recommended.

STATUS REGISTER: The status register can be used to determine the device's ready/busy status, the result of a Main Memory Page to Buffer Compare operation, or the device density. To read the status register, an opcode of 57H must be loaded into the device. After the last bit of the opcode is shifted in, the eight bits of the status register, starting with the MSB (bit 7), will be shifted out on the SO pin during the next eight clock cycles. The five most-significant bits of the status register will contain device information, while the remaining three least-significant bits are reserved for future use and will have undefined values. After bit 0 of the status register has been shifted out, the sequence will repeat itself (as long as $\overline{CS}$ remains low and SCK is being toggled) starting again with bit 7. The data in the status register is constantly updated, so each repeating sequence will output new data.

Ready/busy status is indicated using bit 7 of the status register. If bit 7 is a 1, then the device is not busy and is ready to accept the next command. If bit 7 is a 0, then the device is in a busy state. The user can continuously poll bit 7 of the status register by stopping SCK once bit 7 has been output. The status of bit 7 will continue to be output on the SO pin, and once the device is no longer busy, the state of SO will change from 0 to 1. There are eight operations which can

cause the device to be in a busy state: Main Memory Page to Buffer Transfer, Main Memory Page to Buffer Compare, Buffer to Main Memory Page Program with Built-In Erase, Buffer to Main Memory Page Program without Built-In Erase, Page Erase, Block Erase, Main Memory Page Program, and Auto Page Rewrite.

The result of the most recent Main Memory Page to Buffer Compare operation is indicated using bit 6 of the status register. If bit 6 is a 0, then the data in the main memory page matches the data in the buffer. If bit 6 is a 1, then at least one bit of the data in the main memory page does not match the data in the buffer.

The device density is indicated using bits 5, 4, and 3 of the status register. For the AT45DB161, the three bits are 1, 0, and 1. The decimal value of these three binary bits does not equate to the device density; the three bits represent a combinational code relating to differing densities of Serial DataFlash devices, allowing a total of eight different density configurations.

Read/Program Mode Summary

The modes listed above can be separated into two groups — modes which make use of the flash memory array (Group A) and modes which do not make use of the flash memory array (Group B).

Group A modes consist of:

1. Main Memory Page Read
2. Main Memory Page to Buffer 1 (or 2) Transfer
3. Main Memory Page to Buffer 1 (or 2) Compare
4. Buffer 1 (or 2) to Main Memory Page Program With Built-In Erase
5. Buffer 1 (or 2) to Main Memory Page Program Without Built-In Erase
6. Page Erase
7. Block Erase
8. Main Memory Page Program
9. Auto Page Rewrite

Group B modes consist of:

1. Buffer 1 (or 2) Read
2. Buffer 1 (or 2) Write
3. Status Register Read

If a Group A mode is in progress (not fully completed) then another mode in Group A should not be started. However, during this time in which a Group A mode is in progress, modes in Group B can be started.

Status Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RDY/$\overline{BUSY}$	COMP	1	0	1	X	X	X

This gives the Serial DataFlash the ability to virtually accommodate a continuous data stream. While data is being programmed into main memory from buffer 1, data can be loaded into buffer 2 (or vice versa). See application note AN-4 ("Using Atmel's Serial DataFlash") for more details.

HARDWARE PAGE WRITE PROTECT: If the $\overline{WP}$ pin is held low, the first 256 pages of the main memory cannot be reprogrammed. The only way to reprogram the first 256 pages is to first drive the protect pin high and then use the program commands previously mentioned. The $\overline{WP}$ pin is internally pulled high; therefore, connection of the $\overline{WP}$ pin is not necessary if this pin and feature will not be utilized. However, it is recommended that the $\overline{WP}$ pin be driven high externally whenever possible.

$\overline{RESET}$: A low state on the reset pin ($\overline{RESET}$) will terminate the operation in progress and reset the internal state machine to an idle state. The device will remain in the reset condition as long as a low level is present on the $\overline{RESET}$ pin. Normal operation can resume once the $\overline{RESET}$ pin is brought back to a high level.

The device incorporates an internal power-on reset circuit, so there are no restrictions on the $\overline{RESET}$ pin during power-on sequences. The $\overline{RESET}$ pin is also internally pulled high; therefore, connection of the $\overline{RESET}$ pin is not necessary if this pin and feature will not be utilized. However, it is recommended that the $\overline{RESET}$ pin be driven high externally whenever possible.

READY/$\overline{BUSY}$: This open drain output pin will be driven low when the device is busy in an internally self-timed operation. This pin, which is normally in a high state (through an external pull-up resistor), will be pulled low during programming operations, compare operations, and during page-to-buffer transfers.

The busy status indicates that the Flash memory array and one of the buffers cannot be accessed; read and write operations to the other buffer can still be performed.

Power On/Reset State

When power is first applied to the device, or when recovering from a reset condition, the device will default to SPI mode 3. In addition, the SO pin will be in a high impedance state, and a high to low transition on the $\overline{CS}$ pin will be required to start a valid instruction. The SPI mode will be automatically selected on every falling edge of $\overline{CS}$ by sampling the inactive clock state.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC and AC Operating Range

		AT45DB161
Operating Temperature (Case)	Com.	0°C to 70°C
	Ind.	-40°C to 85°C
V_{CC} Power Supply[1]		2.7V to 3.6V

Note: 1. After power is applied and V_{CC} is at the minimum specified data sheet value, the system should wait 20 ms before an operational mode is started.

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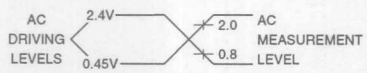
DC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{SB}	Standby Current	$\overline{CS}$, $\overline{RESET}$, $\overline{WP}$ = V_{IH}, all inputs at CMOS levels		3	10	µA
I_{CC1}	Active Current, Read Operation	f = 13 MHz; I_{OUT} = 0 mA; V_{CC} = 3.6V		4	10	mA
I_{CC2}	Active Current, Program/Erase Operation	V_{CC} = 3.6V		15	35	mA
I_{LI}	Input Load Current	V_{IN} = CMOS levels			1	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = CMOS levels			1	µA
V_{IL}	Input Low Voltage				0.6	V
V_{IH}	Input High Voltage		2.0			V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA; V_{CC} = 2.7V			0.4	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA	V_{CC} - 0.2V			V

AC Characteristics

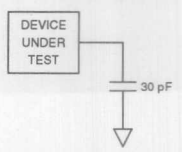
Symbol	Parameter	Min	Typ	Max	Units
f_{SCK}	SCK Frequency			13	MHz
t_{WH}	SCK High Time	35			ns
t_{WL}	SCK Low Time	35			ns
t_{CS}	Minimum $\overline{CS}$ High Time	250			ns
t_{CSS}	$\overline{CS}$ Setup Time	250			ns
t_{CSH}	$\overline{CS}$ Hold Time	250			ns
t_{CSB}	$\overline{CS}$ High to RDY/$\overline{BUSY}$ Low			200	ns
t_{SU}	Data In Setup Time	10			ns
t_H	Data In Hold Time	20			ns
t_{HO}	Output Hold Time	0			ns
t_{DIS}	Output Disable Time			25	ns
t_V	Output Valid			30	ns
t_{XFR}	Page to Buffer Transfer/Compare Time		250	350	µs
t_{EP}	Page Erase and Programming Time		10	20	ms
t_P	Page Programming Time		7	15	ms
t_{PE}	Page Erase Time		6	10	ms
t_{BE}	Block Erase Time		7	15	ms
t_{RST}	$\overline{RESET}$ Pulse Width	10			µs
t_{REC}	$\overline{RESET}$ Recovery Time			1	µs

Input Test Waveforms and Measurement Levels



t_R, t_F < 5 ns (10% to 90%)

Output Test Load

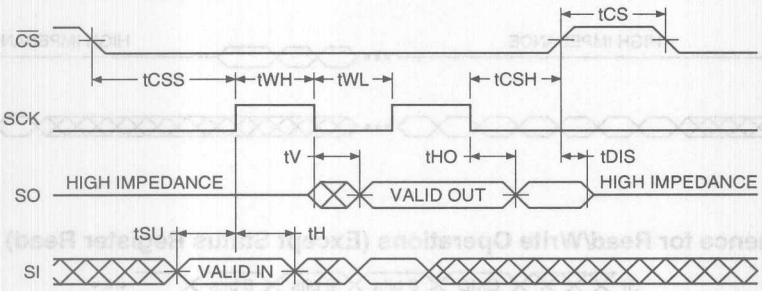


AC Waveforms

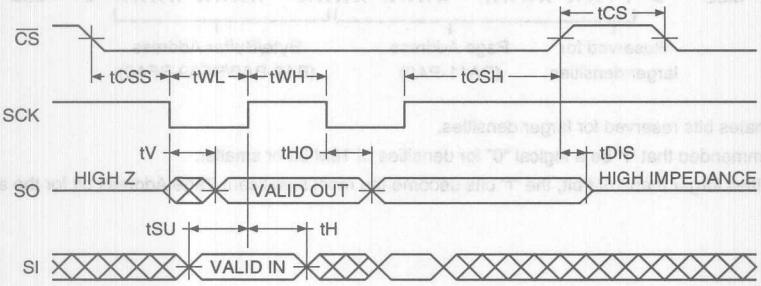
Two different timing diagrams are shown below. Waveform 1 shows the SCK signal being low when $\overline{CS}$ makes a high-to-low transition, and Waveform 2 shows the SCK signal being high when $\overline{CS}$ makes a high-to-low transition. Both waveforms show valid timing diagrams. The setup and hold times for the SI signal are referenced to the low-to-high transition on the SCK signal.

Waveform 1 shows timing that is also compatible with SPI Mode 0, and Waveform 2 shows timing that is compatible with SPI Mode 3

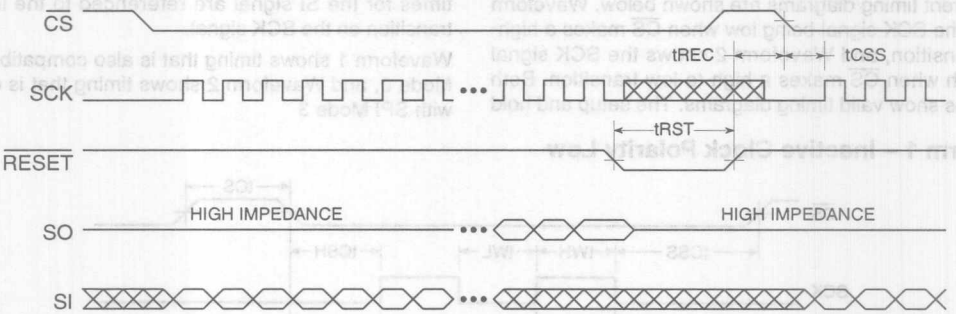
Waveform 1 – Inactive Clock Polarity Low



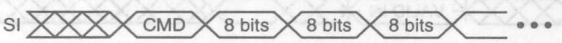
Waveform 2 – Inactive Clock Polarity High

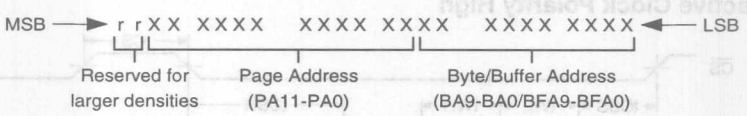


Reset Timing (Inactive Clock Polarity Low Shown)



Command Sequence for Read/Write Operations (Except Status Register Read)

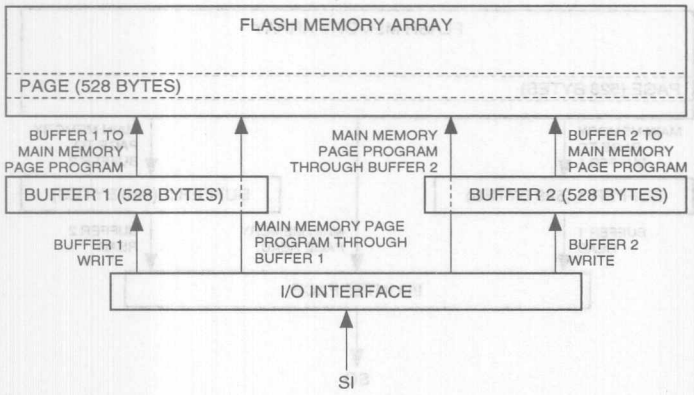




Notes:
1. "r" designates bits reserved for larger densities.
2. It is recommended that "r" be a logical "0" for densities of 16M bit or smaller.
3. For densities larger than 16M bit, the "r" bits become the most significant Page Address bit for the appropriate density.

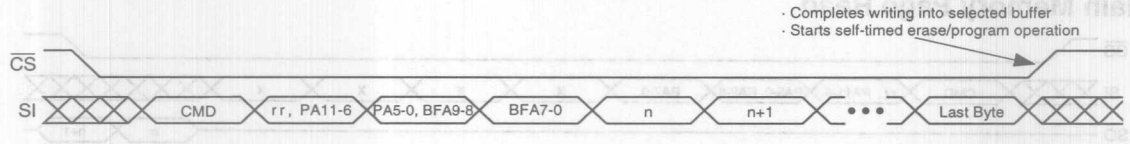
Write Operations

The following block diagram and waveforms illustrate the various write sequences available.

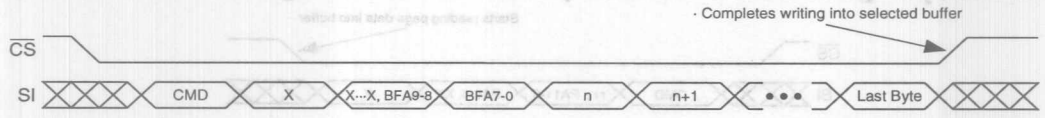


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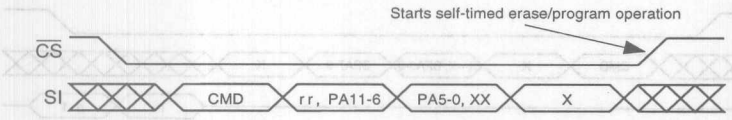
Main Memory Page Program through Buffers



Buffer Write



Buffer to Main Memory Page Program (Data from Buffer Programmed into Flash Page)

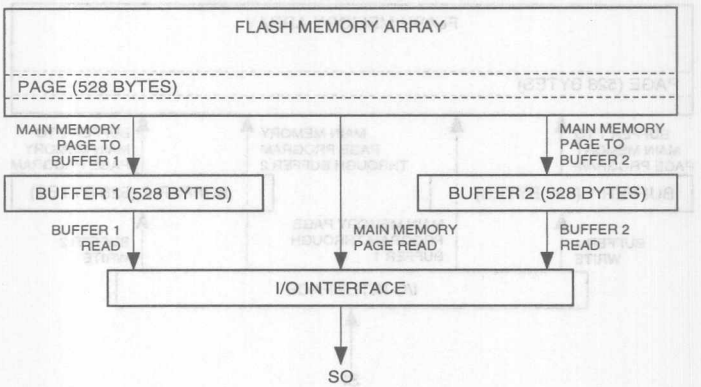


Each transition represents 8 bits and 8 clock cycles

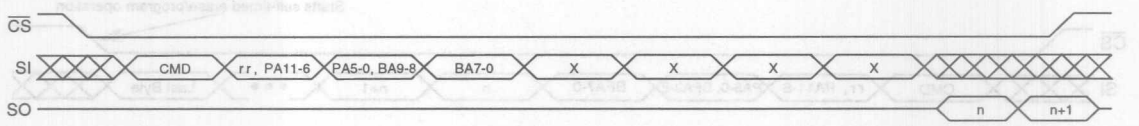
n = 1st byte written
n+1 = 2nd byte written

Read Operations

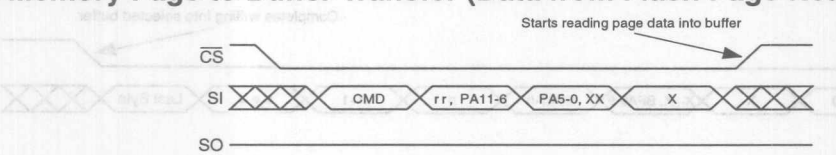
The following block diagram and waveforms illustrate the various read sequences available.



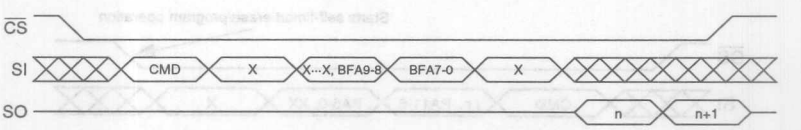
Main Memory Page Read



Main Memory Page to Buffer Transfer (Data from Flash Page Read into Buffer)



Buffer Read

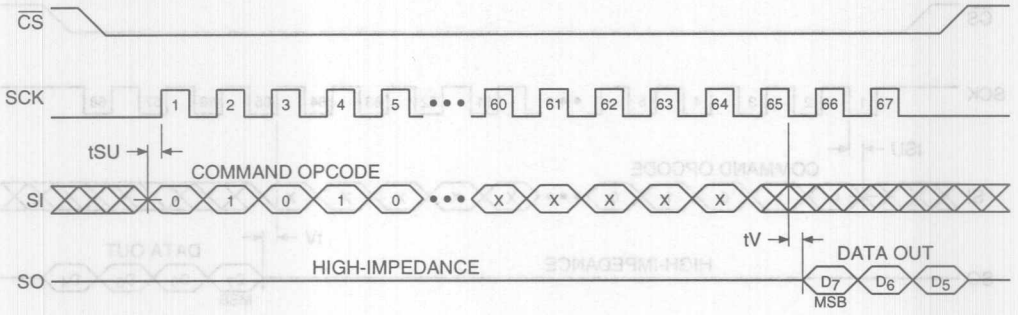


Each transition represents 8 bits and 8 clock cycles

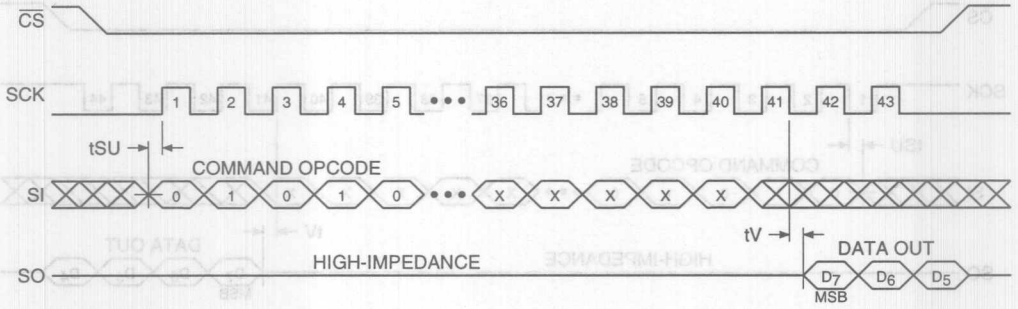
n = 1st byte read
n+1 = 2nd byte read

Detailed Bit-Level Read Timing – Inactive Clock Polarity Low

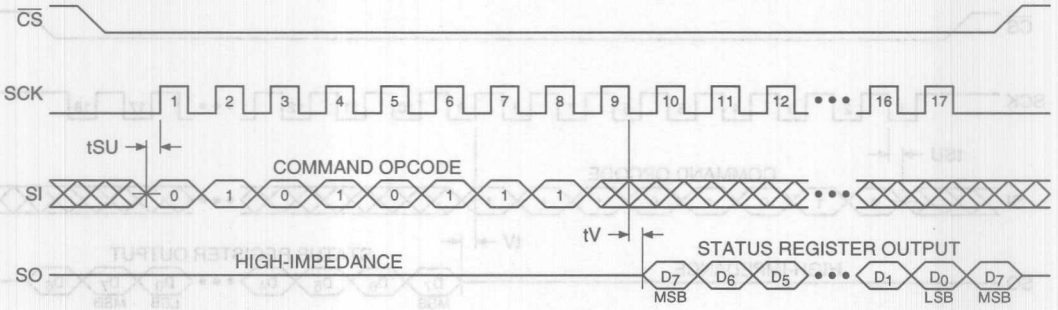
Main Memory Page Read



Buffer Read

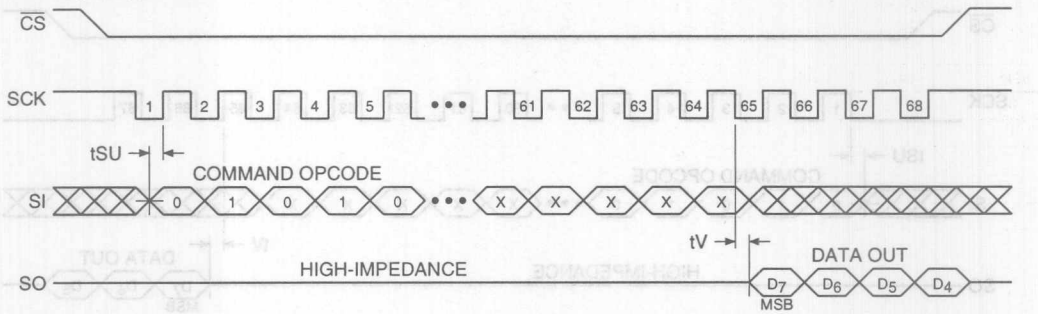


Status Register Read

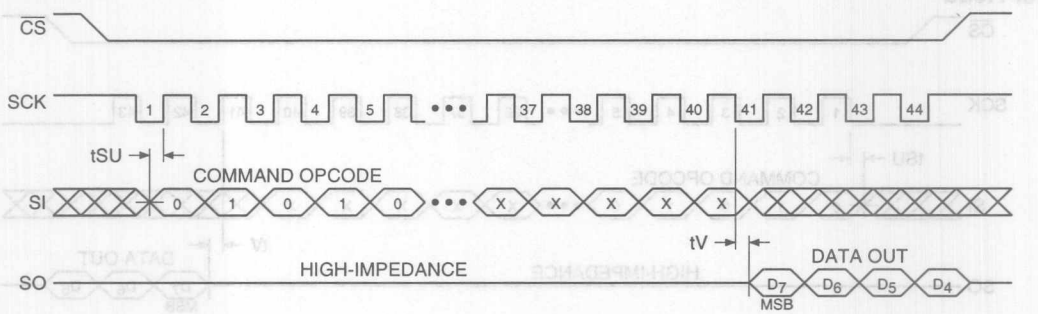


Detailed Bit-Level Read Timing – Inactive Clock Polarity High

Main Memory Page Read



Buffer Read



Status Register Read

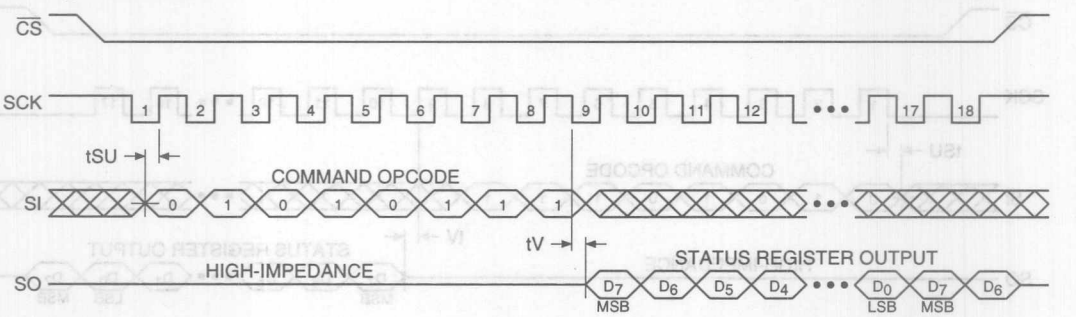


Table 1.

Main Memory Page Read	Buffer 1 Read	Buffer 2 Read	Main Memory Page to Buffer 1 Transfer	Main Memory Page to Buffer 2 Transfer	Main Memory Page to Buffer 1 Compare	Main Memory Page to Buffer 2 Compare	Buffer 1 Write	Buffer 2 Write
Opcode								
52H	54H	56H	53H	55H	60H	61H	84H	87H
0	0	0	0	0	0	0	1	1
1	1	1	1	1	1	1	0	0
0	0	0	0	0	1	1	0	0
1	1	1	1	1	0	0	0	0
0	0	0	0	0	0	0	0	0
0	1	1	0	1	0	0	1	1
1	0	1	1	0	0	0	0	1
0	0	0	1	1	0	1	0	1
r	X	X	r	r	r	r	X	X
r	X	X	r	r	r	r	X	X
PA11	X	X	PA11	PA11	PA11	PA11	X	X
PA10	X	X	PA10	PA10	PA10	PA10	X	X
PA9	X	X	PA9	PA9	PA9	PA9	X	X
PA8	X	X	PA8	PA8	PA8	PA8	X	X
PA7	X	X	PA7	PA7	PA7	PA7	X	X
PA6	X	X	PA6	PA6	PA6	PA6	X	X
PA5	X	X	PA5	PA5	PA5	PA5	X	X
PA4	X	X	PA4	PA4	PA4	PA4	X	X
PA3	X	X	PA3	PA3	PA3	PA3	X	X
PA2	X	X	PA2	PA2	PA2	PA2	X	X
PA1	X	X	PA1	PA1	PA1	PA1	X	X
PA0	X	X	PA0	PA0	PA0	PA0	X	X
BA9	BFA9	BFA9	X	X	X	X	BFA9	BFA9
BA8	BFA8	BFA8	X	X	X	X	BFA8	BFA8
BA7	BFA7	BFA7	X	X	X	X	BFA7	BFA7
BA6	BFA6	BFA6	X	X	X	X	BFA6	BFA6
BA5	BFA5	BFA5	X	X	X	X	BFA5	BFA5
BA4	BFA4	BFA4	X	X	X	X	BFA4	BFA4
BA3	BFA3	BFA3	X	X	X	X	BFA3	BFA3
BA2	BFA2	BFA2	X	X	X	X	BFA2	BFA2
BA1	BFA1	BFA1	X	X	X	X	BFA1	BFA1
BA0	BFA0	BFA0	X	X	X	X	BFA0	BFA0
X	X	X						
X	X	X						
X	X	X						
X	X	X						
X	X	X						
X	X	X						
X	X	X						
X	X	X						
•								
•								
•								
X (64th bit)								

X (Don't Care)
r (reserved bits)

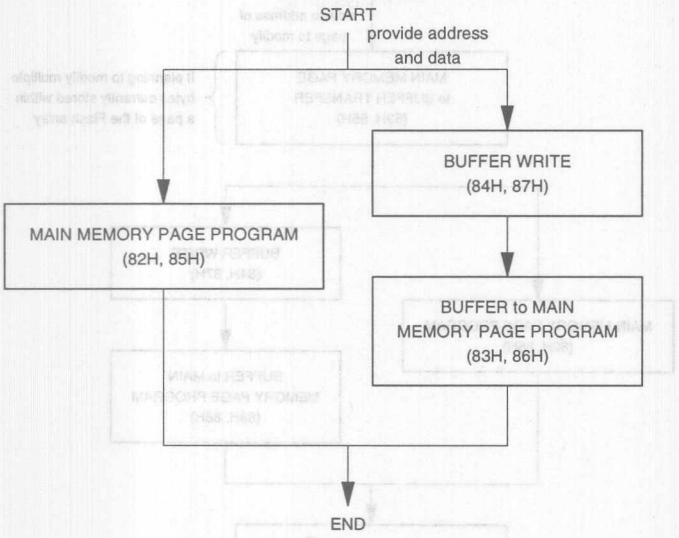
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Table 2.

Buffer 1 to Main Memory Page Program with Built-In Erase	Buffer 2 to Main Memory Page Program with Built-In Erase	Buffer 1 to Main Memory Page Program without Built-In Erase	Buffer 2 to Main Memory Page Program without Built-In Erase	Page Erase	Block Erase	Main Memory Page Program Through Buffer 1	Main Memory Page Program Through Buffer 2	Auto Page Rewrite Through Buffer 1	Auto Page Rewrite Through Buffer 2	Status Register
Opcode										
83H	86H	88H	89H	81H	50H	82H	85H	58H	59H	57H
1	1	1	1	1	0	1	1	0	0	0
0	0	0	0	0	1	0	0	1	1	1
0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	1	0	0	1	1	1
0	0	1	1	0	0	0	0	1	1	0
0	1	0	0	0	0	0	1	0	0	1
1	1	0	0	0	0	1	0	0	0	1
1	0	0	1	1	0	0	1	0	1	1
r	r	r	r	r	r	r	r	r	r	
r	r	r	r	r	r	r	r	r	r	
PA11	PA11	PA11	PA11	PA11	PA11	PA11	PA11	PA11	PA11	
PA10	PA10	PA10	PA10	PA10	PA10	PA10	PA10	PA10	PA10	
PA9	PA9	PA9	PA9	PA9	PA9	PA9	PA9	PA9	PA9	
PA8	PA8	PA8	PA8	PA8	PA8	PA8	PA8	PA8	PA8	
PA7	PA7	PA7	PA7	PA7	PA7	PA7	PA7	PA7	PA7	
PA6	PA6	PA6	PA6	PA6	PA6	PA6	PA6	PA6	PA6	
PA5	PA5	PA5	PA5	PA5	PA5	PA5	PA5	PA5	PA5	
PA4	PA4	PA4	PA4	PA4	PA4	PA4	PA4	PA4	PA4	
PA3	PA3	PA3	PA3	PA3	PA3	PA3	PA3	PA3	PA3	
PA2	PA2	PA2	PA2	PA2	X	PA2	PA2	PA2	PA2	
PA1	PA1	PA1	PA1	PA1	X	PA1	PA1	PA1	PA1	
PA0	PA0	PA0	PA0	PA0	X	PA0	PA0	PA0	PA0	
X	X	X	X	X	X	BFA9	BFA9	X	X	
X	X	X	X	X	X	BFA8	BFA8	X	X	
X	X	X	X	X	X	BFA7	BFA7	X	X	
X	X	X	X	X	X	BFA6	BFA6	X	X	
X	X	X	X	X	X	BFA5	BFA5	X	X	
X	X	X	X	X	X	BFA4	BFA4	X	X	
X	X	X	X	X	X	BFA3	BFA3	X	X	
X	X	X	X	X	X	BFA2	BFA2	X	X	
X	X	X	X	X	X	BFA1	BFA1	X	X	
X	X	X	X	X	X	BFA0	BFA0	X	X	

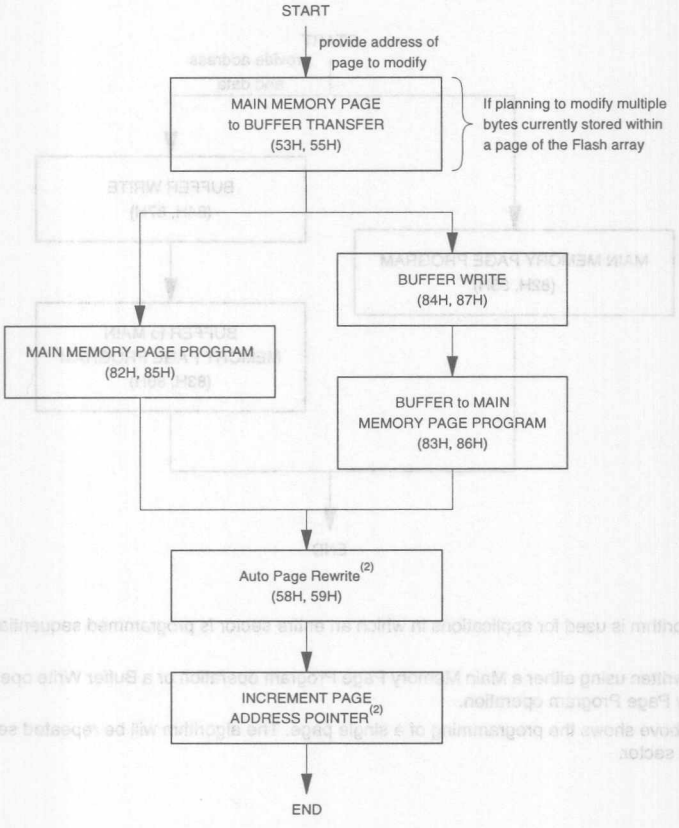
X (Don't Care)
r (reserved bits)

Figure 1. Algorithm for Programming or Reprogramming of an Entire Sector Sequentially



Notes:
1. This type of algorithm is used for applications in which an entire sector is programmed sequentially, filling the sector page-by-page.
2. A page can be written using either a Main Memory Page Program operation or a Buffer Write operation followed by a Buffer to Main Memory Page Program operation.
3. The algorithm above shows the programming of a single page. The algorithm will be repeated sequentially for each page within the entire sector.

Figure 2. Algorithm for Randomly Modifying Data



Notes:
1. To preserve data integrity, each page of a DataFlash sector (256 pages per sector) must be updated/rewritten at least once within every 10,000 cumulative page erase/program operations within that sector.
2. A Page Address Pointer must be maintained to indicate which page is to be rewritten. The Auto Page Rewrite command must use the address specified by the Page Address Pointer.
3. Other algorithms can be used to rewrite portions of the Flash array. Low power applications may choose to wait until 10,000 cumulative page erase/program operations have accumulated before rewriting all 256 pages of the sector. See application note AN-4 ("Using Atmel's Serial DataFlash") for more details.

Sector Addressing

PA11	PA10	PA9	PA8	Sector
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

Ordering Information

f_{SCK} (MHz)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
13	10	0.01	AT45DB161-JC AT45DB161-RC AT45DB161-TC AT45DB161-CC	32J 28R 28T 24C2	Commercial (0°C to 70°C)
13	10	0.01	AT45DB161-JI AT45DB161-RI AT45DB161-TI AT45DB161-CI	32J 28R 28T 24C2	Industrial (-40°C to 85°C)

Package Type	
32J	32-Lead, Plastic J-Leaded Chip Carrier (PLCC)
28R	28-Lead, 0.330" Wide, Plastic Gull Wing Small Outline (SOIC)
28T	28-Lead, Plastic Thin Small Outline Package (TSOP)
24C2	24-Ball, 5 x 5 Array Plastic Chip-Scale Ball Grid Array (CBGA)

Features

- Single 2.7V - 3.6V Supply
- Serial Interface Architecture
- Page Program Operation
  - Single Cycle Reprogram (Erase and Program)
  - 8192 Pages (528 Bytes/Page) Main Memory
- Optional Page and Block Erase Operations
- Two 528-Byte SRAM Data Buffers – Allows Receiving of Data while Reprogramming of Nonvolatile Memory
- Internal Program and Control Timer
- Fast Page Program Time – 7 ms Typical
- 120 µs Typical Page to Buffer Transfer Time
- Low-Power Dissipation
  - 4 mA Active Read Current Typical
  - 3 µA CMOS Standby Current Typical
- 13 MHz Max Clock Frequency
- Hardware Data Protection Feature
- Serial Peripheral Interface (SPI) Compatible – Modes 0 and 3
- CMOS and TTL Compatible Inputs and Outputs
- Commercial and Industrial Temperature Ranges

Description

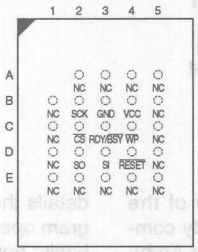
The AT45DB321 is a 2.7-volt only, serial interface Flash memory suitable for in-system reprogramming. Its 34,603,008 bits of memory are organized as 8192 pages of 528 bytes each. In addition to the main memory, the AT45DB321 also contains two SRAM data buffers of 528 bytes each. The buffers allow receiving of data while a page in the main memory is being reprogrammed. Unlike conventional Flash memo-

(continued)

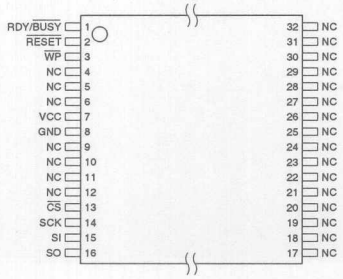
Pin Configurations

Pin Name	Function
$\overline{CS}$	Chip Select
SCK	Serial Clock
SI	Serial Input
SO	Serial Output
$\overline{WP}$	Hardware Page Write Protect Pin
$\overline{RESET}$	Chip Reset
RDY/$\overline{BUSY}$	Ready/Busy

CBGA Top View Through Package



TSOP Top View
Type 1



32-Megabit 2.7-volt Only Serial DataFlash®

4

AT45DB321 Preliminary

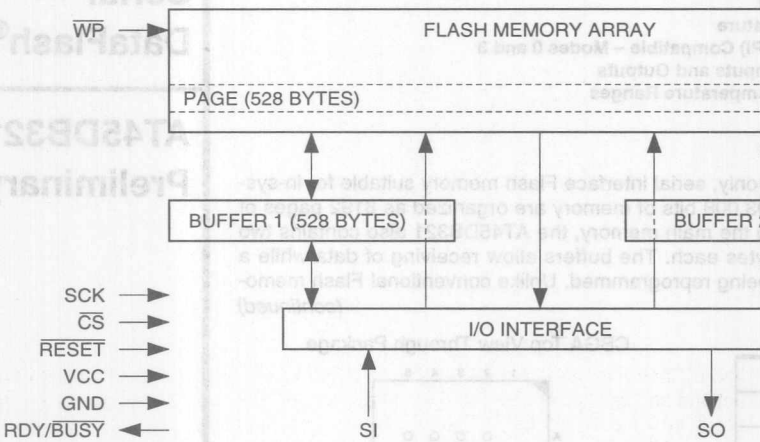
Rev. 1121A–09/98

ries that are accessed randomly with multiple address lines and a parallel interface, the DataFlash uses a serial interface to sequentially access its data. The simple serial interface facilitates hardware layout, increases system reliability, minimizes switching noise, and reduces package size and active pin count. The device is optimized for use in many commercial and industrial applications where high density, low pin count, low voltage, and low power are essential. Typical applications for the DataFlash are digital voice storage, image storage, and data storage. The device operates at clock frequencies up to 13 MHz with a typical active read current consumption of 4 mA.

To allow for simple in-system reprogrammability, the AT45DB321 does not require high input voltages for programming. The device operates from a single power supply, 2.7V to 3.6V, for both the program and read operations. The AT45DB321 is enabled through the chip select pin ($\overline{CS}$) and accessed via a three-wire interface consisting of the Serial Input (SI), Serial Output (SO), and the Serial Clock (SCK).

All programming cycles are self-timed, and no separate erase cycle is required before programming.

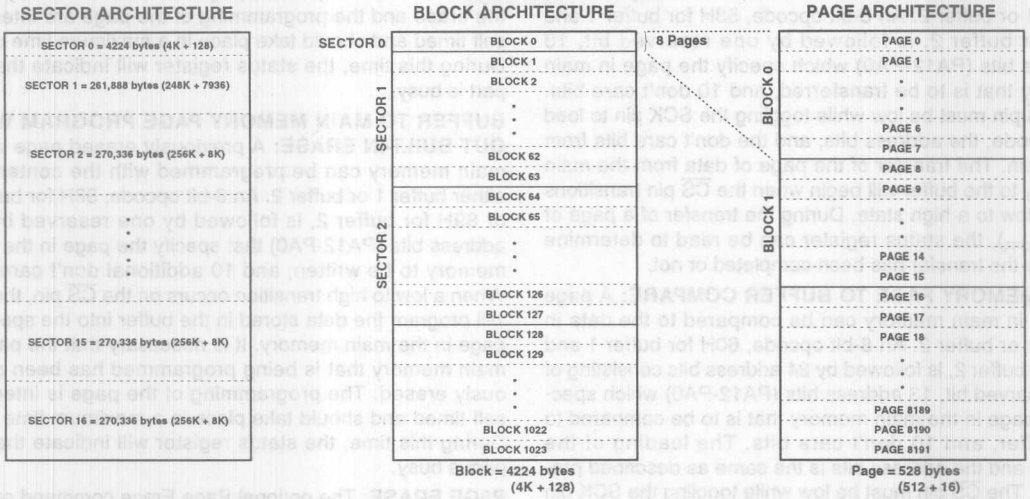
Block Diagram



Memory Array

To provide optimal flexibility, the memory array of the AT45DB321 is divided into three levels of granularity comprising of sectors, blocks, and pages. The Memory Architecture Diagram illustrates the breakdown of each level and details the number of pages per sector and block. All program operations to the DataFlash occur on a page by page basis; however, the optional erase operations can be performed at the block or page level.

Memory Architecture Diagram



Device Operation

The device operation is controlled by instructions from the host processor. The list of instructions and their associated opcodes are contained in Table 1 and Table 2. A valid instruction starts with the falling edge of $\overline{CS}$ followed by the appropriate 8-bit opcode and the desired buffer or main memory address location. While the $\overline{CS}$ pin is low, toggling the SCK pin controls the loading of the opcode and the desired buffer or main memory address location through the SI (serial input) pin. All instructions, addresses, and data are transferred with the most significant bit (MSB) first.

Read

By specifying the appropriate opcode, data can be read from the main memory or from either one of the two data buffers.

MAIN MEMORY PAGE READ: A main memory read allows the user to read data directly from any one of the 8192 pages in the main memory, bypassing both of the data buffers and leaving the contents of the buffers unchanged. To start a page read, the 8-bit opcode, 52H, is followed by 24 address bits and 32 don't care bits. In the AT45DB321, the first address bit is reserved for larger density devices (see Notes on page 10), the next 13 address bits (PA12-PA0) specify the page address, and the next 10 address bits (BA9-BA0) specify the starting byte address within the page. The 32 don't care bits which follow the 24 address bits are sent to initialize the read operation. Following the 32 don't care bits, additional pulses on SCK result in serial data being output on the SO (serial output) pin. The $\overline{CS}$ pin must remain low during the loading of the opcode, the address bits, and the reading of data. When the end of a page in main memory is reached during a main memory page read, the device will continue reading at the beginning of the same page. A low to high transition on the $\overline{CS}$ pin will terminate the read operation and tri-state the SO pin.

BUFFER READ: Data can be read from either one of the two buffers, using different opcodes to specify which buffer to read from. An opcode of 54H is used to read data from buffer 1, and an opcode of 56H is used to read data from buffer 2. To perform a buffer read, the eight bits of the opcode must be followed by 14 don't care bits, 10 address bits, and eight don't care bits. Since the buffer size is 528-bytes, 10 address bits (BFA9-BFA0) are required to specify the first byte of data to be read from the buffer. The $\overline{CS}$ pin must remain low during the loading of the opcode, the address bits, the don't care bits, and the reading of data. When the end of a buffer is reached, the device will continue reading back at the beginning of the buffer. A low to high transition on the $\overline{CS}$ pin will terminate the read operation and tri-state the SO pin.

MAIN MEMORY PAGE TO BUFFER TRANSFER: A page of data can be transferred from the main memory to either buffer 1 or buffer 2. An 8-bit opcode, 53H for buffer 1 and 55H for buffer 2, is followed by one reserved bit, 13 address bits (PA12-PA0) which specify the page in main memory that is to be transferred, and 10 don't care bits. The $\overline{CS}$ pin must be low while toggling the SCK pin to load the opcode, the address bits, and the don't care bits from the SI pin. The transfer of the page of data from the main memory to the buffer will begin when the $\overline{CS}$ pin transitions from a low to a high state. During the transfer of a page of data (t_{XFR}), the status register can be read to determine whether the transfer has been completed or not.

MAIN MEMORY PAGE TO BUFFER COMPARE: A page of data in main memory can be compared to the data in buffer 1 or buffer 2. An 8-bit opcode, 60H for buffer 1 and 61H for buffer 2, is followed by 24 address bits consisting of one reserved bit, 13 address bits (PA12-PA0) which specify the page in the main memory that is to be compared to the buffer, and 10 don't care bits. The loading of the opcode and the address bits is the same as described previously. The $\overline{CS}$ pin must be low while toggling the SCK pin to load the opcode, the address bits, and the don't care bits from the SI pin. On the low to high transition of the $\overline{CS}$ pin, the 528 bytes in the selected main memory page will be compared with the 528 bytes in buffer 1 or buffer 2. During this time (t_{XFR}), the status register will indicate that the part is busy. On completion of the compare operation, bit 6 of the status register is updated with the result of the compare.

Program

BUFFER WRITE: Data can be shifted in from the SI pin into either buffer 1 or buffer 2. To load data into either buffer, an 8-bit opcode, 84H for buffer 1 or 87H for buffer 2, is followed by 14 don't care bits and 10 address bits (BFA9-BFA0). The 10 address bits specify the first byte in the buffer to be written. The data is entered following the address bits. If the end of the data buffer is reached, the device will wrap around back to the beginning of the buffer. Data will continue to be loaded into the buffer until a low to high transition is detected on the $\overline{CS}$ pin.

BUFFER TO MAIN MEMORY PAGE PROGRAM WITH BUILT-IN ERASE: Data written into either buffer 1 or buffer 2 can be programmed into the main memory. An 8-bit opcode, 83H for buffer 1 or 86H for buffer 2, is followed by one reserved bit, 13 address bits (PA12-PA0) that specify the page in the main memory to be written, and 10 additional don't care bits. When a low to high transition occurs on the $\overline{CS}$ pin, the part will first erase the selected page in main memory to all 1s and then program the data stored in the buffer into the specified page in the main memory. Both the erase and the programming of the page are internally self timed and should take place in a maximum time of t_{EP}. During this time, the status register will indicate that the part is busy.

BUFFER TO MAIN MEMORY PAGE PROGRAM WITHOUT BUILT-IN ERASE: A previously erased page within main memory can be programmed with the contents of either buffer 1 or buffer 2. An 8-bit opcode, 88H for buffer 1 or 89H for buffer 2, is followed by one reserved bit, 13 address bits (PA12-PA0) that specify the page in the main memory to be written, and 10 additional don't care bits. When a low to high transition occurs on the $\overline{CS}$ pin, the part will program the data stored in the buffer into the specified page in the main memory. It is necessary that the page in main memory that is being programmed has been previously erased. The programming of the page is internally self timed and should take place in a maximum time of t_P. During this time, the status register will indicate that the part is busy.

PAGE ERASE: The optional Page Erase command can be used to individually erase any page in the main memory array allowing the Buffer to Main Memory Page Program without Built-In Erase command to be utilized at a later time. To perform a Page Erase, an opcode of 81H must be loaded into the device, followed by one reserved bit, 13 address bits (PA12-PA0), and 10 don't care bits. The 13 address bits are used to specify which page of the memory array is to be erased. When a low to high transition occurs on the $\overline{CS}$ pin, the part will erase the selected page to 1s. The erase operation is internally self-timed and should take place in a maximum time of t_{PE}. During this time, the status register will indicate that the part is busy.

BLOCK ERASE: A block of eight pages can be erased at one time allowing the Buffer to Main Memory Page Program without Built-In Erase command to be utilized to reduce programming times when writing large amounts of data to the device. To perform a Block Erase, an opcode of 50H must be loaded into the device, followed by one reserved bit, 10 address bits (PA12-PA3), and 13 don't care bits. The 10 address bits are used to specify which block of eight pages is to be erased. When a low to high transition occurs on the $\overline{CS}$ pin, the part will erase the selected block of eight pages to 1s. The erase operation is internally self-timed and should take place in a maximum time of t_{BE}. During this time, the status register will indicate that the part is busy.

Block Erase Addressing

PA12	PA11	PA10	PA9	PA8	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	Block
0	0	0	0	0	0	0	0	0	0	X	X	X	0
0	0	0	0	0	0	0	0	0	1	X	X	X	1
0	0	0	0	0	0	0	0	1	0	X	X	X	2
0	0	0	0	0	0	0	0	1	1	X	X	X	3
•	•	•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•	•	•
1	1	1	1	1	1	1	1	0	0	X	X	X	1020
1	1	1	1	1	1	1	1	0	1	X	X	X	1021
1	1	1	1	1	1	1	1	1	0	X	X	X	1022
1	1	1	1	1	1	1	1	1	1	X	X	X	1023

MAIN MEMORY PAGE PROGRAM: This operation is a combination of the Buffer Write and Buffer to Main Memory Page Program with Built-In Erase operations. Data is first shifted into buffer 1 or buffer 2 from the SI pin and then programmed into a specified page in the main memory. An 8-bit opcode, 82H for buffer 1 or 85H for buffer 2, is followed by one reserved bit and 23 address bits. The 13 most significant address bits (PA12-PA0) select the page in the main memory where data is to be written, and the next 10 address bits (BFA9-BFA0) select the first byte in the buffer to be written. After all address bits are shifted in, the part will take data from the SI pin and store it in one of the data buffers. If the end of the buffer is reached, the device will wrap around back to the beginning of the buffer. When there is a low to high transition on the $\overline{CS}$ pin, the part will first erase the selected page in main memory to all 1s and then program the data stored in the buffer into the specified page in the main memory. Both the erase and the programming of the page are internally self timed and should take place in a maximum of time t_{EP}. During this time, the status register will indicate that the part is busy.

AUTO PAGE REWRITE: This mode is only needed if multiple bytes within a page or multiple pages of data are modified in a random fashion. This mode is a combination of two operations: Main Memory Page to Buffer Transfer and Buffer to Main Memory Page Program with Built-In Erase. A page of data is first transferred from the main memory to buffer 1 or buffer 2, and then the same data (from buffer 1 or buffer 2) is programmed back into its original page of main memory. An 8-bit opcode, 58H for buffer 1 or 59H for buffer 2, is followed by one reserved bit, 13 address bits (PA12-PA0) that specify the page in main memory to be rewritten, and 10 additional don't care bits. When a low to high transition occurs on the $\overline{CS}$ pin, the part will first transfer data from the page in main memory to a buffer and then program the data from the buffer back into same page of main memory. The operation is internally self-timed and should take place in a maximum time of t_{EP}. During this time, the status register will indicate that the part is busy.

If a sector is programmed or reprogrammed sequentially page by page, then the programming algorithm shown in Figure 1 is recommended. Otherwise, if multiple bytes in a page or several pages are programmed randomly in a sector, then the programming algorithm shown in Figure 2 is recommended.

STATUS REGISTER: The status register can be used to determine the device's ready/busy status, the result of a Main Memory Page to Buffer Compare operation, or the device density. To read the status register, an opcode of 57H must be loaded into the device. After the last bit of the opcode is shifted in, the eight bits of the status register, starting with the MSB (bit 7), will be shifted out on the SO pin during the next eight clock cycles. The five most-significant bits of the status register will contain device information, while the remaining three least-significant bits are reserved for future use and will have undefined values. After bit 0 of the status register has been shifted out, the sequence will repeat itself (as long as $\overline{CS}$ remains low and SCK is being toggled) starting again with bit 7. The data in the status register is constantly updated, so each repeating sequence will output new data.

Ready/busy status is indicated using bit 7 of the status register. If bit 7 is a 1, then the device is not busy and is ready to accept the next command. If bit 7 is a 0, then the device is in a busy state. The user can continuously poll bit 7 of the status register by stopping SCK once bit 7 has been output. The status of bit 7 will continue to be output on the SO pin, and once the device is no longer busy, the state of SO will change from 0 to 1. There are eight operations which can

cause the device to be in a busy state: Main Memory Page to Buffer Transfer, Main Memory Page to Buffer Compare, Buffer to Main Memory Page Program with Built-In Erase, Buffer to Main Memory Page Program without Built-In Erase, Page Erase, Block Erase, Main Memory Page Program, and Auto Page Rewrite.

The result of the most recent Main Memory Page to Buffer Compare operation is indicated using bit 6 of the status register. If bit 6 is a 0, then the data in the main memory page matches the data in the buffer. If bit 6 is a 1, then at least one bit of the data in the main memory page does not match the data in the buffer.

The device density is indicated using bits 5, 4, and 3 of the status register. For the AT45DB321, the three bits are 1, 1, and 0. The decimal value of these three binary bits does not equate to the device density; the three bits represent a combinational code relating to differing densities of Serial DataFlash devices, allowing a total of eight different density configurations.

Read/Program Mode Summary

The modes listed above can be separated into two groups — modes which make use of the flash memory array (Group A) and modes which do not make use of the flash memory array (Group B).

Group A modes consist of:

1. Main Memory Page Read
2. Main Memory Page to Buffer 1 (or 2) Transfer
3. Main Memory Page to Buffer 1 (or 2) Compare
4. Buffer 1 (or 2) to Main Memory Page Program With Built-In Erase
5. Buffer 1 (or 2) to Main Memory Page Program Without Built-In Erase
6. Page Erase
7. Block Erase
8. Main Memory Page Program
9. Auto Page Rewrite

Group B modes consist of:

1. Buffer 1 (or 2) Read
2. Buffer 1 (or 2) Write
3. Status Register Read

If a Group A mode is in progress (not fully completed) then another mode in Group A should not be started. However, during this time in which a Group A mode is in progress, modes in Group B can be started.

Status Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RDY/$\overline{\text{BUSY}}$	COMP	1	1	0	X	X	X

This gives the Serial DataFlash the ability to virtually accommodate a continuous data stream. While data is being programmed into main memory from buffer 1, data can be loaded into buffer 2 (or vice versa). See application note AN-4 ("Using Atmel's Serial DataFlash") for more details.

HARDWARE PAGE WRITE PROTECT: If the $\overline{\text{WP}}$ pin is held low, the first 256 pages of the main memory cannot be reprogrammed. The only way to reprogram the first 256 pages is to first drive the protect pin high and then use the program commands previously mentioned. The $\overline{\text{WP}}$ pin is internally pulled high; therefore, connection of the $\overline{\text{WP}}$ pin is not necessary if this pin and feature will not be utilized. However, it is recommended that the $\overline{\text{WP}}$ pin be driven high externally whenever possible.

$\overline{\text{RESET}}$: A low state on the reset pin ($\overline{\text{RESET}}$) will terminate the operation in progress and reset the internal state machine to an idle state. The device will remain in the reset condition as long as a low level is present on the $\overline{\text{RESET}}$ pin. Normal operation can resume once the $\overline{\text{RESET}}$ pin is brought back to a high level.

The device incorporates an internal power-on reset circuit, so there are no restrictions on the $\overline{\text{RESET}}$ pin during power-on sequences. The $\overline{\text{RESET}}$ pin is also internally pulled high; therefore, connection of the $\overline{\text{RESET}}$ pin is not necessary if this pin and feature will not be utilized. However, it is recommended that the $\overline{\text{RESET}}$ pin be driven high externally whenever possible.

READY/$\overline{\text{BUSY}}$: This open drain output pin will be driven low when the device is busy in an internally self-timed operation. This pin, which is normally in a high state (through an external pull-up resistor), will be pulled low during programming operations, compare operations, and during page-to-buffer transfers.

The busy status indicates that the Flash memory array and one of the buffers cannot be accessed; read and write operations to the other buffer can still be performed.

Power On/Reset State

When power is first applied to the device, or when recovering from a reset condition, the device will default to SPI mode 3. In addition, the SO pin will be in a high impedance state, and a high to low transition on the $\overline{\text{CS}}$ pin will be required to start a valid instruction. The SPI mode will be automatically selected on every falling edge of $\overline{\text{CS}}$ by sampling the inactive clock state.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC and AC Operating Range

		AT45DB321
Operating Temperature (Case)	Com.	0°C to 70°C
	Ind.	-40°C to 85°C
V_{CC} Power Supply[1]		2.7V to 3.6V

Note: 1. After power is applied and V_{CC} is at the minimum specified data sheet value, the system should wait 20 ms before an operational mode is started.

4

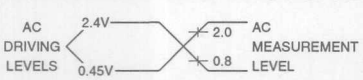
DC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{SB}	Standby Current	$\overline{CS}$, $\overline{RESET}$, $\overline{WP}$ = V_{IH}, all inputs at CMOS levels		3	10	µA
I_{CC1}	Active Current, Read Operation	f = 13 MHz; I_{OUT} = 0 mA; V_{CC} = 3.6V		4	10	mA
I_{CC2}	Active Current, Program/Erase Operation	V_{CC} = 3.6V		15	35	mA
I_{LI}	Input Load Current	V_{IN} = CMOS levels			1	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = CMOS levels			1	µA
V_{IL}	Input Low Voltage				0.6	V
V_{IH}	Input High Voltage		2.0			V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA; V_{CC} = 2.7V			0.4	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA	V_{CC} - 0.2V			V

AC Characteristics

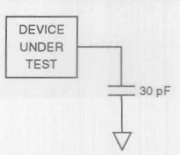
Symbol	Parameter	Min	Typ	Max	Units
f_{SCK}	SCK Frequency			13	MHz
t_{WH}	SCK High Time	35			ns
t_{WL}	SCK Low Time	35			ns
t_{CS}	Minimum $\overline{CS}$ High Time	250			ns
t_{CSS}	$\overline{CS}$ Setup Time	250			ns
t_{CSH}	$\overline{CS}$ Hold Time	250			ns
t_{CSB}	$\overline{CS}$ High to RDY/$\overline{BUSY}$ Low			200	ns
t_{SU}	Data In Setup Time	10			ns
t_H	Data In Hold Time	20			ns
t_{HO}	Output Hold Time	0			ns
t_{DIS}	Output Disable Time			25	ns
t_V	Output Valid			30	ns
t_{XFR}	Page to Buffer Transfer/Compare Time		250	350	µs
t_{EP}	Page Erase and Programming Time		10	20	ms
t_P	Page Programming Time		7	15	ms
t_{PE}	Page Erase Time		6	10	ms
t_{BE}	Block Erase Time		7	15	ms
t_{RST}	$\overline{RESET}$ Pulse Width	10			µs
t_{REC}	$\overline{RESET}$ Recovery Time			1	µs

Input Test Waveforms and Measurement Levels



t_R, t_F < 5 ns (10% to 90%)

Output Test Load

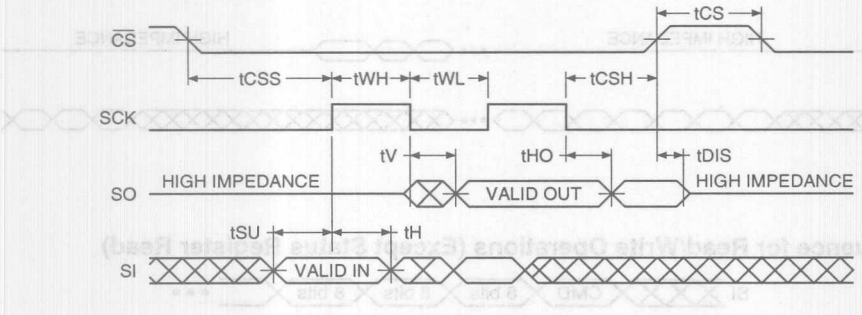


AC Waveforms

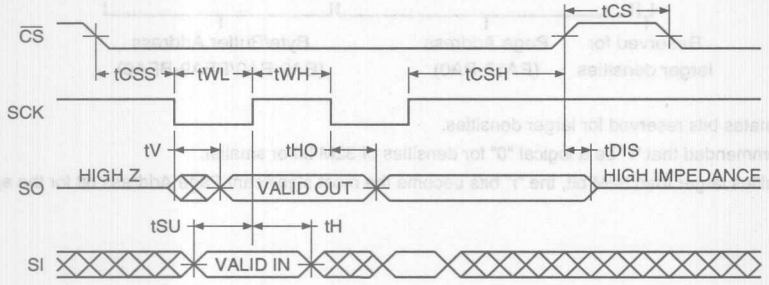
Two different timing diagrams are shown below. Waveform 1 shows the SCK signal being low when $\overline{CS}$ makes a high-to-low transition, and Waveform 2 shows the SCK signal being high when $\overline{CS}$ makes a high-to-low transition. Both waveforms show valid timing diagrams. The setup and hold times for the SI signal are referenced to the low-to-high transition on the SCK signal.

Waveform 1 shows timing that is also compatible with SPI Mode 0, and Waveform 2 shows timing that is compatible with SPI Mode 3

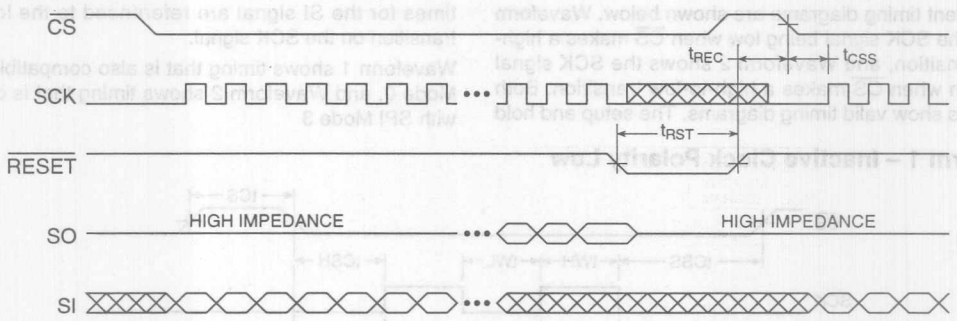
Waveform 1 – Inactive Clock Polarity Low



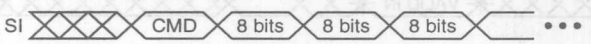
Waveform 2 – Inactive Clock Polarity High

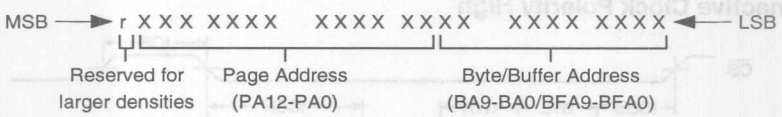


Reset Timing (Inactive Clock Polarity Low Shown)



Command Sequence for Read/Write Operations (Except Status Register Read)

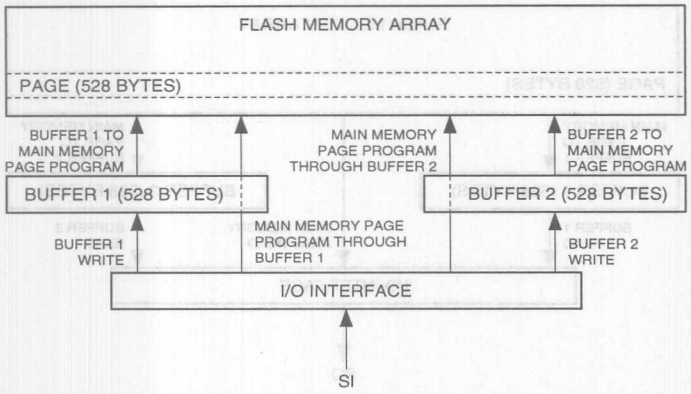




Notes:
1. "r" designates bits reserved for larger densities.
2. It is recommended that "r" be a logical "0" for densities of 32M bit or smaller.
3. For densities larger than 32M bit, the "r" bits become the most significant Page Address bit for the appropriate density.

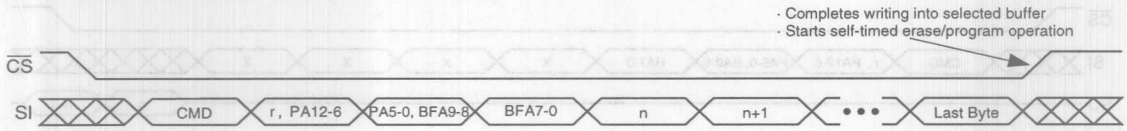
Write Operations

The following block diagram and waveforms illustrate the various write sequences available.

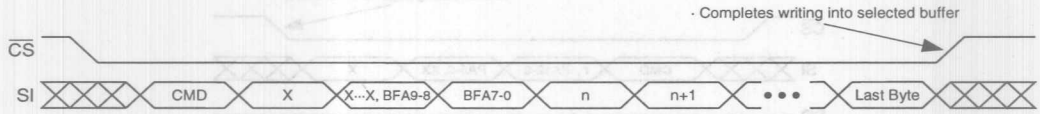


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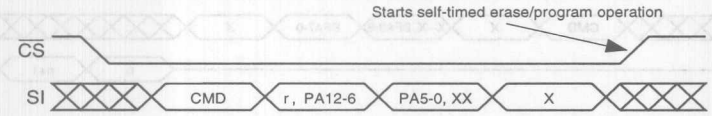
Main Memory Page Program through Buffers



Buffer Write



Buffer to Main Memory Page Program (Data from Buffer Programmed into Flash Page)

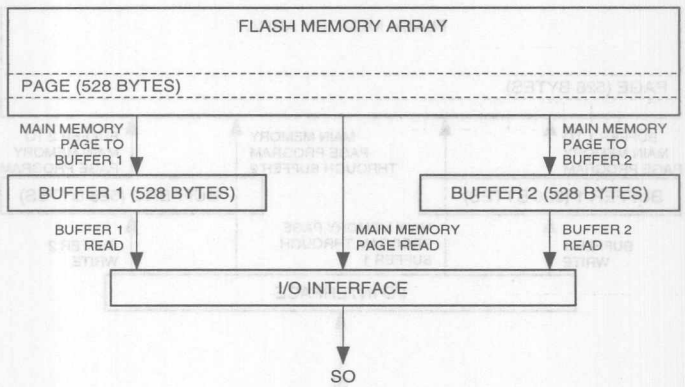


Each transition represents 8 bits and 8 clock cycles

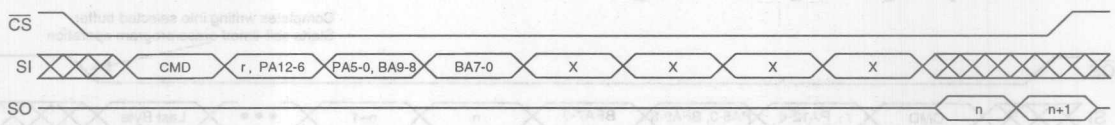
n = 1st byte written
n+1 = 2nd byte written

Read Operations

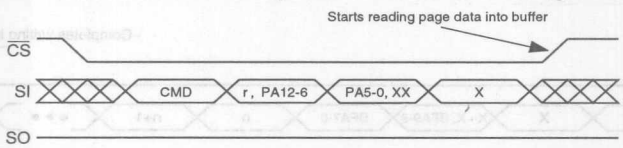
The following block diagram and waveforms illustrate the various read sequences available.



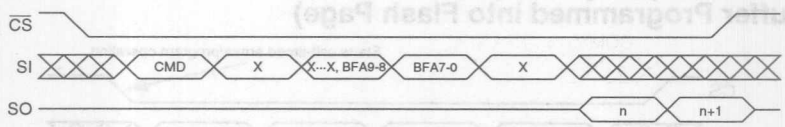
Main Memory Page Read



Main Memory Page to Buffer Transfer (Data from Flash Page Read into Buffer)



Buffer Read

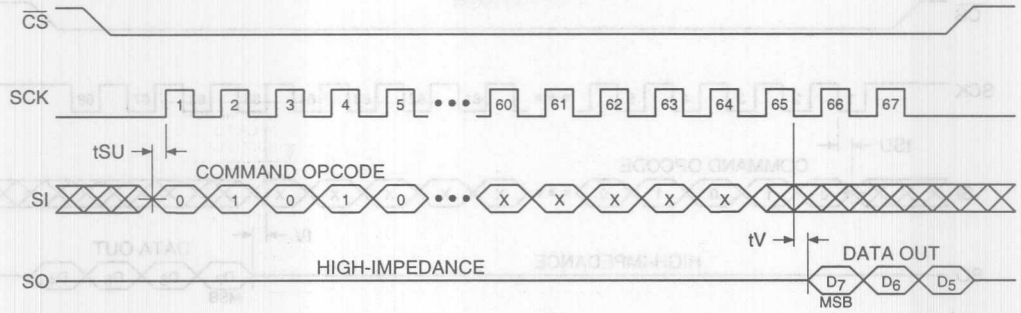


Each transition represents 8 bits and 8 clock cycles

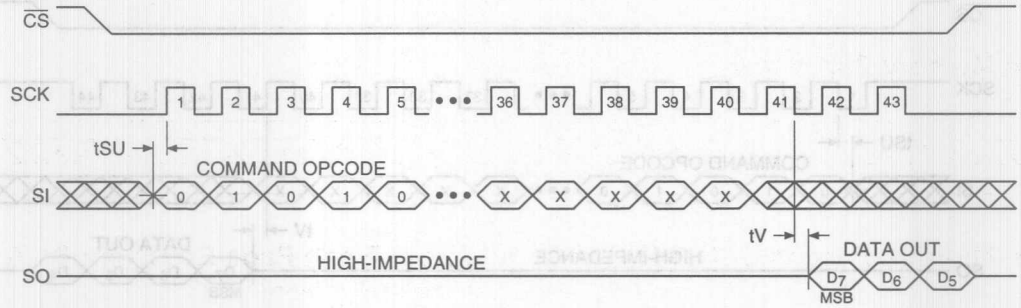
n = 1st byte read
n+1 = 2nd byte read

Detailed Bit-Level Read Timing – Inactive Clock Polarity Low

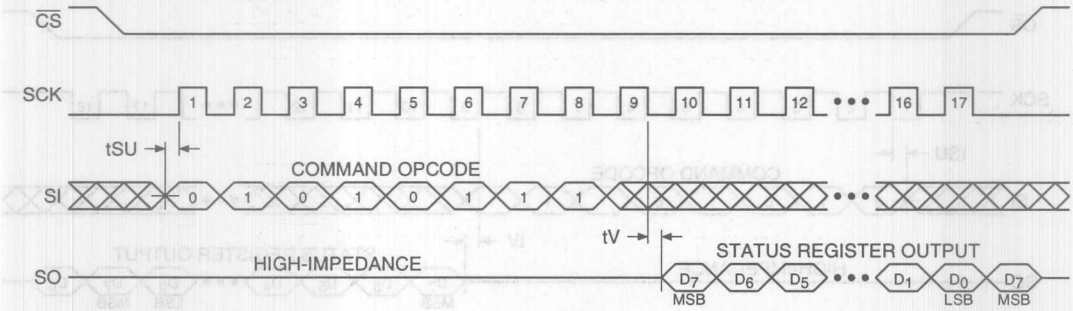
Main Memory Page Read



Buffer Read

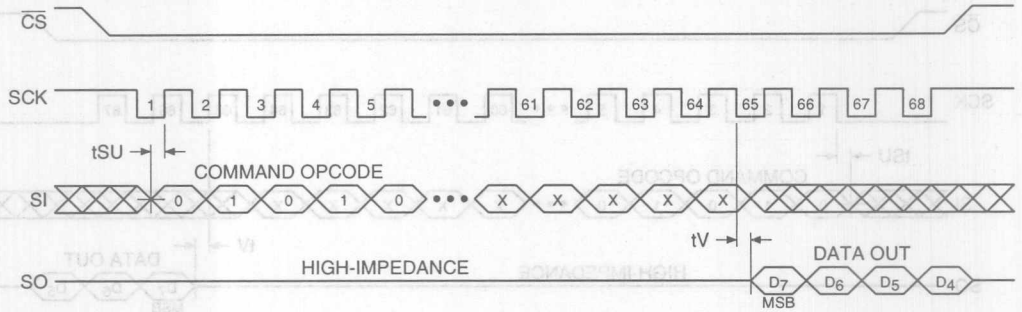


Status Register Read

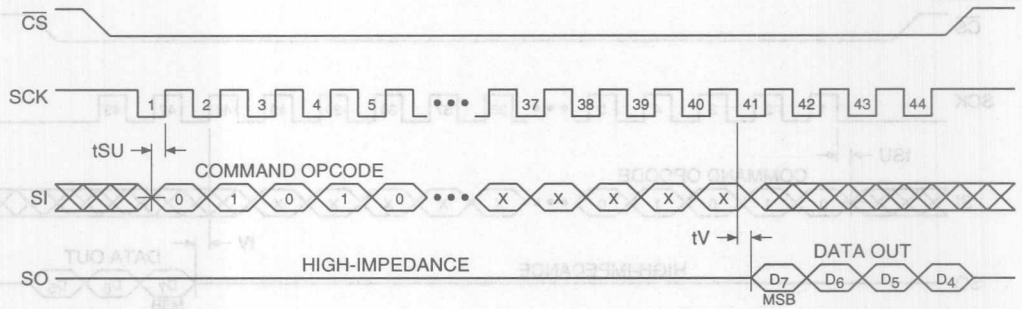


Detailed Bit-Level Read Timing – Inactive Clock Polarity High

Main Memory Page Read



Buffer Read



Status Register Read

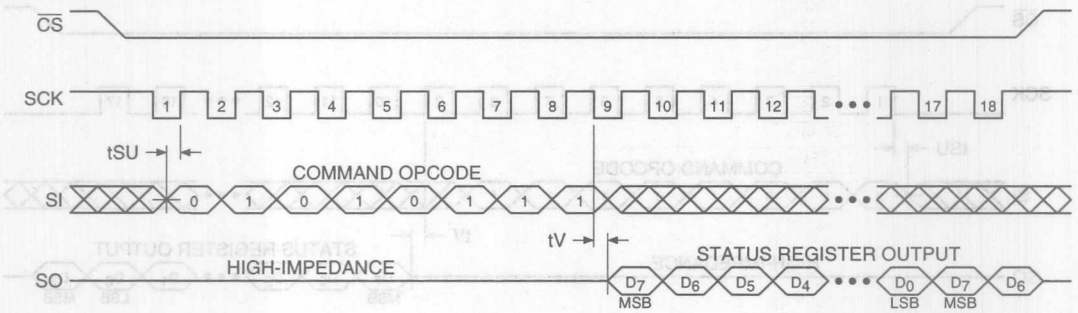


Table 1.

Main Memory Page Read	Buffer 1 Read	Buffer 2 Read	Main Memory Page to Buffer 1 Transfer	Main Memory Page to Buffer 2 Transfer	Main Memory Page to Buffer 1 Compare	Main Memory Page to Buffer 2 Compare	Buffer 1 Write	Buffer 2 Write
Opcode								
52H	54H	56H	53H	55H	60H	61H	84H	87H
0	0	0	0	0	0	0	1	1
1	1	1	1	1	1	1	0	0
0	0	0	0	0	1	1	0	0
1	1	1	1	1	0	0	0	0
0	0	0	0	0	0	0	0	0
0	1	1	0	1	0	0	1	1
1	0	1	1	0	0	0	0	1
0	0	0	1	1	0	1	0	1
r	X	X	r	r	r	r	X	X
PA12	X	X	PA12	PA12	PA12	PA12	X	X
PA11	X	X	PA11	PA11	PA11	PA11	X	X
PA10	X	X	PA10	PA10	PA10	PA10	X	X
PA9	X	X	PA9	PA9	PA9	PA9	X	X
PA8	X	X	PA8	PA8	PA8	PA8	X	X
PA7	X	X	PA7	PA7	PA7	PA7	X	X
PA6	X	X	PA6	PA6	PA6	PA6	X	X
PA5	X	X	PA5	PA5	PA5	PA5	X	X
PA4	X	X	PA4	PA4	PA4	PA4	X	X
PA3	X	X	PA3	PA3	PA3	PA3	X	X
PA2	X	X	PA2	PA2	PA2	PA2	X	X
PA1	X	X	PA1	PA1	PA1	PA1	X	X
PA0	X	X	PA0	PA0	PA0	PA0	X	X
BA9	BFA9	BFA9	X	X	X	X	BFA9	BFA9
BA8	BFA8	BFA8	X	X	X	X	BFA8	BFA8
BA7	BFA7	BFA7	X	X	X	X	BFA7	BFA7
BA6	BFA6	BFA6	X	X	X	X	BFA6	BFA6
BA5	BFA5	BFA5	X	X	X	X	BFA5	BFA5
BA4	BFA4	BFA4	X	X	X	X	BFA4	BFA4
BA3	BFA3	BFA3	X	X	X	X	BFA3	BFA3
BA2	BFA2	BFA2	X	X	X	X	BFA2	BFA2
BA1	BFA1	BFA1	X	X	X	X	BFA1	BFA1
BA0	BFA0	BFA0	X	X	X	X	BFA0	BFA0
X	X	X						
X	X	X						
X	X	X						
X	X	X						
X	X	X						
X	X	X						
X	X	X						
X	X	X						
•								
•								
•								
X (64th bit)								

X (Don't Care)
r (reserved bits)

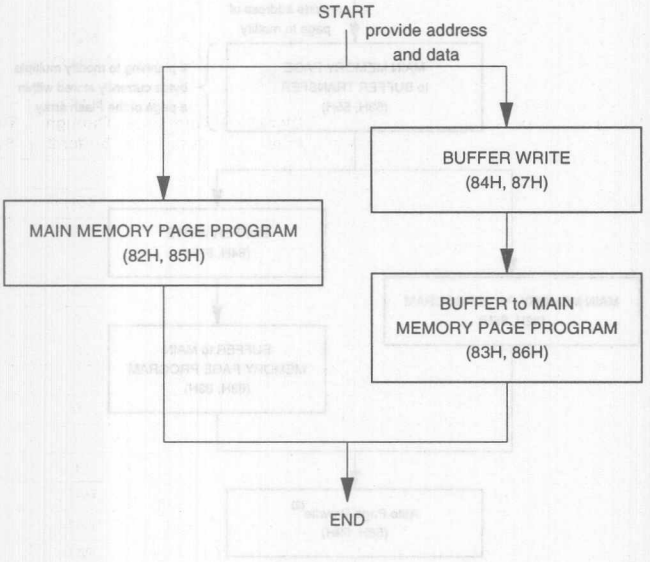
4

Table 2.

Buffer 1 to Main Memory Page Program with Built In Erase	Buffer 2 to Main Memory Page Program with Built-In Erase	Buffer 1 to Main Memory Page Program without Built-In Erase	Buffer 2 to Main Memory Page Program without Built-In Erase	Page Erase	Block Erase	Main Memory Page Program Through Buffer 1	Main Memory Page Program Through Buffer 2	Auto Page Rewrite Through Buffer 1	Auto Page Rewrite Through Buffer 2	Status Register
Opcode										
83H	86H	88H	89H	81H	50H	82H	85H	58H	59H	57H
1	1	1	1	1	0	1	1	0	0	0
0	0	0	0	0	1	0	0	1	1	1
0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	1	0	0	1	1	1
0	0	1	1	0	0	0	0	1	1	0
0	1	0	0	0	0	0	1	0	0	1
1	1	0	0	0	0	1	0	0	0	1
1	0	0	1	1	0	0	1	0	1	1
r	r	r	r	r	r	r	r	r	r	
PA12	PA12	PA12	PA12	PA12	PA12	PA12	PA12	PA12	PA12	
PA11	PA11	PA11	PA11	PA11	PA11	PA11	PA11	PA11	PA11	
PA10	PA10	PA10	PA10	PA10	PA10	PA10	PA10	PA10	PA10	
PA9	PA9	PA9	PA9	PA9	PA9	PA9	PA9	PA9	PA9	
PA8	PA8	PA8	PA8	PA8	PA8	PA8	PA8	PA8	PA8	
PA7	PA7	PA7	PA7	PA7	PA7	PA7	PA7	PA7	PA7	
PA6	PA6	PA6	PA6	PA6	PA6	PA6	PA6	PA6	PA6	
PA5	PA5	PA5	PA5	PA5	PA5	PA5	PA5	PA5	PA5	
PA4	PA4	PA4	PA4	PA4	PA4	PA4	PA4	PA4	PA4	
PA3	PA3	PA3	PA3	PA3	PA3	PA3	PA3	PA3	PA3	
PA2	PA2	PA2	PA2	PA2	X	PA2	PA2	PA2	PA2	
PA1	PA1	PA1	PA1	PA1	X	PA1	PA1	PA1	PA1	
PA0	PA0	PA0	PA0	PA0	X	PA0	PA0	PA0	PA0	
X	X	X	X	X	X	BFA9	BFA9	X	X	
X	X	X	X	X	X	BFA8	BFA8	X	X	
X	X	X	X	X	X	BFA7	BFA7	X	X	
X	X	X	X	X	X	BFA6	BFA6	X	X	
X	X	X	X	X	X	BFA5	BFA5	X	X	
X	X	X	X	X	X	BFA4	BFA4	X	X	
X	X	X	X	X	X	BFA3	BFA3	X	X	
X	X	X	X	X	X	BFA2	BFA2	X	X	
X	X	X	X	X	X	BFA1	BFA1	X	X	
X	X	X	X	X	X	BFA0	BFA0	X	X	

X (Don't Care)
r (reserved bits)

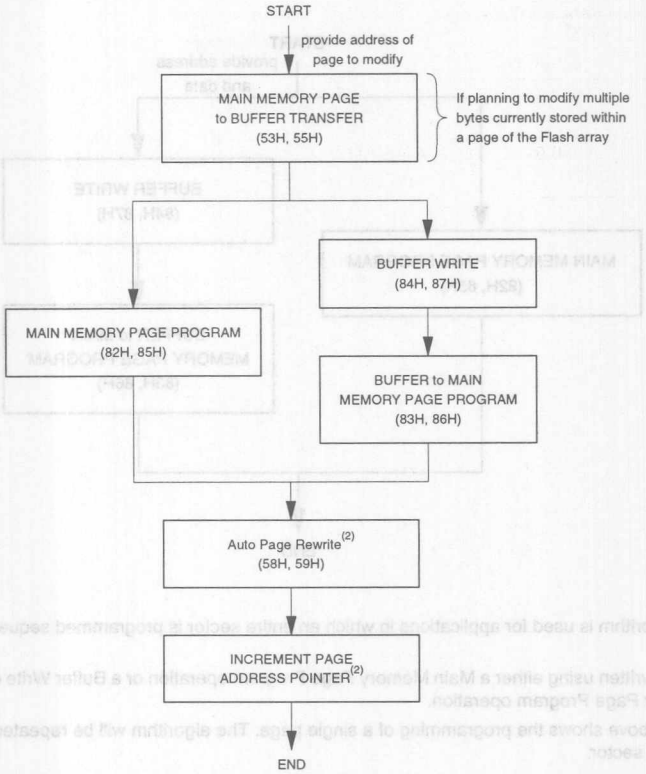
Figure 1. Algorithm for Programming or Reprogramming of an Entire Sector Sequentially



Notes:
1. This type of algorithm is used for applications in which an entire sector is programmed sequentially, filling the sector page-by-page.
2. A page can be written using either a Main Memory Page Program operation or a Buffer Write operation followed by a Buffer to Main Memory Page Program operation.
3. The algorithm above shows the programming of a single page. The algorithm will be repeated sequentially for each page within the entire sector.

4

Figure 2. Algorithm for Randomly Modifying Data



Notes:
1. To preserve data integrity, each page of a DataFlash sector must be updated/rewritten at least once within every 10,000 cumulative page erase/program operations within that sector.
2. A Page Address Pointer must be maintained to indicate which page is to be rewritten. The Auto Page Rewrite command must use the address specified by the Page Address Pointer.
3. Other algorithms can be used to rewrite portions of the Flash array. Low power applications may choose to wait until 10,000 cumulative page erase/program operations have accumulated before rewriting all pages of the sector. See application note AN-4 ("Using Atmel's Serial DataFlash") for more details.

Sector Addressing

PA12	PA11	PA10	PA9	PA8	PA7	PA6	PA5	PA4	PA3	Sector
0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	X	X	X	X	X	X	1
0	0	0	1	X	X	X	X	X	X	2
0	0	1	0	X	X	X	X	X	X	3
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
1	1	0	0	X	X	X	X	X	X	13
1	1	0	1	X	X	X	X	X	X	14
1	1	1	0	X	X	X	X	X	X	15
1	1	1	1	X	X	X	X	X	X	16

Ordering Information

f_{SCK} (MHz)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
13	10	0.01	AT45DB321-TC AT45DB321-CC	32T 24C3	Commercial (0°C to 70°C)
13	10	0.01	AT45DB321-TI AT45DB321-CI	32T 24C3	Industrial (-40°C to 85°C)

4

Package Type	
32T	32-Lead, Plastic Thin Small Outline Package (TSOP)
24C3	24-Ball, 5 x 5 Array Plastic Chip-Scale Ball Grid Array (CBGA)

Features

- Single 4.5V - 5.5V Supply
- Serial Interface Architecture
- Page Program Operation
  - Single Cycle Reprogram (Erase and Program)
  - 512 Pages (264 Bytes/Page) Main Memory
- Optional Page and Block Erase Operations
- One 264-Byte SRAM Data Buffer
- Internal Program and Control Timer
- Fast Page Program Time – 7 ms Typical
- 120 µs Typical Page to Buffer Transfer Time
- Low-Power Dissipation
  - 15 mA Active Read Current Typical
  - 10 µA CMOS Standby Current Typical
- 15 MHz Max Clock Frequency
- Hardware Data Protection Feature
- Serial Peripheral Interface (SPI) Compatible – Modes 0 and 3
- CMOS and TTL Compatible Inputs and Outputs
- Commercial and Industrial Temperature Ranges

Description

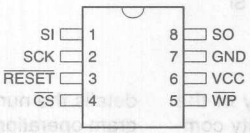
The AT45D011 is a 5.0-volt only, serial interface Flash memory suitable for in-system reprogramming. Its 1,081,344 bits of memory are organized as 512 pages of 264 bytes each. In addition to the main memory, the AT45D011 also contains one SRAM data buffer of 264 bytes. Unlike conventional Flash memories that are accessed randomly with multiple address lines and a parallel interface, the DataFlash uses a serial interface to sequentially access its data. The simple serial interface facilitates hard-

(continued)

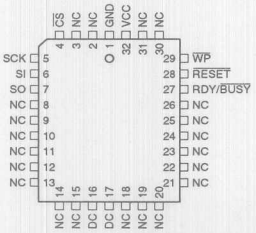
Pin Configurations

Pin Name	Function
$\overline{CS}$	Chip Select
SCK	Serial Clock
SI	Serial Input
SO	Serial Output
$\overline{WP}$	Hardware Page Write Protect Pin
$\overline{RESET}$	Chip Reset
RDY/$\overline{BUSY}$	Ready/Busy

SOIC



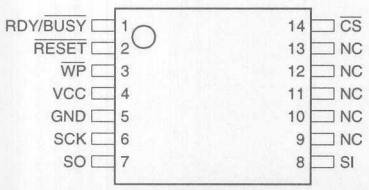
PLCC



Note: PLCC package pins 16 and 17 are DON'T CONNECT

TSSOP Top View

Type 1



1-Megabit 5.0-volt Only Serial DataFlash®

4

AT45D011 Preliminary

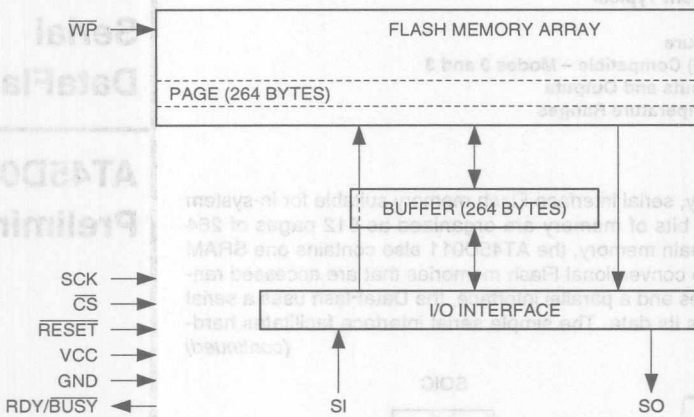
Rev. 1123A–08/98

ware layout, increases system reliability, minimizes switching noise, and reduces package size and active pin count. The device is optimized for use in many commercial and industrial applications where high density, low pin count, low voltage, and low power are essential. Typical applications for the DataFlash are digital voice storage, image storage, and data storage. The device operates at clock frequencies up to 15 MHz with a typical active read current consumption of 15 mA.

To allow for simple in-system reprogrammability, the AT45D011 does not require high input voltages for programming. The device operates from a single power supply, 4.5V to 5.5V, for both the program and read operations. The AT45D011 is enabled through the chip select pin ($\overline{CS}$) and accessed via a three-wire interface consisting of the Serial Input (SI), Serial Output (SO), and the Serial Clock (SCK).

All programming cycles are self-timed, and no separate erase cycle is required before programming.

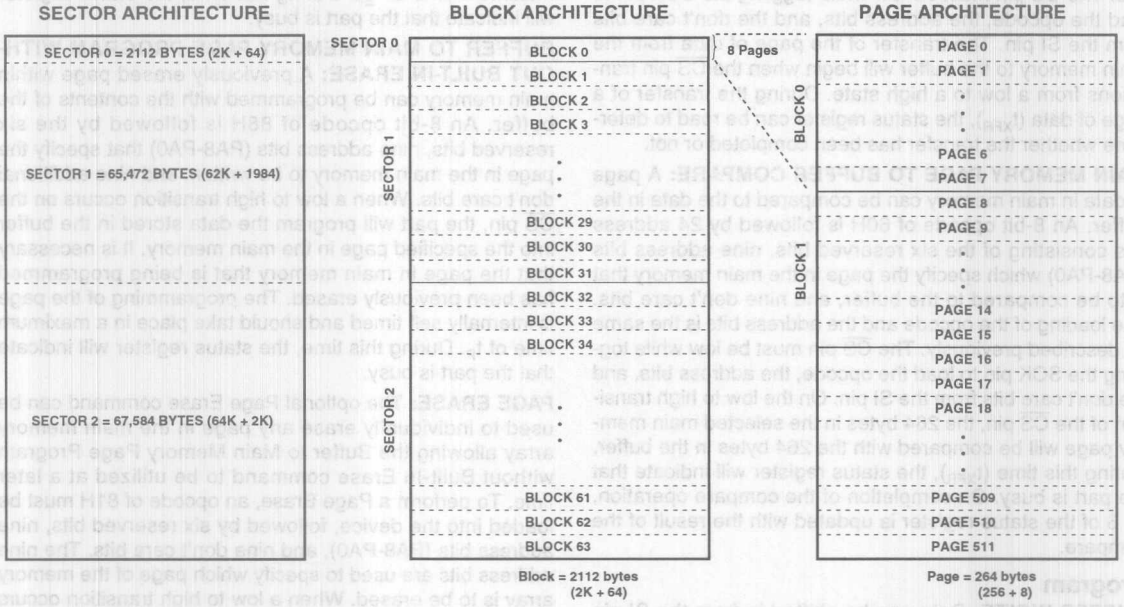
Block Diagram



Memory Array

To provide optimal flexibility, the memory array of the AT45D011 is divided into three levels of granularity comprising of sectors, blocks, and pages. The Memory Architecture Diagram illustrates the breakdown of each level and details the number of pages per sector and block. All program operations to the DataFlash occur on a page by page basis; however, the optional erase operations can be performed at the block or page level.

Memory Architecture Diagram



Device Operation

The device operation is controlled by instructions from the host processor. The list of instructions and their associated opcodes are contained in Table 1 and Table 2. A valid instruction starts with the falling edge of $\overline{CS}$ followed by the appropriate 8-bit opcode and the desired buffer or main memory address location. While the $\overline{CS}$ pin is low, toggling the SCK pin controls the loading of the opcode and the desired buffer or main memory address location through the SI (serial input) pin. All instructions, addresses, and data are transferred with the most significant bit (MSB) first.

Read

By specifying the appropriate opcode, data can be read from the main memory or from the data buffer.

MAIN MEMORY PAGE READ: A main memory read allows the user to read data directly from any one of the 512 pages in the main memory, bypassing the data buffer and leaving the contents of the buffer unchanged. To start a page read, the 8-bit opcode, 52H, is followed by 24 address bits and 32 don't care bits. In the AT45D011, the first six address bits are reserved for larger density devices (see Notes on page 10), the next nine address bits (PA8-PA0) specify the page address, and the next nine address bits (BA8-BA0) specify the starting byte address within the page. The 32 don't care bits which follow the 24 address bits are sent to initialize the read operation. Following the 32 don't care bits, additional pulses on SCK result in serial data being output on the SO (serial output) pin. The $\overline{CS}$ pin must remain low during the loading of the opcode, the address bits, and the reading of data. When the end of a page in main memory is reached during a main memory page read, the device will continue reading at the beginning of the same page. A low to high transition on the $\overline{CS}$ pin will terminate the read operation and tri-state the SO pin.

BUFFER READ: Data can be read from the data buffer using an opcode of 54H. To perform a buffer read, the eight bits of the opcode must be followed by 15 don't care bits, nine address bits, and eight don't care bits. Since the buffer size is 264-bytes, nine address bits (BFA8-BFA0) are required to specify the first byte of data to be read from the buffer. The $\overline{CS}$ pin must remain low during the loading of the opcode, the address bits, the don't care bits, and the reading of data. When the end of the buffer is reached, the device will continue reading back at the beginning of the buffer. A low to high transition on the $\overline{CS}$ pin will terminate the read operation and tri-state the SO pin.

MAIN MEMORY PAGE TO BUFFER TRANSFER: A page of data can be transferred from the main memory to buffer. An 8-bit opcode of 53H is followed by the six reserved bits, nine address bits (PA8-PA0) which specify the page in

main memory that is to be transferred, and nine don't care bits. The $\overline{CS}$ pin must be low while toggling the SCK pin to load the opcode, the address bits, and the don't care bits from the SI pin. The transfer of the page of data from the main memory to the buffer will begin when the $\overline{CS}$ pin transitions from a low to a high state. During the transfer of a page of data (t_{XFR}), the status register can be read to determine whether the transfer has been completed or not.

MAIN MEMORY PAGE TO BUFFER COMPARE: A page of data in main memory can be compared to the data in the buffer. An 8-bit opcode of 60H is followed by 24 address bits consisting of the six reserved bits, nine address bits (PA8-PA0) which specify the page in the main memory that is to be compared to the buffer, and nine don't care bits. The loading of the opcode and the address bits is the same as described previously. The $\overline{CS}$ pin must be low while toggling the SCK pin to load the opcode, the address bits, and the don't care bits from the SI pin. On the low to high transition of the $\overline{CS}$ pin, the 264 bytes in the selected main memory page will be compared with the 264 bytes in the buffer. During this time (t_{XFR}), the status register will indicate that the part is busy. On completion of the compare operation, bit 6 of the status register is updated with the result of the compare.

Program

BUFFER WRITE: Data can be shifted in from the SI pin into the data buffer. To load data into the buffer, an 8-bit opcode of 84H is followed by 15 don't care bits and nine address bits (BFA8-BFA0). The nine address bits specify the first byte in the buffer to be written. The data is entered following the address bits. If the end of the data buffer is reached, the device will wrap around back to the beginning of the buffer. Data will continue to be loaded into the buffer until a low to high transition is detected on the $\overline{CS}$ pin.

BUFFER TO MAIN MEMORY PAGE PROGRAM WITH BUILT-IN ERASE: Data written into the buffer can be programmed into the main memory. An 8-bit opcode of 83H is followed by the six reserved bits, nine address bits (PA8-PA0) that specify the page in the main memory to be written, and nine additional don't care bits. When a low to high transition occurs on the $\overline{CS}$ pin, the part will first erase the selected page in main memory to all 1s and then program the data stored in the buffer into the specified page in the main memory. Both the erase and the programming of the page are internally self timed and should take place in a maximum time of t_{EP}. During this time, the status register will indicate that the part is busy.

BUFFER TO MAIN MEMORY PAGE PROGRAM WITHOUT BUILT-IN ERASE: A previously erased page within main memory can be programmed with the contents of the buffer. An 8-bit opcode of 88H is followed by the six reserved bits, nine address bits (PA8-PA0) that specify the page in the main memory to be written, and nine additional don't care bits. When a low to high transition occurs on the $\overline{CS}$ pin, the part will program the data stored in the buffer into the specified page in the main memory. It is necessary that the page in main memory that is being programmed has been previously erased. The programming of the page is internally self timed and should take place in a maximum time of t_P. During this time, the status register will indicate that the part is busy.

PAGE ERASE: The optional Page Erase command can be used to individually erase any page in the main memory array allowing the Buffer to Main Memory Page Program without Built-In Erase command to be utilized at a later time. To perform a Page Erase, an opcode of 81H must be loaded into the device, followed by six reserved bits, nine address bits (PA8-PA0), and nine don't care bits. The nine address bits are used to specify which page of the memory array is to be erased. When a low to high transition occurs on the $\overline{CS}$ pin, the part will erase the selected page to 1s. The erase operation is internally self-timed and should take place in a maximum time of t_{PE}. During this time, the status register will indicate that the part is busy.

BLOCK ERASE: A block of eight pages can be erased at one time allowing the Buffer to Main Memory Page Program without Built-In Erase command to be utilized to reduce programming times when writing large amounts of data to the device. To perform a Block Erase, an opcode of 50H must be loaded into the device, followed by six reserved bits, six address bits (PA8-PA3), and 12 don't care bits. The six address bits are used to specify which block of eight pages is to be erased. When a low to high transition occurs on the $\overline{CS}$ pin, the part will erase the selected block of eight pages to 1s. The erase operation is internally self-timed and should take place in a maximum time of t_{BE}. During this time, the status register will indicate that the part is busy.

Block Erase Addressing

PA8	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	Block
0	0	0	0	0	0	X	X	X	0
0	0	0	0	0	1	X	X	X	1
0	0	0	0	1	0	X	X	X	2
0	0	0	0	1	1	X	X	X	3
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
1	1	1	1	0	0	X	X	X	60
1	1	1	1	0	1	X	X	X	61
1	1	1	1	1	0	X	X	X	62
1	1	1	1	1	1	X	X	X	63

MAIN MEMORY PAGE PROGRAM: This operation is a combination of the Buffer Write and Buffer to Main Memory Page Program with Built-In Erase operations. Data is first shifted into the buffer from the SI pin and then programmed into a specified page in the main memory. An 8-bit opcode of 82H is followed by the six reserved bits and 18 address bits. The nine most significant address bits (PA8-PA0) select the page in the main memory where data is to be written, and the next nine address bits (BFA8-BFA0) select the first byte in the buffer to be written. After all address bits are shifted in, the part will take data from the SI pin and store it in the data buffer. If the end of the buffer is reached, the device will wrap around back to the beginning of the buffer. When there is a low to high transition on the $\overline{CS}$ pin, the part will first erase the selected page in main memory to all 1s and then program the data stored in the buffer into the specified page in the main memory. Both the erase and the programming of the page are internally self timed and should take place in a maximum of time t_{EP}. During this time, the status register will indicate that the part is busy.

AUTO PAGE REWRITE: This mode is only needed if multiple bytes within a page or multiple pages of data are modified in a random fashion. This mode is a combination of two operations: Main Memory Page to Buffer Transfer and Buffer to Main Memory Page Program with Built-In Erase. A page of data is first transferred from the main memory to the data buffer, and then the same data (from the buffer) is programmed back into its original page of main memory. An 8-bit opcode of 58H is followed by the six reserved bits, nine address bits (PA8-PA0) that specify the page in main memory to be rewritten, and nine additional don't care bits. When a low to high transition occurs on the $\overline{CS}$ pin, the part will first transfer data from the page in main memory to the buffer and then program the data from the buffer back into same page of main memory. The operation is internally self-timed and should take place in a maximum time of t_{EP}. During this time, the status register will indicate that the part is busy.

If a sector is programmed or reprogrammed sequentially page by page, then the programming algorithm shown in Figure 1 is recommended. Otherwise, if multiple bytes in a page or several pages are programmed randomly in a sector, then the programming algorithm shown in Figure 2 is recommended.

STATUS REGISTER: The status register can be used to determine the device's ready/busy status, the result of a Main Memory Page to Buffer Compare operation, or the device density. To read the status register, an opcode of 57H must be loaded into the device. After the last bit of the opcode is shifted in, the eight bits of the status register, starting with the MSB (bit 7), will be shifted out on the SO pin during the next eight clock cycles. The five most-significant bits of the status register will contain device information, while the remaining three least-significant bits are reserved for future use and will have undefined values. After bit 0 of the status register has been shifted out, the sequence will repeat itself (as long as $\overline{CS}$ remains low and SCK is being toggled) starting again with bit 7. The data in the status register is constantly updated, so each repeating sequence will output new data.

Ready/busy status is indicated using bit 7 of the status register. If bit 7 is a 1, then the device is not busy and is ready to accept the next command. If bit 7 is a 0, then the device is in a busy state. The user can continuously poll bit 7 of the status register by stopping SCK once bit 7 has been output. The status of bit 7 will continue to be output on the SO pin, and once the device is no longer busy, the state of SO will change from 0 to 1. There are eight operations which can cause the device to be in a busy state: Main Memory Page

to Buffer Transfer, Main Memory Page to Buffer Compare, Buffer to Main Memory Page Program with Built-In Erase, Buffer to Main Memory Page Program without Built-In Erase, Page Erase, Block Erase, Main Memory Page Program, and Auto Page Rewrite.

The result of the most recent Main Memory Page to Buffer Compare operation is indicated using bit 6 of the status register. If bit 6 is a 0, then the data in the main memory page matches the data in the buffer. If bit 6 is a 1, then at least one bit of the data in the main memory page does not match the data in the buffer.

The device density is indicated using bits 5, 4, and 3 of the status register. For the AT45D011, the three bits are 0, 0, and 1. The decimal value of these three binary bits does not equate to the device density; the three bits represent a combinational code relating to differing densities of Serial DataFlash devices, allowing a total of eight different density configurations.

HARDWARE PAGE WRITE PROTECT: If the $\overline{WP}$ pin is held low, the first 256 pages of the main memory cannot be reprogrammed. The only way to reprogram the first 256 pages is to first drive the protect pin high and then use the program commands previously mentioned. The $\overline{WP}$ pin is internally pulled high; therefore, in low pin count applications, connection of the $\overline{WP}$ pin is not necessary if this pin and feature will not be utilized. However, it is recommended that the $\overline{WP}$ pin be driven high externally whenever possible.

$\overline{RESET}$: A low state on the reset pin ($\overline{RESET}$) will terminate the operation in progress and reset the internal state machine to an idle state. The device will remain in the reset condition as long as a low level is present on the $\overline{RESET}$ pin. Normal operation can resume once the $\overline{RESET}$ pin is brought back to a high level.

The device incorporates an internal power-on reset circuit, so there are no restrictions on the $\overline{RESET}$ pin during power-on sequences. The $\overline{RESET}$ pin is also internally pulled high; therefore, in low pin count applications, connection of the $\overline{RESET}$ pin is not necessary if this pin and feature will not be utilized. However, it is recommended that the $\overline{RESET}$ pin be driven high externally whenever possible.

READY/$\overline{BUSY}$: This open drain output pin will be driven low when the device is busy in an internally self-timed operation. This pin, which is normally in a high state (through an external pull-up resistor), will be pulled low during programming operations, compare operations, and during page-to-buffer transfers.

The busy status indicates that the Flash memory array and the buffer cannot be accessed.

Power On/Reset State

When power is first applied to the device, or when recovering from a reset condition, the device will default to SPI mode 3. In addition, the SO pin will be in a high impedance state, and a high to low transition on the $\overline{CS}$ pin will be required to start a valid instruction. The SPI mode will be automatically selected on every falling edge of $\overline{CS}$ by sampling the inactive clock state.

Status Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RDY/$\overline{BUSY}$	COMP	0	0	1	X	X	X

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC and AC Operating Range

		AT45D011
Operating Temperature (Case)	Com.	0°C to 70°C
	Ind.	-40°C to 85°C
V_{CC} Power Supply[1]		4.5V to 5.5V

Note: 1. After power is applied and V_{CC} is at the minimum specified data sheet value, the system should wait 20 ms before an operational mode is started.

DC Characteristics

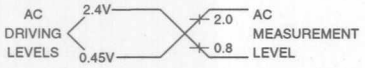
Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{SB}	Standby Current	$\overline{CS}$, $\overline{RESET}$, $\overline{WP}$ = V_{IH}, all inputs at CMOS levels		10	20	µA
I_{CC1}	Active Current, Read Operation	f = 15 MHz; I_{OUT} = 0 mA; V_{CC} = 5.5V		15	25	mA
I_{CC2}	Active Current, Program/Erase Operation	V_{CC} = 5.5V		25	50	mA
I_{LI}	Input Load Current	V_{IN} = CMOS levels			10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = CMOS levels			10	µA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage		2.0			V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			0.45	V
V_{OH1}	Output High Voltage	I_{OH} = -400 µA	2.4			V
V_{OH2}	Output High Voltage	I_{OH} = -100 µA; V_{CC} = 4.5V	4.2			V

4

AC Characteristics

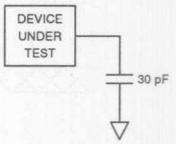
Symbol	Parameter	Min	Typ	Max	Units
f_{SCK}	SCK Frequency			15	MHz
t_{WH}	SCK High Time	30			ns
t_{WL}	SCK Low Time	30			ns
t_{CS}	Minimum $\overline{CS}$ High Time	250			ns
t_{CSS}	$\overline{CS}$ Setup Time	250			ns
t_{CSH}	$\overline{CS}$ Hold Time	250			ns
t_{CSB}	$\overline{CS}$ High to RDY/$\overline{BUSY}$ Low			200	ns
t_{SU}	Data In Setup Time	10			ns
t_H	Data In Hold Time	15			ns
t_{HO}	Output Hold Time	0			ns
t_{DIS}	Output Disable Time			20	ns
t_V	Output Valid			25	ns
t_{XFR}	Page to Buffer Transfer/Compare Time		120	200	µs
t_{EP}	Page Erase and Programming Time		10	20	ms
t_P	Page Programming Time		7	15	ms
t_{PE}	Page Erase Time		6	10	ms
t_{BE}	Block Erase Time		7	15	ms
t_{RST}	$\overline{RESET}$ Pulse Width	10			µs
t_{REC}	$\overline{RESET}$ Recovery Time			1	µs

Input Test Waveforms and Measurement Levels



t_R, t_F < 5 ns (10% to 90%)

Output Test Load

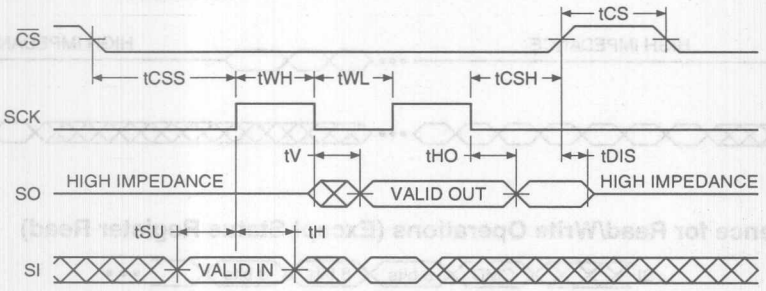


AC Waveforms

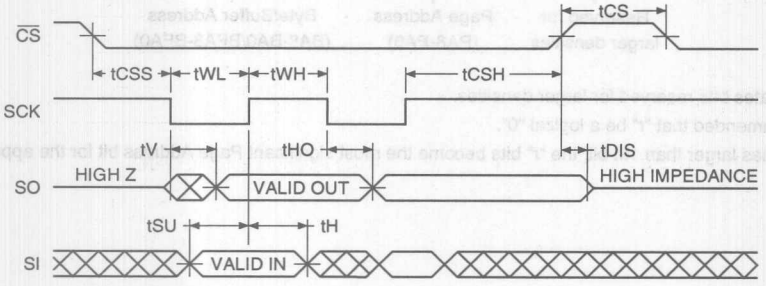
Two different timing diagrams are shown below. Waveform 1 shows the SCK signal being low when $\overline{CS}$ makes a high-to-low transition, and Waveform 2 shows the SCK signal being high when $\overline{CS}$ makes a high-to-low transition. Both waveforms show valid timing diagrams. The setup and hold times for the SI signal are referenced to the low-to-high transition on the SCK signal.

Waveform 1 shows timing that is also compatible with SPI Mode 0, and Waveform 2 shows timing that is compatible with SPI Mode 3.

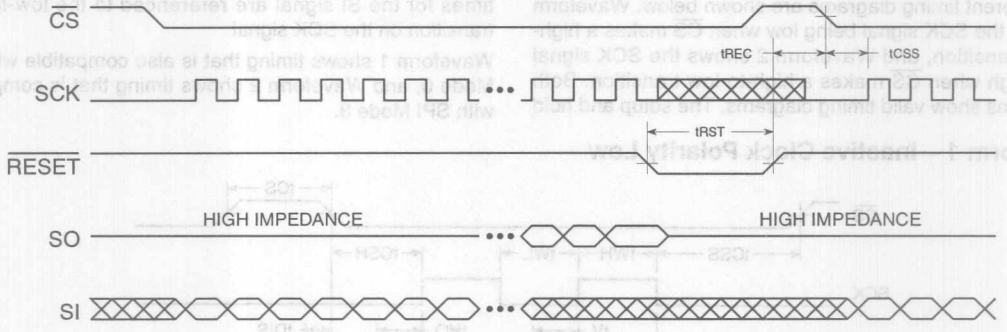
Waveform 1 – Inactive Clock Polarity Low



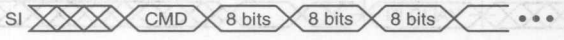
Waveform 2 – Inactive Clock Polarity High

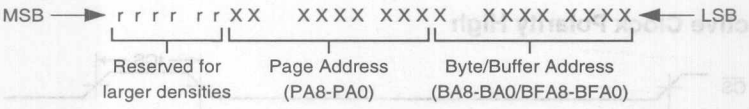


Reset Timing (Inactive Clock Polarity Low Shown)



Command Sequence for Read/Write Operations (Except Status Register Read)

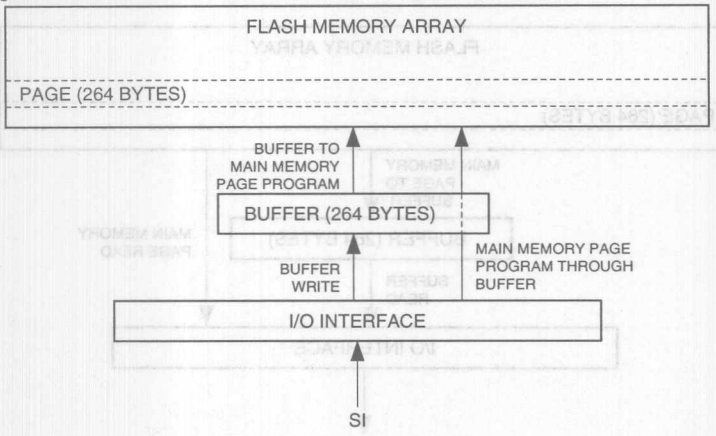




Notes:
1. "r" designates bits reserved for larger densities.
2. It is recommended that "r" be a logical "0".
3. For densities larger than 1M bit, the "r" bits become the most significant Page Address bit for the appropriate density.

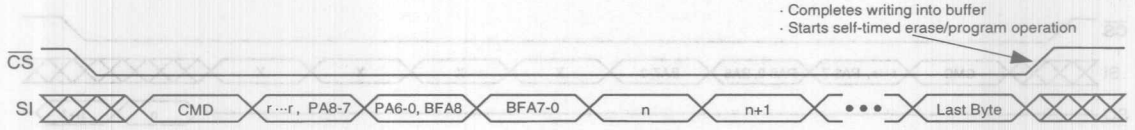
Write Operations

The following block diagram and waveforms illustrate the various write sequences available.

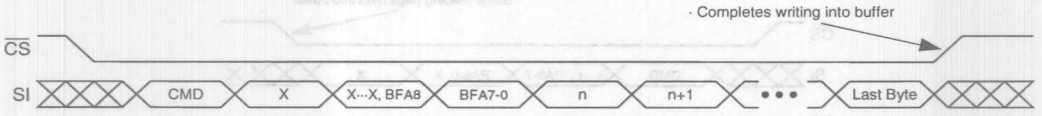


4

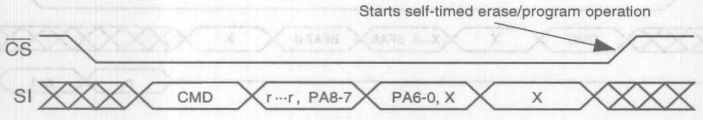
Main Memory Page Program through Buffer

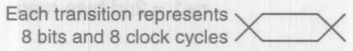


Buffer Write



Buffer to Main Memory Page Program (Data from Buffer Programmed into Flash Page)

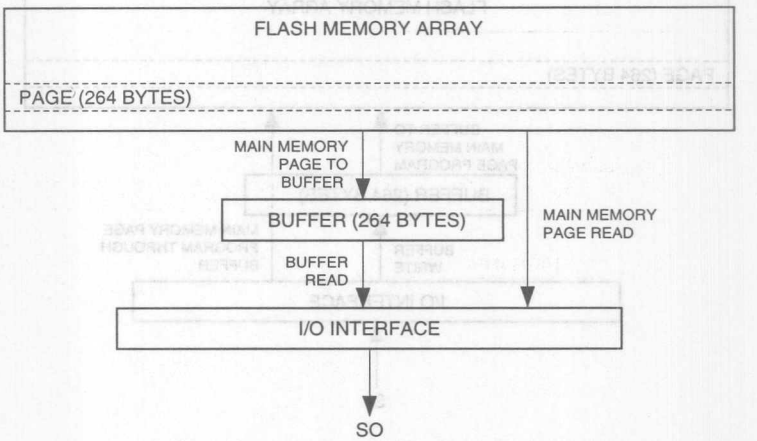




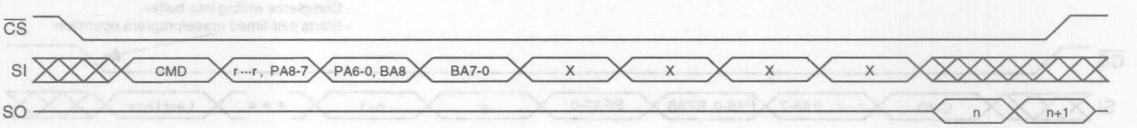
n = 1st byte written
n+1 = 2nd byte written

Read Operations

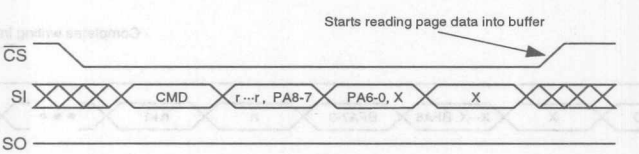
The following block diagram and waveforms illustrate the various read sequences available.



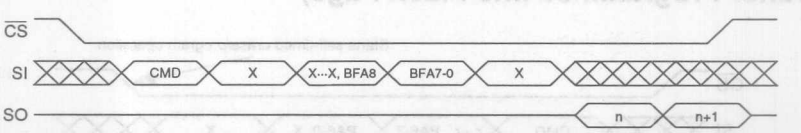
Main Memory Page Read



Main Memory Page to Buffer Transfer (Data from Flash Page Read into Buffer)



Buffer Read

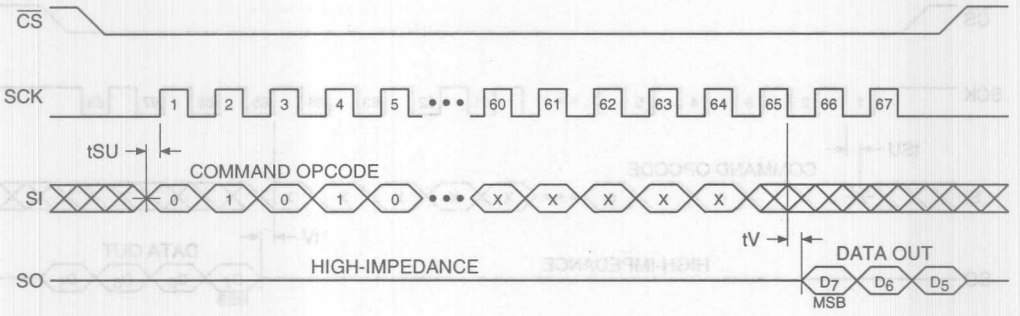


Each transition represents 8 bits and 8 clock cycles

n = 1st byte read
n+1 = 2nd byte read

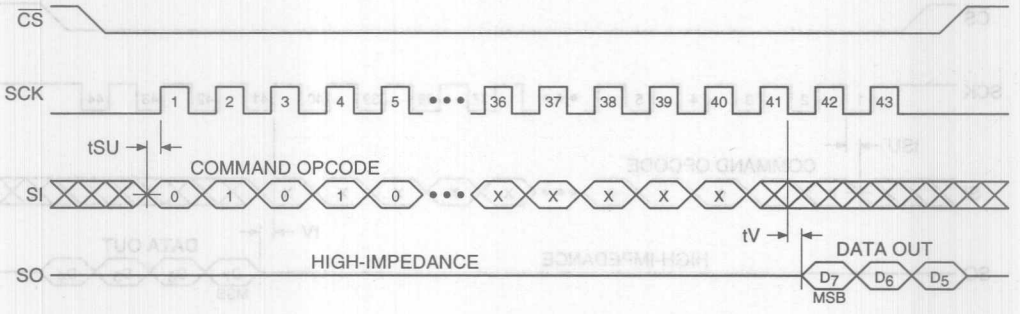
Detailed Bit-Level Read Timing – Inactive Clock Polarity Low

Main Memory Page Read

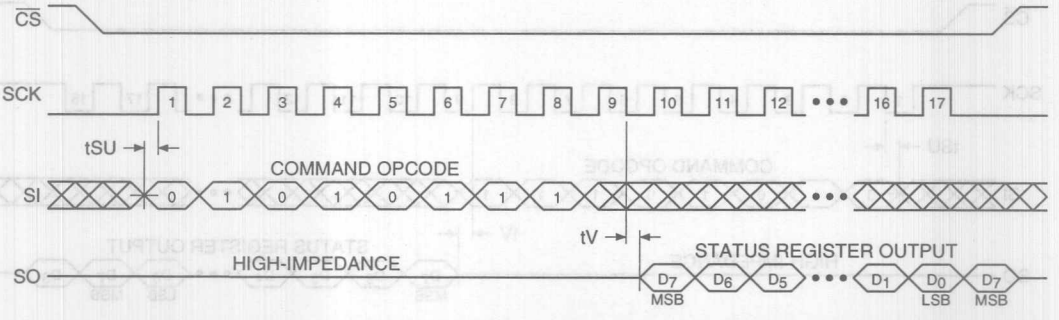


4

Buffer Read

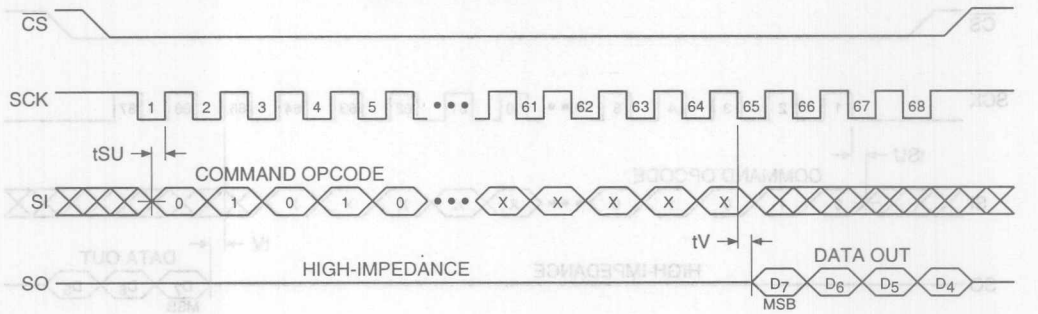


Status Register Read

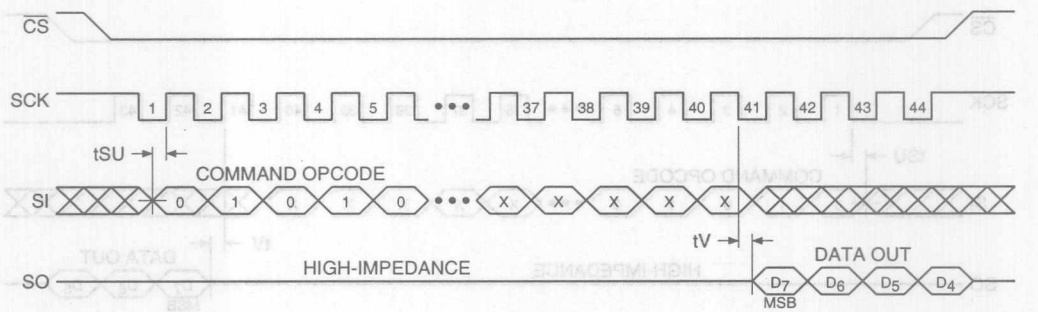


Detailed Bit-Level Read Timing – Inactive Clock Polarity High

Main Memory Page Read



Buffer Read



Status Register Read

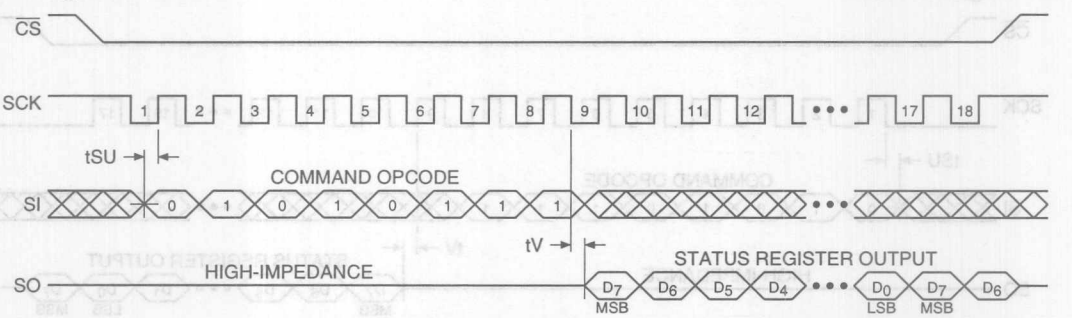


Table 1.

Main Memory Page Read	Buffer Read	Main Memory Page to Buffer Transfer	Main Memory Page to Buffer Compare	Buffer Write
Opcode				
52H	54H	53H	60H	84H
0	0	0	0	1
1	1	1	1	0
0	0	0	1	0
1	1	1	0	0
0	0	0	0	0
0	1	0	0	1
1	0	1	0	0
0	0	1	0	0
r	X	r	r	X
r	X	r	r	X
r	X	r	r	X
r	X	r	r	X
r	X	r	r	X
r	X	r	r	X
PA8	X	PA8	PA8	X
PA7	X	PA7	PA7	X
PA6	X	PA6	PA6	X
PA5	X	PA5	PA5	X
PA4	X	PA4	PA4	X
PA3	X	PA3	PA3	X
PA2	X	PA2	PA2	X
PA1	X	PA1	PA1	X
PA0	X	PA0	PA0	X
BA8	BFA8	X	X	BFA8
BA7	BFA7	X	X	BFA7
BA6	BFA6	X	X	BFA6
BA5	BFA5	X	X	BFA5
BA4	BFA4	X	X	BFA4
BA3	BFA3	X	X	BFA3
BA2	BFA2	X	X	BFA2
BA1	BFA1	X	X	BFA1
BA0	BFA0	X	X	BFA0
X	X			
X	X			
X	X			
X	X			
X	X			
X	X			
X	X			
X	X			
•				
•				
•				
X (64th bit)				

X (Don't Care)
r (reserved bits)

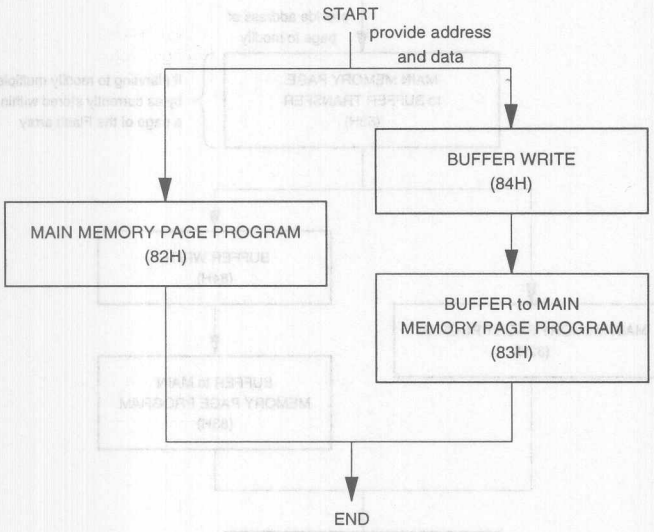
4

Table 2.

Buffer to Main Memory Page Program with Built-In Erase	Buffer to Main Memory Page Program without Built-In Erase	Page Erase	Block Erase	Main Memory Page Program Through Buffer	Auto Page Rewrite Through Buffer	Status Register
Opcode						
83H	88H	81H	50H	82H	58H	57H
1	1	1	0	1	0	0
0	0	0	1	0	1	1
0	0	0	0	0	0	0
0	0	0	1	0	1	1
0	1	0	0	0	1	0
0	0	0	0	0	0	1
1	0	0	0	1	0	1
1	0	1	0	0	0	1
r	r	r	r	r	r	
r	r	r	r	r	r	
r	r	r	r	r	r	
r	r	r	r	r	r	
r	r	r	r	r	r	
r	r	r	r	r	r	
PA8	PA8	PA8	PA8	PA8	PA8	
PA7	PA7	PA7	PA7	PA7	PA7	
PA6	PA6	PA6	PA6	PA6	PA6	
PA5	PA5	PA5	PA5	PA5	PA5	
PA4	PA4	PA4	PA4	PA4	PA4	
PA3	PA3	PA3	PA3	PA3	PA3	
PA2	PA2	PA2	X	PA2	PA2	
PA1	PA1	PA1	X	PA1	PA1	
PA0	PA0	PA0	X	PA0	PA0	
X	X	X	X	BFA8	X	
X	X	X	X	BFA7	X	
X	X	X	X	BFA6	X	
X	X	X	X	BFA5	X	
X	X	X	X	BFA4	X	
X	X	X	X	BFA3	X	
X	X	X	X	BFA2	X	
X	X	X	X	BFA1	X	
X	X	X	X	BFA0	X	

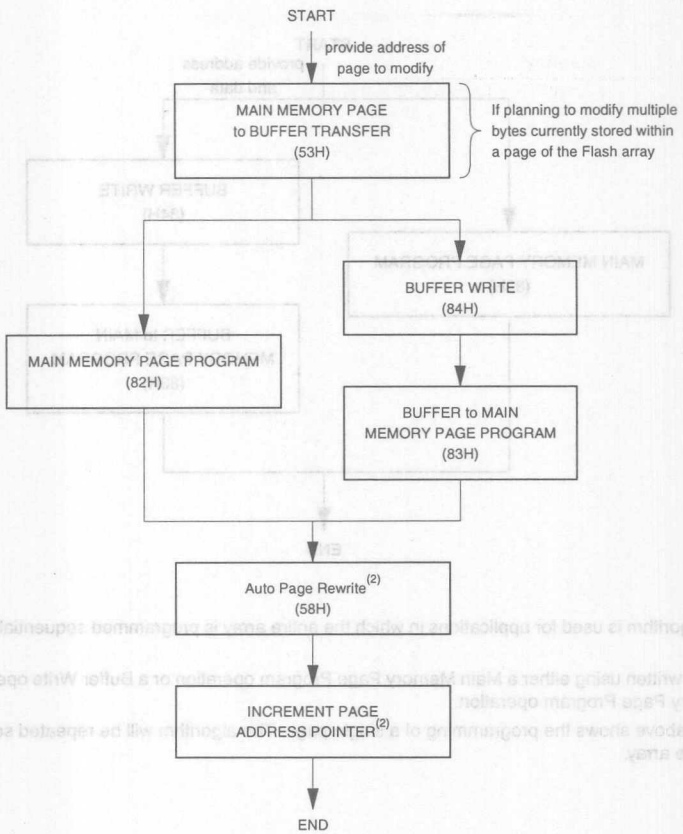
X (Don't Care) r (reserved bits)

Figure 1. Algorithm for Programming or Reprogramming of the Entire Array Sequentially



Notes:
1. This type of algorithm is used for applications in which the entire array is programmed sequentially, filling the array page-by-page.
2. A page can be written using either a Main Memory Page Program operation or a Buffer Write operation followed by a Buffer to Main Memory Page Program operation.
3. The algorithm above shows the programming of a single page. The algorithm will be repeated sequentially for each page within the entire array.

Figure 2. Algorithm for Randomly Modifying Data



Notes:
1. To preserve data integrity, each page of a DataFlash sector must be updated/rewritten at least once within every 10,000 cumulative page erase/program operations within that sector.
2. A Page Address Pointer must be maintained to indicate which page is to be rewritten. The Auto Page Rewrite command must use the address specified by the Page Address Pointer.
3. Other algorithms can be used to rewrite portions of the Flash array. Low power applications may choose to wait until 10,000 cumulative page erase/program operations have accumulated before rewriting all pages of the sector. See application note AN-4 ("Using Atmel's Serial DataFlash") for more details.

Sector Addressing

PA8	PA7	PA6	PA5	PA4	PA3	PA2-PA0	Sector
0	0	0	0	0	0	X	0
0	X	X	X	X	X	X	1
1	X	X	X	X	X	X	2

Ordering Information

f_{SCK} (MHz)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
15	25	0.02	AT45D011-JC AT45D011-SC AT45D011-XC	32J 8S2 14X	Commercial (0°C to 70°C)
15	25	0.02	AT45D011-JI AT45D011-SI AT45D011-XI	32J 8S2 14X	Industrial (-40°C to 85°C)

4

Package Type	
32J	32-Lead, Plastic J-Leaded Chip Carrier (PLCC)
8S2	8-Lead, 0.210" Wide, Plastic Gull Wing Small Outline (EIAJ SOIC)
14X	14-Lead, 0.170" Wide, Plastic Thin Shrink Small Outline Package (TSSOP)

Features

- Single 4.5V - 5.5V Supply
- Serial Interface Architecture
- Page Program Operation
  - Single Cycle Reprogram (Erase and Program)
  - 1024 Pages (264 Bytes/Page) Main Memory
- Two 264-Byte SRAM Data Buffers – Allows Receiving of Data while Reprogramming of Nonvolatile Memory
- Internal Program and Control Timer
- Fast Page Program Time – 7 ms Typical
- 80 µs Typical Page to Buffer Transfer Time
- Low Power Dissipation
  - 15 mA Active Read Current Typical
  - 15 µA CMOS Standby Current Typical
- 10 MHz Max Clock Frequency
- Hardware Data Protection Feature
- Serial Peripheral Interface (SPI) Compatible – Modes 0 and 3
- CMOS and TTL Compatible Inputs and Outputs
- Commercial and Industrial Temperature Ranges

2-Megabit 5-volt Only Serial DataFlash®

4

AT45D021

Description

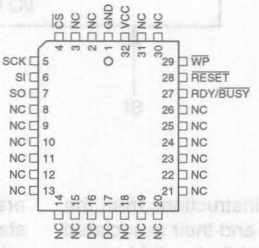
The AT45D021 is a 5-volt only, serial interface Flash memory suitable for in-system reprogramming. Its 2,162,688 bits of memory are organized as 1024 pages of 264-bytes each. In addition to the main memory, the AT45D021 also contains two data SRAM buffers of 264-bytes each. The buffers allow receiving of data while a page in

(continued)

Pin Configurations

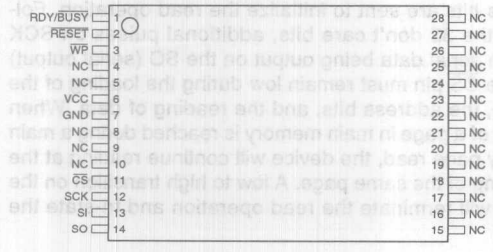
Pin Name	Function
CS	Chip Select
SCK	Serial Clock
SI	Serial Input
SO	Serial Output
WP	Harware Page Write Protect Pin
$\overline{\text{RESET}}$	Chip Reset
RDY/$\overline{\text{BUSY}}$	Ready/Busy

PLCC

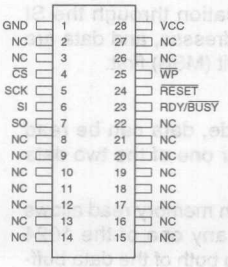


Note: PLCC package pins 16 and 17 are DON'T CONNECT.

TSOP Top View
Type 1



SOIC



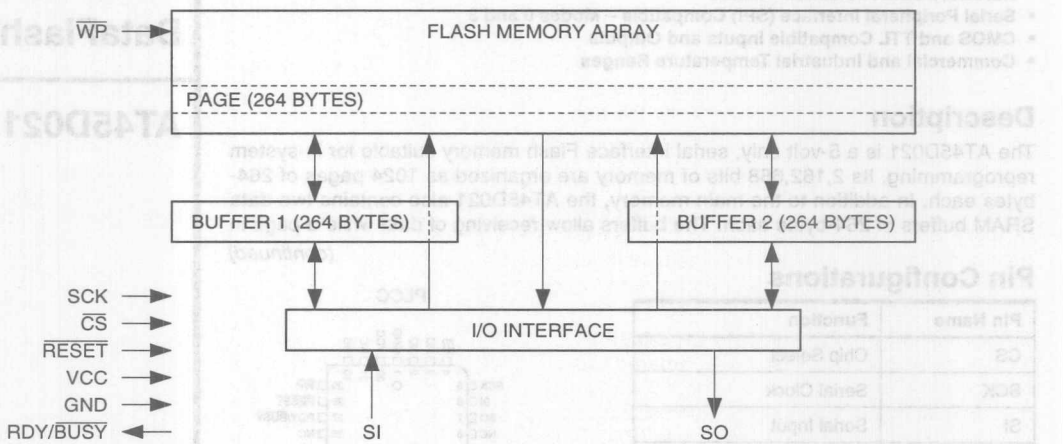
Rev. 0869B–10/98

the main memory is being reprogrammed. Unlike conventional Flash memories that are accessed randomly with multiple address lines and a parallel interface, the DataFlash uses a serial interface to sequentially access its data. The simple serial interface facilitates hardware layout, increases system reliability, minimizes switching noise, and reduces package size and active pin count. The device is optimized for use in many commercial and industrial applications where high density, low pin count, low voltage, and low power are essential. Typical applications for the DataFlash are digital voice storage, image storage, and data storage. The device operates at clock frequencies up to 10 MHz with a typical active read current consumption of 15 mA.

To allow for simple in-system reprogrammability, the AT45D021 does not require high input voltages for programming. The device operates from a single power supply, 4.5V to 5.5V, for both the program and read operations. The AT45D021 is enabled through the chip select pin ($\overline{CS}$) and accessed via a three-wire interface consisting of the Serial Input (SI), Serial Output (SO), and the Serial Clock (SCK).

All programming cycles are self-timed, and no separate erase cycle is required before programming.

Block Diagram



Device Operation

The device operation is controlled by instructions from the host processor. The list of instructions and their associated opcodes are contained in Tables 1 and 2. A valid instruction starts with the falling edge of $\overline{CS}$ followed by the appropriate 8-bit opcode and the desired buffer or main memory address location. While the $\overline{CS}$ pin is low, toggling the SCK pin controls the loading of the opcode and the desired buffer or main memory address location through the SI (serial input) pin. All instructions, addresses, and data are transferred with the most significant bit (MSB) first.

Read

By specifying the appropriate opcode, data can be read from the main memory or from either one of the two data buffers.

MAIN MEMORY PAGE READ: A main memory read allows the user to read data directly from any one of the 1024 pages in the main memory, bypassing both of the data buffers and leaving the contents of the buffers unchanged. To start a page read, the 8-bit opcode, 52H, is followed by 24 address bits and 32 don't care bits. In the AT45D021, the first five address bits are reserved for larger density devices (see Notes on page 160), the next 10 address bits (PA9-PA0) specify the page address, and the next nine address bits (BA8-BA0) specify the starting byte address within the page. The 32 don't care bits which follow the 24 address bits are sent to initialize the read operation. Following the 32 don't care bits, additional pulses on SCK result in serial data being output on the SO (serial output) pin. The $\overline{CS}$ pin must remain low during the loading of the opcode, the address bits, and the reading of data. When the end of a page in main memory is reached during a main memory page read, the device will continue reading at the beginning of the same page. A low to high transition on the $\overline{CS}$ pin will terminate the read operation and tri-state the SO pin.

BUFFER READ: Data can be read from either one of the two buffers, using different opcodes to specify which buffer to read from. An opcode of 54H is used to read data from buffer 1, and an opcode of 56H is used to read data from buffer 2. To perform a buffer read, the eight bits of the opcode must be followed by 15 don't care bits, nine address bits, and eight don't care bits. Since the buffer size is 264-bytes, nine address bits (BFA8-BFA0) are required to specify the first byte of data to be read from the buffer. The $\overline{CS}$ pin must remain low during the loading of the opcode, the address bits, the don't care bits, and the reading of data. When the end of a buffer is reached, the device will continue reading back at the beginning of the buffer. A low to high transition on the $\overline{CS}$ pin will terminate the read operation and tri-state the SO pin.

MAIN MEMORY PAGE TO BUFFER TRANSFER: A page of data can be transferred from the main memory to either buffer 1 or buffer 2. An 8-bit opcode, 53H for buffer 1 and 55H for buffer 2, is followed by the five reserved bits, 10 address bits (PA9-PA0) which specify the page in main memory that is to be transferred, and nine don't care bits. The $\overline{CS}$ pin must be low while toggling the SCK pin to load the opcode, the address bits, and the don't care bits from the SI pin. The transfer of the page of data from the main memory to the buffer will begin when the $\overline{CS}$ pin transitions from a low to a high state. During the transfer of a page of data (t_{XFR}), the status register can be read to determine whether the transfer has been completed or not.

MAIN MEMORY PAGE TO BUFFER COMPARE: A page of data in main memory can be compared to the data in buffer 1 or buffer 2. An 8-bit opcode, 60H for buffer 1 and 61H for buffer 2, is followed by 24 address bits consisting of the five reserved bits, 10 address bits (PA9-PA0) which specify the page in the main memory that is to be compared to the buffer, and nine don't care bits. The loading of the opcode and the address bits is the same as described previously. The $\overline{CS}$ pin must be low while toggling the SCK pin to load the opcode, the address bits, and the don't care bits from the SI pin. On the low to high transition of the $\overline{CS}$ pin, the 264 bytes in the selected main memory page will be compared with the 264 bytes in buffer 1 or buffer 2. During this time (t_{XFR}), the status register will indicate that the part is busy. On completion of the compare operation, bit 6 of the status register is updated with the result of the compare.

Program

BUFFER WRITE: Data can be shifted in from the SI pin into either buffer 1 or buffer 2. To load data into either buffer, an 8-bit opcode, 84H for buffer 1 or 87H for buffer 2, is followed by 15 don't care bits and nine address bits (BFA8-BFA0). The nine address bits specify the first byte in the buffer to be written. The data is entered following the address bits. If the end of the data buffer is reached, the device will wrap around back to the beginning of the buffer. Data will continue to be loaded into the buffer until a low to high transition is detected on the $\overline{CS}$ pin.

BUFFER TO MAIN MEMORY PAGE PROGRAM WITH BUILT-IN ERASE: Data written into either buffer 1 or buffer 2 can be programmed into the main memory. An 8-bit opcode, 83H for buffer 1 or 86H for buffer 2, is followed by the five reserved bits, 10 address bits (PA9-PA0) that specify the page in the main memory to be written, and nine additional don't care bits. When a low to high transition occurs on the $\overline{CS}$ pin, the part will first erase the selected page in main memory to all 1s and then program the data stored in the buffer into the specified page in the main memory. Both the erase and the programming of the page are internally self timed and should take place in a maximum time of t_{EP}. During this time, the status register will indicate that the part is busy.

BUFFER TO MAIN MEMORY PAGE PROGRAM WITHOUT BUILT-IN ERASE: A previously erased page within main memory can be programmed with the contents of either buffer 1 or buffer 2. An 8-bit opcode, 88H for buffer 1 or 89H for buffer 2, is followed by the five reserved bits, 10 address bits (PA9-PA0) that specify the page in the main memory to be written, and nine additional don't care bits. When a low to high transition occurs on the $\overline{CS}$ pin, the part will program the data stored in the buffer into the specified page in the main memory. It is necessary that the page in main memory that is being programmed has been previously programmed to all 1s (erased state). The programming of the page is internally self timed and should take place in a maximum time of t_P. During this time, the status register will indicate that the part is busy.

MAIN MEMORY PAGE PROGRAM: This operation is a combination of the Buffer Write and Buffer to Main Memory Page Program with Built-In Erase operations. Data is first shifted into buffer 1 or buffer 2 from the SI pin and then programmed into a specified page in the main memory. An 8-bit opcode, 82H for buffer 1 or 85H for buffer 2, is followed by the five reserved bits and 19 address bits. The 10 most significant address bits (PA9-PA0) select the page in the main memory where data is to be written, and the next nine address bits (BFA8-BFA0) select the first byte in the buffer to be written. After all address bits are shifted in, the part will take data from the SI pin and store it in one of the data buffers. If the end of the buffer is reached, the device will wrap around back to the beginning of the buffer. When there is a low to high transition on the $\overline{CS}$ pin, the part will first erase the selected page in main memory to all 1s and then program the data stored in the buffer into the specified page in the main memory. Both the erase and the programming of the page are internally self timed and should take place in a maximum of time t_{EP}. During this time, the status register will indicate that the part is busy.

AUTO PAGE REWRITE: This mode is only needed if multiple bytes within a page or multiple pages of data are modified in a random fashion. This mode is a combination of two operations: Main Memory Page to Buffer Transfer and Buffer to Main Memory Page Program with Built-In Erase. A page of data is first transferred from the main memory to buffer 1 or buffer 2, and then the same data (from buffer 1 or buffer 2) is programmed back into its original page of main memory. An 8-bit opcode, 58H for buffer 1 or 59H for buffer 2, is followed by the five reserved bits, 10 address bits (PA9-PA0) that specify the page in main memory to be rewritten, and nine additional don't care bits. When a low to high transition occurs on the $\overline{CS}$ pin, the part will first transfer data from the page in main memory to a buffer and then program the data from the buffer back into same page of main memory. The operation is internally self-timed and should take place in a maximum time of t_{EP}. During this time, the status register will indicate that the part is busy.

If the main memory is programmed or reprogrammed sequentially page by page, then the programming algorithm shown in Figure 1 is recommended. Otherwise, if multiple bytes in a page or several pages are programmed randomly in the main memory, then the programming algorithm shown in Figure 2 is recommended.

STATUS REGISTER: The status register can be used to determine the device's ready/busy status, the result of a Main Memory Page to Buffer Compare operation, or the device density. To read the status register, an opcode of 57H must be loaded into the device. After the last bit of the opcode is shifted in, the eight bits of the status register, starting with the MSB (bit 7), will be shifted out on the SO pin during the next eight clock cycles. The five most-significant bits of the status register will contain device information, while the remaining three least-significant bits are reserved for future use and will have undefined values. After bit 0 of the status register has been shifted out, the sequence will repeat itself (as long as $\overline{CS}$ remains low and SCK is being toggled) starting again with bit 7. The data in the status register is constantly updated, so each repeating sequence will output new data.

Ready/busy status is indicated using bit 7 of the status register. If bit 7 is a 1, then the device is not busy and is ready to accept the next command. If bit 7 is a 0, then the device is in a busy state. The user can continuously poll bit 7 of the status register by stopping SCK once bit 7 has been output. The status of bit 7 will continue to be output on the SO pin, and once the device is no longer busy, the state of SO will change from 0 to 1. There are six operations which can cause the device to be in a busy state: Main Memory Page to Buffer Transfer, Main Memory Page to Buffer Compare, Buffer to Main Memory Page Program with Built-In Erase, Buffer to Main Memory Page Program without Built-In Erase, Main Memory Page Program, and Auto Page Rewrite.

The result of the most recent Main Memory Page to Buffer Compare operation is indicated using bit 6 of the status register. If bit 6 is a 0, then the data in the main memory page matches the data in the buffer. If bit 6 is a 1, then at least one bit of the data in the main memory page does not match the data in the buffer.

The device density is indicated using bits 5, 4, and 3 of the status register. For the AT45D021, the three bits are 0, 1, and 0. The decimal value of these three binary bits does not equate to the device density; the three bits represent a combinational code relating to differing densities of Serial DataFlash devices, allowing a total of eight different density configurations.

Read/Program Mode Summary

The modes listed above can be separated into two groups — modes which make use of the flash memory array (Group A) and modes which do not make use of the flash memory array (Group B).

Group A modes consist of:

1. Main memory page read
2. Main memory page to buffer 1 (or 2) transfer
3. Main memory page to buffer 1 (or 2) compare
4. Buffer 1 (or 2) to main memory page program with built-in erase
5. Buffer 1 (or 2) to main memory page program without built-in erase
6. Main memory page program
7. Auto page rewrite

Group B modes consist of:

1. Buffer 1 (or 2) read
2. Buffer 1 (or 2) write
3. Status read

If a Group A mode is in progress (not fully completed) then another mode in Group A should not be started. However, during this time in which a Group A mode is in progress, modes in Group B can be started.

This gives the Serial DataFlash the ability to virtually accommodate a continuous data stream. While data is being programmed into main memory from buffer 1, data can be loaded into buffer 2 (or vice versa). See application note AN-4 ("Using Atmel's Serial DataFlash") for more details.

HARDWARE PAGE WRITE PROTECT: If the $\overline{WP}$ pin is held low, the first 256 pages of the main memory cannot be reprogrammed. The only way to reprogram the first 256 pages is to first drive the protect pin high and then use the program commands previously mentioned.

Status Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RDY/$\overline{BUSY}$	COMP	0	1	0	X	X	X

$\overline{RESET}$: A low state on the reset pin ($\overline{RESET}$) will terminate the operation in progress and reset the internal state machine to an idle state. The device will remain in the reset condition as long as a low level is present on the $\overline{RESET}$ pin. Normal operation can resume once the $\overline{RESET}$ pin is brought back to a high level.

The device also incorporates an internal power-on reset circuit; therefore, there are no restrictions on the $\overline{RESET}$ pin during power-on sequences.

READY/$\overline{BUSY}$: This open drain output pin will be driven low when the device is busy in an internally self-timed operation. This pin, which is normally in a high state (through an external pull-up resistor), will be pulled low during programming operations, compare operations, and during page-to-buffer transfers.

The busy status indicates that the Flash memory array and one of the buffers cannot be accessed; read and write operations to the other buffer can still be performed.

Power On/Reset State

When power is first applied to the device, or when recovering from a reset condition, the device will default to SPI mode 3. In addition, the SO pin will be in a high impedance state, and a high to low stransition on the $\overline{CS}$ pin will be required to start a valid instruction. The SPI mode will be automatically selected on every falling edge of $\overline{CS}$ by sampling the inactive clock state.

4

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC and AC Operating Range

		AT45D021
Operating Temperature (Case)	Com.	0°C to 70°C
	Ind.	-40°C to 85°C
V_{CC} Power Supply[1]		4.5V to 5.5V

Note: 1. After power is applied and V_{CC} is at the minimum specified data sheet value, the system should wait 20 ms before an operational mode is started.

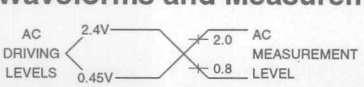
DC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{SB}	Standby Current	$\overline{CS}$, $\overline{RESET}$, $\overline{WP}$ = V_{IH}, all inputs at CMOS levels		15	30	µA
I_{CC1}	Active Current, Read Operation	f = 10 MHz; I_{OUT} = 0 mA; V_{CC} = 5.5V		15	25	mA
I_{CC2}	Active Current, Program/Erase Operation	V_{CC} = 5.5V		25	50	mA
I_{LI}	Input Load Current	V_{IN} = CMOS levels			10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = CMOS levels			10	µA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage		2.0			V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			0.45	V
V_{OH1}	Output High Voltage	I_{OH} = -400 µA	2.4			V
V_{OH2}	Output High Voltage	I_{OH} = -100 µA; V_{CC} = 4.5V	4.2			V

AC Characteristics

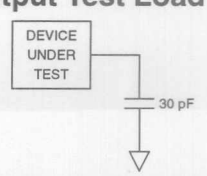
Symbol	Parameter	Min	Typ	Max	Units
f_{SCK}	SCK Frequency			10	MHz
t_{WH}	SCK High Time	40			ns
t_{WL}	SCK Low Time	40			ns
t_{CS}	Minimum $\overline{CS}$ High Time	250			ns
t_{CSS}	$\overline{CS}$ Setup Time	250			ns
t_{CSH}	$\overline{CS}$ Hold Time	250			ns
t_{CSB}	$\overline{CS}$ High to RDY/$\overline{BUSY}$ Low			200	ns
t_{SU}	Data In Setup Time	10			ns
t_H	Data In Hold Time	25			ns
t_{HO}	Output Hold Time	0			ns
t_{DIS}	Output Disable Time			75	ns
t_V	Output Valid			80	ns
t_{XFR}	Page to Buffer Transfer/Compare Time		80	150	µs
t_{EP}	Page Erase and Programming Time		10	20	ms
t_P	Page Programming Time		7	14	ms
t_{RST}	$\overline{RESET}$ Pulse Width	10			µs
t_{REC}	$\overline{RESET}$ Recovery Time			1	µs

Input Test Waveforms and Measurement Levels



t_R, t_F < 20 ns (10% to 90%)

Output Test Load

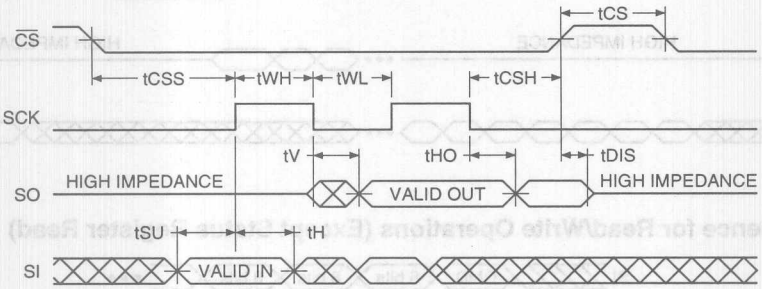


AC Waveforms

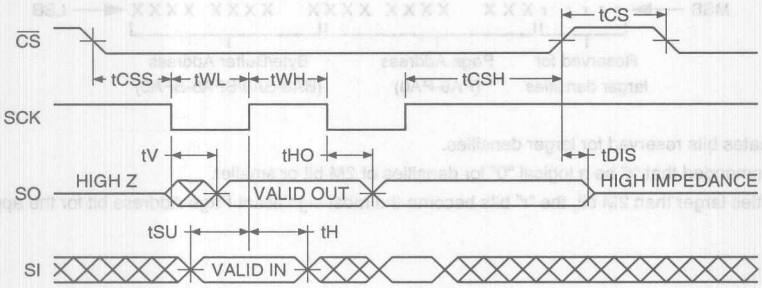
Two different timing diagrams are shown below. Waveform 1 shows the SCK signal being low when $\overline{CS}$ makes a high-to-low transition, and Waveform 2 shows the SCK signal being high when $\overline{CS}$ makes a high-to-low transition. Both wavforms show valid timing diagrams. The setup and hold times for the SI signal are referenced to the low-to-high transition on the SCK signal.

Waveform 1 shows timing that is also compatible with SPI Mode 0, and Waveform 2 shows timing that is compatible with SPI Mode 3.

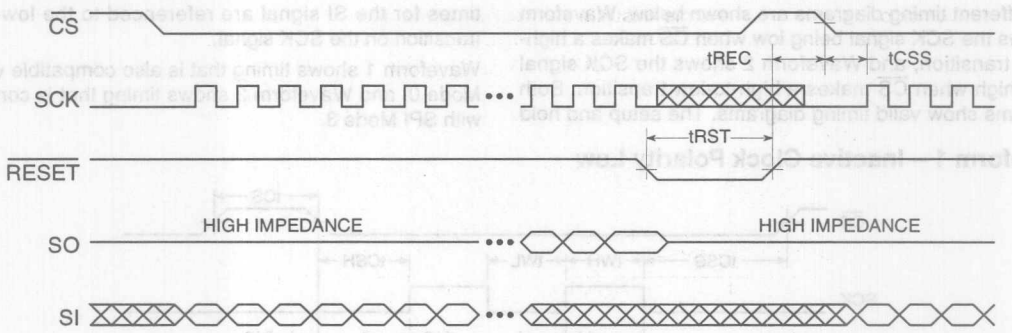
Waveform 1 – Inactive Clock Polarity Low



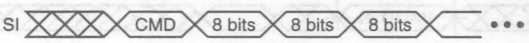
Waveform 2 – Inactive Clock Polarity High

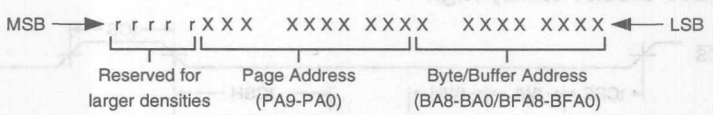


Reset Timing (Inactive Clock Polarity Low Shown)



Command Sequence for Read/Write Operations (Except Status Register Read)

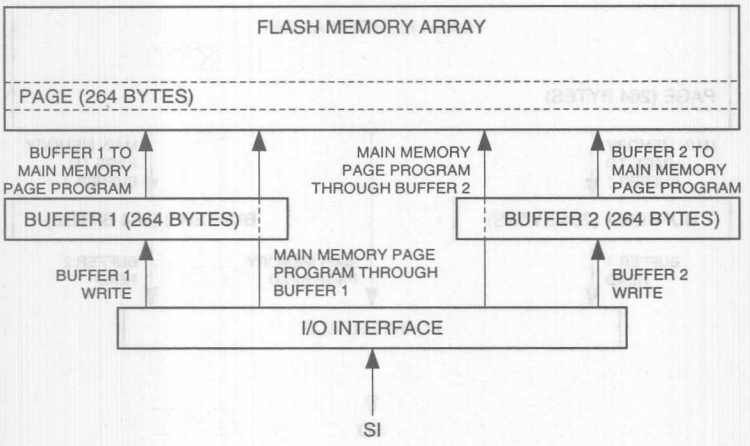




Notes: 1. "r" designates bits reserved for larger densities.
2. It is recommended that "r" be a logical "0" for densities of 2M bit or smaller.
3. For densities larger than 2M bit, the "r" bits become the most significant Page Address bit for the appropriate density.

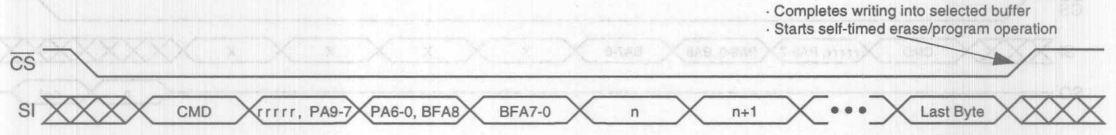
Write Operations

The following block diagram and waveforms illustrate the various write sequences available.

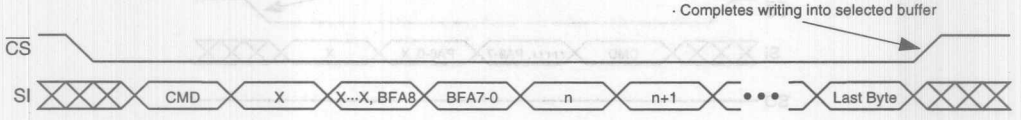


4

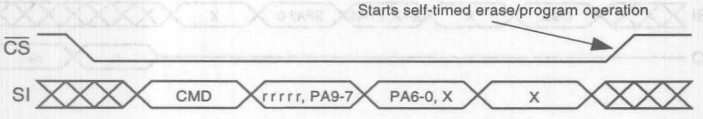
Main Memory Page Program through Buffers

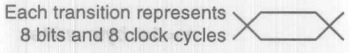


Buffer Write



Buffer to Main Memory Page Program (Data from Buffer Programmed into Flash Page)

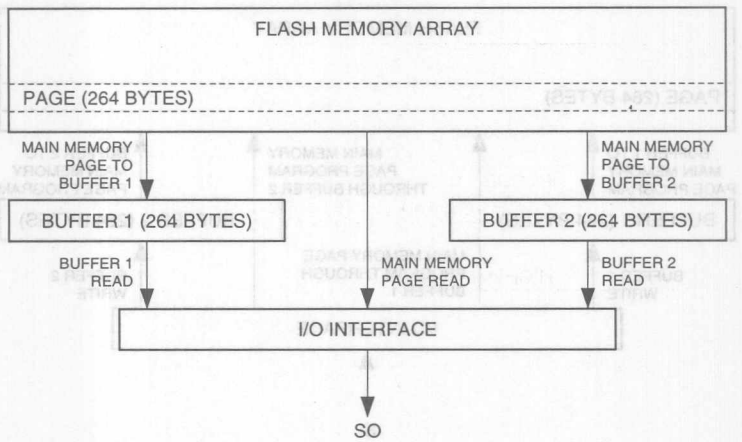




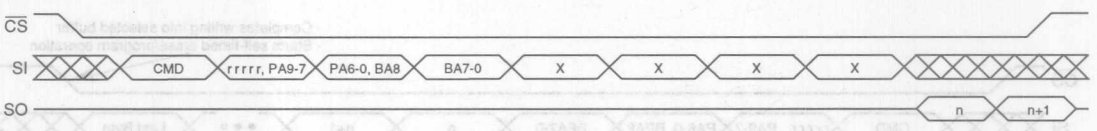
n = 1st byte read
n+1 = 2nd byte read

Read Operations

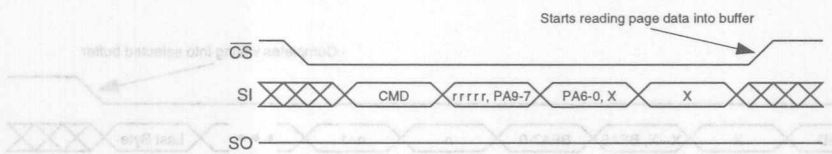
The following block diagram and waveforms illustrate the various read sequences available.



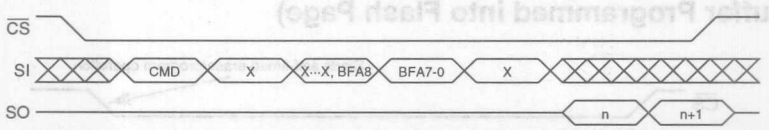
Main Memory Page Read



Main Memory Page to Buffer Transfer (Data from Flash Page Read into Buffer)



Buffer Read

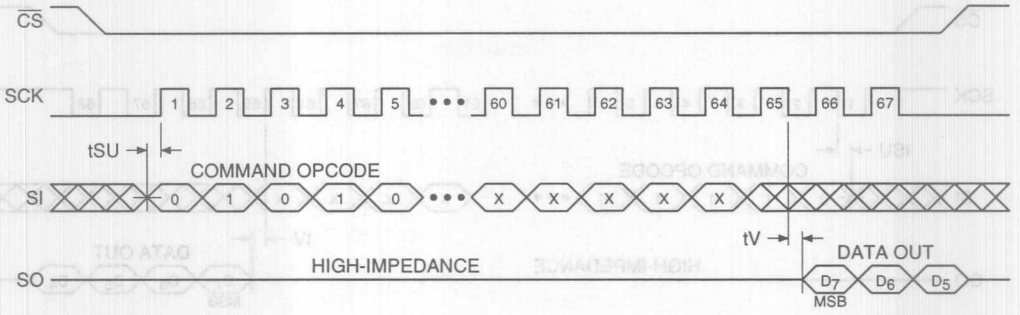


Each transition represents 8 bits and 8 clock cycles

n = 1st byte written
n+1 = 2nd byte written

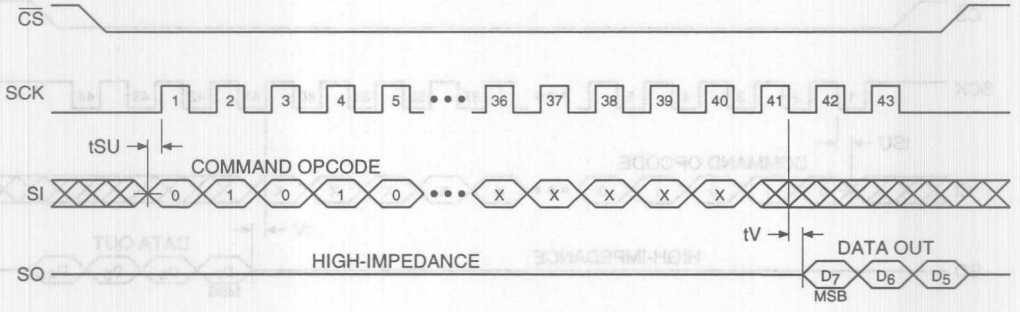
Detailed Bit-Level Read Timing – Inactive Clock Polarity Low

Main Memory Page Read

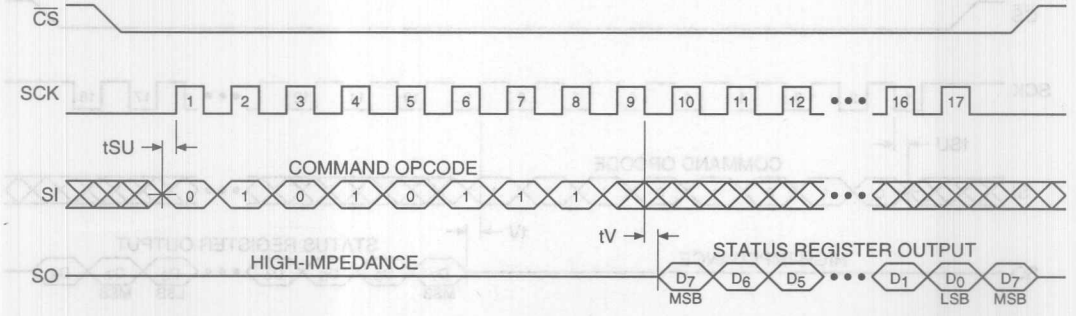


4

Buffer Read

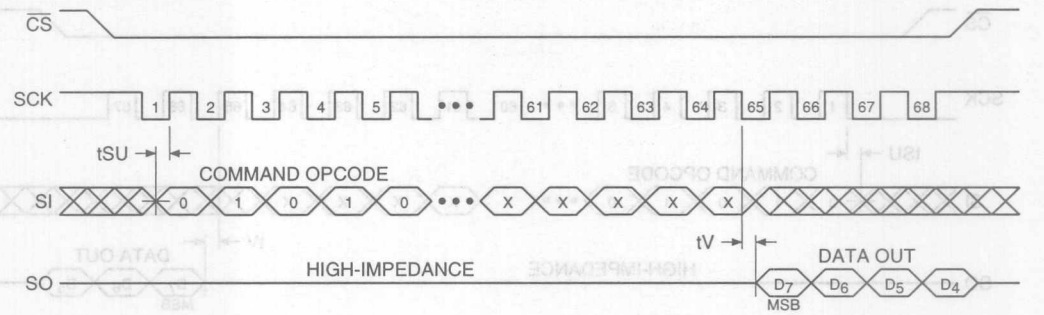


Status Register Read

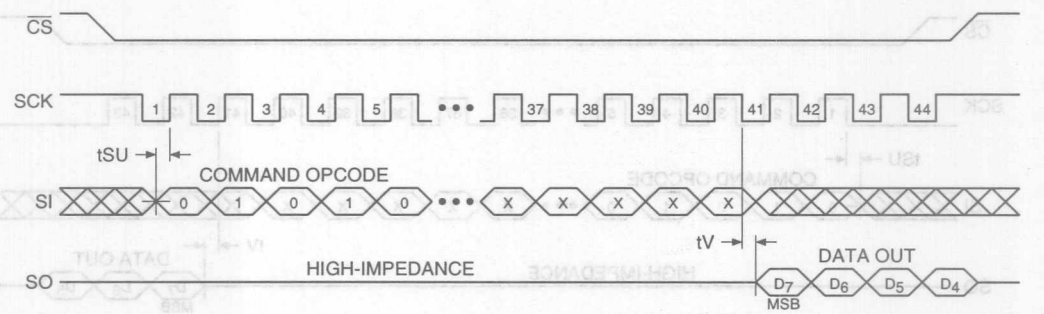


Detailed Bit-Level Read Timing – Inactive Clock Polarity High

Main Memory Page Read



Buffer Read



Status Register Read

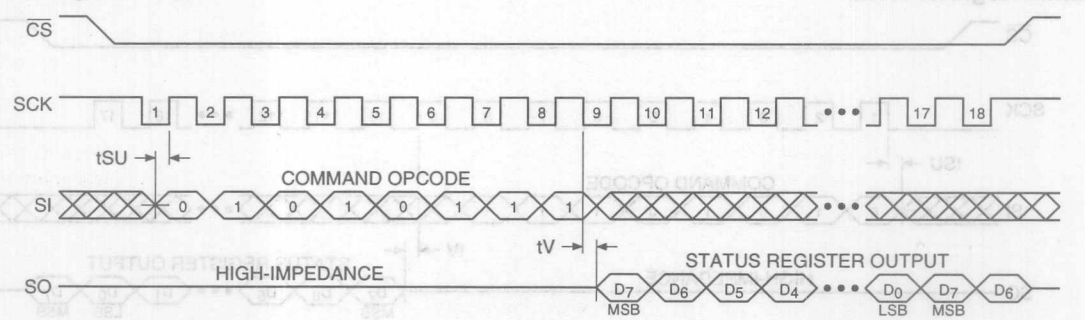


Table 1.

Main Memory Page Read	Buffer 1 Read	Buffer 2 Read	Main Memory Page to Buffer 1 Transfer	Main Memory Page to Buffer 2 Transfer	Main Memory Page to Buffer 1 Compare	Main Memory Page to Buffer 2 Compare	Buffer 1 Write	Buffer 2 Write
				Opcode				
52H	54H	56H	53H	55H	60H	61H	84H	87H
0	0	0	0	0	0	0	1	1
1	1	1	1	1	1	1	0	0
0	0	0	0	0	1	1	0	0
1	1	1	1	1	0	0	0	0
0	0	0	0	0	0	0	0	0
0	1	1	0	1	0	0	1	1
1	0	1	1	0	0	0	0	1
0	0	0	1	1	0	1	0	1
r	X	X	r	r	r	r	X	X
r	X	X	r	r	r	r	X	X
r	X	X	r	r	r	r	X	X
r	X	X	r	r	r	r	X	X
r	X	X	r	r	r	r	X	X
PA9	X	X	PA9	PA9	PA9	PA9	X	X
PA8	X	X	PA8	PA8	PA8	PA8	X	X
PA7	X	X	PA7	PA7	PA7	PA7	X	X
PA6	X	X	PA6	PA6	PA6	PA6	X	X
PA5	X	X	PA5	PA5	PA5	PA5	X	X
PA4	X	X	PA4	PA4	PA4	PA4	X	X
PA3	X	X	PA3	PA3	PA3	PA3	X	X
PA2	X	X	PA2	PA2	PA2	PA2	X	X
PA1	X	X	PA1	PA1	PA1	PA1	X	X
PA0	X	X	PA0	PA0	PA0	PA0	X	X
BA8	BFA8	BFA8	X	X	X	X	BFA8	BFA8
BA7	BFA7	BFA7	X	X	X	X	BFA7	BFA7
BA6	BFA6	BFA6	X	X	X	X	BFA6	BFA6
BA5	BFA5	BFA5	X	X	X	X	BFA5	BFA5
BA4	BFA4	BFA4	X	X	X	X	BFA4	BFA4
BA3	BFA3	BFA3	X	X	X	X	BFA3	BFA3
BA2	BFA2	BFA2	X	X	X	X	BFA2	BFA2
BA1	BFA1	BFA1	X	X	X	X	BFA1	BFA1
BA0	BFA0	BFA0	X	X	X	X	BFA0	BFA0
X	X	X						
X	X	X						
X	X	X						
X	X	X						
X	X	X						
X	X	X						
X	X	X						
X	X	X						
•								
•								
•								
X (64th bit)								

X (Don't Care)
r (reserved bits)

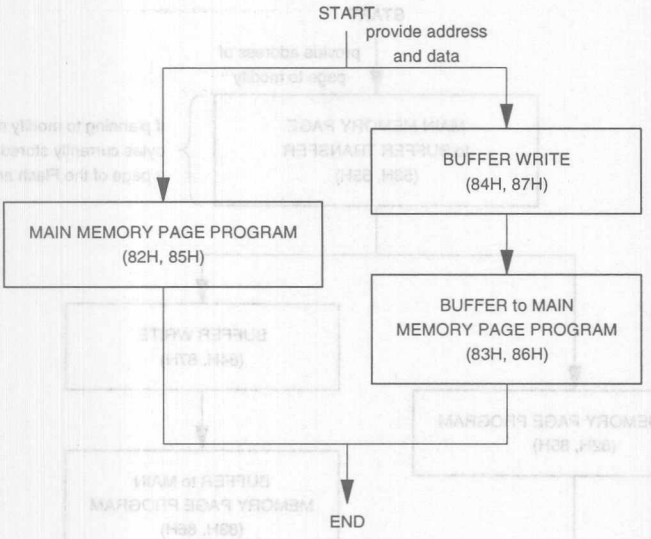
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Table 2.

Buffer 1 to Main Memory Page Program with Built-In Erase	Buffer 2 to Main Memory Page Program with Built-In Erase	Buffer 1 to Main Memory Page Program without Built-In Erase	Buffer 2 to Main Memory Page Program without Built-In Erase	Main Memory Page Program Through Buffer 1	Main Memory Page Program Through Buffer 2	Auto Page Rewrite Through Buffer 1	Auto Page Rewrite Through Buffer 2	Status Register
Opcode								
83H	86H	88H	89H	82H	85H	58H	59H	57H
1	1	1	1	1	1	0	0	0
0	0	0	0	0	0	1	1	1
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1	1
0	0	1	1	0	0	1	1	0
0	1	0	0	0	1	0	0	1
1	1	0	0	1	0	0	0	1
1	0	0	1	0	1	0	1	1
r	r	r	r	r	r	r	r	
r	r	r	r	r	r	r	r	
r	r	r	r	r	r	r	r	
r	r	r	r	r	r	r	r	
r	r	r	r	r	r	r	r	
PA9	PA9	PA9	PA9	PA9	PA9	PA9	PA9	
PA8	PA8	PA8	PA8	PA8	PA8	PA8	PA8	
PA7	PA7	PA7	PA7	PA7	PA7	PA7	PA7	
PA6	PA6	PA6	PA6	PA6	PA6	PA6	PA6	
PA5	PA5	PA5	PA5	PA5	PA5	PA5	PA5	
PA4	PA4	PA4	PA4	PA4	PA4	PA4	PA4	
PA3	PA3	PA3	PA3	PA3	PA3	PA3	PA3	
PA2	PA2	PA2	PA2	PA2	PA2	PA2	PA2	
PA1	PA1	PA1	PA1	PA1	PA1	PA1	PA1	
PA0	PA0	PA0	PA0	PA0	PA0	PA0	PA0	
X	X	X	X	BA8	BA8	X	X	
X	X	X	X	BA7	BA7	X	X	
X	X	X	X	BA6	BA6	X	X	
X	X	X	X	BA5	BA5	X	X	
X	X	X	X	BA4	BA4	X	X	
X	X	X	X	BA3	BA3	X	X	
X	X	X	X	BA2	BA2	X	X	
X	X	X	X	BA1	BA1	X	X	
X	X	X	X	BA0	BA0	X	X	

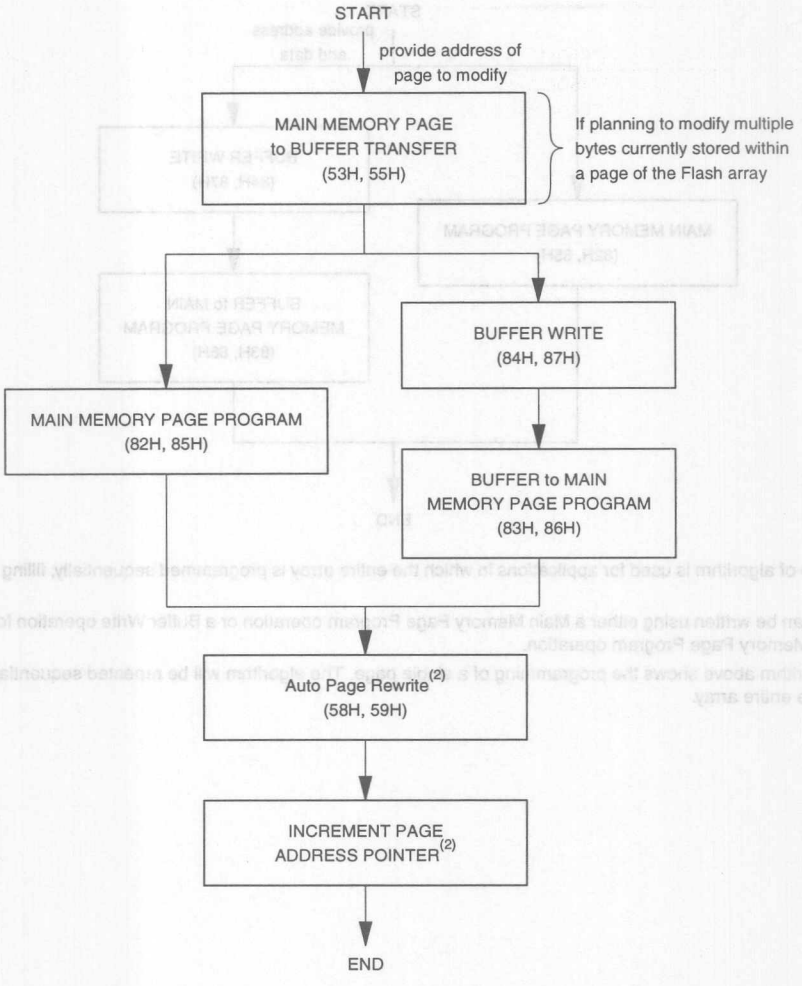
X (Don't Care)
r (reserved bits)

Figure 1. Algorithm for Programming or Reprogramming of the Entire Array Sequentially



Notes:
1. This type of algorithm is used for applications in which the entire array is programmed sequentially, filling the array page-by-page.
2. A page can be written using either a Main Memory Page Program operation or a Buffer Write operation followed by a Buffer to Main Memory Page Program operation.
3. The algorithm above shows the programming of a single page. The algorithm will be repeated sequentially for each page within the entire array.

Figure 2. Algorithm for Randomly Modifying Data



Notes:
1. To preserve data integrity, each page of the DataFlash memory array must be updated/rewritten at least once within every 10,000 cumulative page erase/program operations.
2. A Page Address Pointer must be maintained to indicate which page is to be rewritten. The Auto Page Rewrite command must use the address specified by the Page Address Pointer.
3. Other algorithms can be used to rewrite portions of the Flash array. Low power applications may choose to wait until 10,000 cumulative page erase/program operations have accumulated before rewriting all pages of the Flash array. See application note AN-4 ("Using Atmel's Serial DataFlash") for more details.

Ordering Information

f_{SCK} (MHz)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
10	25	0.03	AT45D021-JC AT45D021-RC AT45D021-TC	32J 28R 28T	Commercial (0°C to 70°C)
10	25	0.03	AT45D021-JI AT45D021-RI AT45D021-TI	32J 28R 28T	Industrial (-40°C to 85°C)

4

Package Type	
32J	32-Lead, Plastic J-Leaded Chip Carrier Package (PLCC)
28R	28-Lead, 0.330" Wide, Plastic Gull-Wing Small Outline Package (SOIC)
28T	28-Lead, Plastic Thin Small Outline Package (TSOP)

Ordering Information

f_{MAX} (MHz)	I_{CC} (mA)		Ordering Code	Packages	Operation Range
	Active	Standby			
10	25	0.03	AT45D021-JC	J21	Commercial
			AT45D021-RC	Z2R	(0°C to 70°C)
			AT45D021-TC	Z2T	
10	25	0.03	AT45D021-JI	J21	Industrial
			AT45D021-RI	Z2R	(-40°C to 85°C)
			AT45D021-TI	Z2T	

Package Type	
J21	32-Lead, Plastic J-Leaded Chip Carrier Package (PLCC)
Z2R	28-Lead, 0.330" Wide, Plastic Gull-Wing Small Outline Package (SOIC)
Z2T	28-Lead, Plastic Thin Small Outline Package (TSOP)

Features

- Single 4.5V - 5.5V Supply
- Serial Interface Architecture
- Page Program Operation
  - Single Cycle Reprogram (Erase and Program)
  - 2048 Pages (264 Bytes/Page) Main Memory
- Two 264-Byte SRAM Data Buffers - Allows Receiving of Data while Reprogramming of Nonvolatile Memory
- Internal Program and Control Timer
- Fast Page Program Time - 7 ms Typical
- 80 µs Typical Page to Buffer Transfer Time
- Low Power Dissipation
  - 15 mA Active Read Current Typical
  - 20 µA CMOS Standby Current Typical
- 10 MHz Max Clock Frequency
- Hardware Data Protection Feature
- Serial Peripheral Interface (SPI) Compatible – Modes 0 and 3
- CMOS and TTL Compatible Inputs and Outputs
- Commercial and Industrial Temperature Ranges

Description

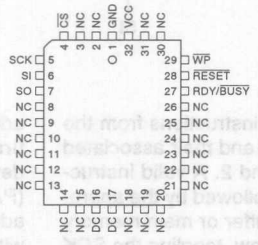
The AT45D041 is a 5-volt only, serial interface Flash memory suitable for in-system reprogramming. Its 4,325,376 bits of memory are organized as 2048 pages of 264-bytes each. In addition to the main memory, the AT45D041 also contains two data SRAM buffers of 264-bytes each. The buffers allow receiving of data while a page in the main memory is being reprogrammed. Unlike conventional Flash memories that

(continued)

Pin Configurations

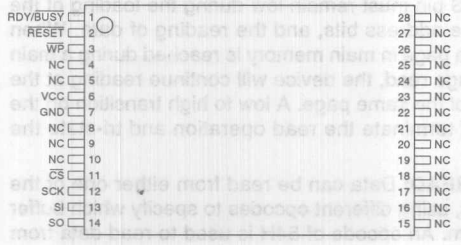
Pin Name	Function
$\overline{CS}$	Chip Select
SCK	Serial Clock
SI	Serial Input
SO	Serial Output
$\overline{WP}$	Hardware Page Write Protect Pin
$\overline{RESET}$	Chip Reset
RDY/$\overline{BUSY}$	Ready/Busy

PLCC

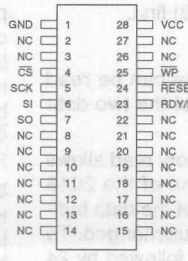


Note: PLCC package pins 16 and 17 are DON'T CONNECT.

TSOP Top View
Type 1



SOIC



4-Megabit 5-volt Only Serial DataFlash®

4

AT45D041

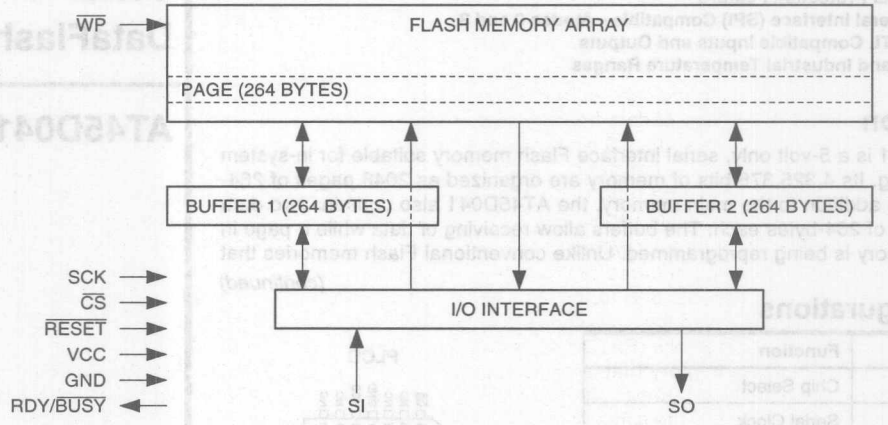
Rev. 0803D–10/98

are accessed randomly with multiple address lines and a parallel interface, the DataFlash uses a serial interface to sequentially access its data. The simple serial interface facilitates hardware layout, increases system reliability, minimizes switching noise, and reduces package size and active pin count. The device is optimized for use in many commercial and industrial applications where high density, low pin count, low voltage, and low power are essential. Typical applications for the DataFlash are digital voice storage, image storage, and data storage. The device operates at clock frequencies up to 10 MHz with a typical active read current consumption of 15 mA.

To allow for simple in-system reprogrammability, the AT45D041 does not require high input voltages for programming. The device operates from a single power supply, 4.5V to 5.5V, for both the program and read operations. The AT45D041 is enabled through the chip select pin ($\overline{CS}$) and accessed via a three-wire interface consisting of the Serial Input (SI), Serial Output (SO), and the Serial Clock (SCK).

All programming cycles are self-timed, and no separate erase cycle is required before programming.

Block Diagram



Device Operation

The device operation is controlled by instructions from the host processor. The list of instructions and their associated opcodes are contained in Tables 1 and 2. A valid instruction starts with the falling edge of $\overline{CS}$ followed by the appropriate 8-bit opcode and the desired buffer or main memory address location. While the $\overline{CS}$ pin is low, toggling the SCK pin controls the loading of the opcode and the desired buffer or main memory address location through the SI (serial input) pin. All instructions, addresses, and data are transferred with the most significant bit (MSB) first.

Read

By specifying the appropriate opcode, data can be read from the main memory or from either one of the two data buffers.

MAIN MEMORY PAGE READ: A main memory read allows the user to read data directly from any one of the 2048 pages in the main memory, bypassing both of the data buffers and leaving the contents of the buffers unchanged. To start a page read, the 8-bit opcode, 52H, is followed by 24 address bits and 32 don't care bits. In the AT45D041, the first four address bits are reserved for larger density devices (see Notes on page 178), the next 11 address bits (PA10-PA0) specify the page address, and the next nine address bits (BA8-BA0) specify the starting byte address within the page. The 32 don't care bits which follow the 24 address bits are sent to initialize the read operation. Following the 32 don't care bits, additional pulses on SCK result in serial data being output on the SO (serial output) pin. The $\overline{CS}$ pin must remain low during the loading of the opcode, the address bits, and the reading of data. When the end of a page in main memory is reached during a main memory page read, the device will continue reading at the beginning of the same page. A low to high transition on the $\overline{CS}$ pin will terminate the read operation and tri-state the SO pin.

BUFFER READ: Data can be read from either one of the two buffers, using different opcodes to specify which buffer to read from. An opcode of 54H is used to read data from buffer 1, and an opcode of 56H is used to read data from

buffer 2. To perform a buffer read, the eight bits of the opcode must be followed by 15 don't care bits, nine address bits, and eight don't care bits. Since the buffer size is 264-bytes, nine address bits (BFA8-BFA0) are required to specify the first byte of data to be read from the buffer. The $\overline{CS}$ pin must remain low during the loading of the opcode, the address bits, the don't care bits, and the reading of data. When the end of a buffer is reached, the device will continue reading back at the beginning of the buffer. A low to high transition on the $\overline{CS}$ pin will terminate the read operation and tri-state the SO pin.

MAIN MEMORY PAGE TO BUFFER TRANSFER: A page of data can be transferred from the main memory to either buffer 1 or buffer 2. An 8-bit opcode, 53H for buffer 1 and 55H for buffer 2, is followed by the four reserved bits, 11 address bits (PA10-PA0) which specify the page in main memory that is to be transferred, and nine don't care bits. The $\overline{CS}$ pin must be low while toggling the SCK pin to load the opcode, the address bits, and the don't care bits from the SI pin. The transfer of the page of data from the main memory to the buffer will begin when the $\overline{CS}$ pin transitions from a low to a high state. During the transfer of a page of data (t_{XFR}), the status register can be read to determine whether the transfer has been completed or not.

MAIN MEMORY PAGE TO BUFFER COMPARE: A page of data in main memory can be compared to the data in buffer 1 or buffer 2. An 8-bit opcode, 60H for buffer 1 and 61H for buffer 2, is followed by 24 address bits consisting of the four reserved bits, 11 address bits (PA10-PA0) which specify the page in the main memory that is to be compared to the buffer, and nine don't care bits. The loading of the opcode and the address bits is the same as described previously. The $\overline{CS}$ pin must be low while toggling the SCK pin to load the opcode, the address bits, and the don't care bits from the SI pin. On the low to high transition of the $\overline{CS}$ pin, the 264 bytes in the selected main memory page will be compared with the 264 bytes in buffer 1 or buffer 2. During this time (t_{XFR}), the status register will indicate that the part is busy. On completion of the compare operation, bit 6 of the status register is updated with the result of the compare.

Program

BUFFER WRITE: Data can be shifted in from the SI pin into either buffer 1 or buffer 2. To load data into either buffer, an 8-bit opcode, 84H for buffer 1 or 87H for buffer 2, is followed by 15 don't care bits and nine address bits (BFA8-BFA0). The nine address bits specify the first byte in the buffer to be written. The data is entered following the address bits. If the end of the data buffer is reached, the device will wrap around back to the beginning of the buffer. Data will continue to be loaded into the buffer until a low to high transition is detected on the $\overline{CS}$ pin.

BUFFER TO MAIN MEMORY PAGE PROGRAM WITH BUILT-IN ERASE: Data written into either buffer 1 or buffer 2 can be programmed into the main memory. An 8-bit opcode, 83H for buffer 1 or 86H for buffer 2, is followed by the four reserved bits, 11 address bits (PA10-PA0) that specify the page in the main memory to be written, and nine additional don't care bits. When a low to high transition occurs on the $\overline{CS}$ pin, the part will first erase the selected page in main memory to all 1s and then program the data stored in the buffer into the specified page in the main memory. Both the erase and the programming of the page are internally self timed and should take place in a maximum time of t_{EP}. During this time, the status register will indicate that the part is busy.

BUFFER TO MAIN MEMORY PAGE PROGRAM WITHOUT BUILT-IN ERASE: A previously erased page within main memory can be programmed with the contents of either buffer 1 or buffer 2. An 8-bit opcode, 88H for buffer 1 or 89H for buffer 2, is followed by the four reserved bits, 11 address bits (PA10-PA0) that specify the page in the main memory to be written, and nine additional don't care bits. When a low to high transition occurs on the $\overline{CS}$ pin, the part will program the data stored in the buffer into the specified page in the main memory. It is necessary that the page in main memory that is being programmed has been previously programmed to all 1s (erased state). The programming of the page is internally self timed and should take place in a maximum time of t_P. During this time, the status register will indicate that the part is busy.

MAIN MEMORY PAGE PROGRAM: This operation is a combination of the Buffer Write and Buffer to Main Memory Page Program with Built-In Erase operations. Data is first shifted into buffer 1 or buffer 2 from the SI pin and then programmed into a specified page in the main memory. An 8-bit opcode, 82H for buffer 1 or 85H for buffer 2, is followed by the four reserved bits and 20 address bits. The 11 most significant address bits (PA10-PA0) select the page in the main memory where data is to be written, and the next nine address bits (BFA8-BFA0) select the first byte in the buffer to be written. After all address bits are shifted in, the part will take data from the SI pin and store it in one of the data buffers. If the end of the buffer is reached, the device will wrap around back to the beginning of the buffer. When there is a low to high transition on the $\overline{CS}$ pin, the part will first erase the selected page in main memory to all 1s and then program the data stored in the buffer into the specified page in the main memory. Both the erase and the programming of the page are internally self timed and should take place in a maximum of time t_{EP}. During this time, the status register will indicate that the part is busy.

AUTO PAGE REWRITE: This mode is only needed if multiple bytes within a page or multiple pages of data are modified in a random fashion. This mode is a combination of two operations: Main Memory Page to Buffer Transfer and

Buffer to Main Memory Page Program with Built-In Erase. A page of data is first transferred from the main memory to buffer 1 or buffer 2, and then the same data (from buffer 1 or buffer 2) is programmed back into its original page of main memory. An 8-bit opcode, 58H for buffer 1 or 59H for buffer 2, is followed by the four reserved bits, 11 address bits (PA10-PA0) that specify the page in main memory to be rewritten, and nine additional don't care bits. When a low to high transition occurs on the $\overline{CS}$ pin, the part will first transfer data from the page in main memory to a buffer and then program the data from the buffer back into same page of main memory. The operation is internally self-timed and should take place in a maximum time of t_{EP}. During this time, the status register will indicate that the part is busy.

If the main memory is programmed or reprogrammed sequentially page by page, then the programming algorithm shown in Figure 1 is recommended. Otherwise, if multiple bytes in a page or several pages are programmed randomly in the main memory, then the programming algorithm shown in Figure 2 is recommended.

STATUS REGISTER: The status register can be used to determine the device's ready/busy status, the result of a Main Memory Page to Buffer Compare operation, or the device density. To read the status register, an opcode of 57H must be loaded into the device. After the last bit of the opcode is shifted in, the eight bits of the status register, starting with the MSB (bit 7), will be shifted out on the SO pin during the next eight clock cycles. The five most-significant bits of the status register will contain device information, while the remaining three least-significant bits are reserved for future use and will have undefined values. After bit 0 of the status register has been shifted out, the sequence will repeat itself (as long as $\overline{CS}$ remains low and SCK is being toggled) starting again with bit 7. The data in the status register is constantly updated, so each repeating sequence will output new data.

Ready/busy status is indicated using bit 7 of the status register. If bit 7 is a 1, then the device is not busy and is ready to accept the next command. If bit 7 is a 0, then the device is in a busy state. The user can continuously poll bit 7 of the status register by stopping SCK once bit 7 has been output. The status of bit 7 will continue to be output on the SO pin, and once the device is no longer busy, the state of SO will change from 0 to 1. There are six operations which can cause the device to be in a busy state: Main Memory Page to Buffer Transfer, Main Memory Page to Buffer Compare, Buffer to Main Memory Page Program with Built-In Erase, Buffer to Main Memory Page Program without Built-In Erase, Main Memory Page Program, and Auto Page Rewrite.

The result of the most recent Main Memory Page to Buffer Compare operation is indicated using bit 6 of the status register. If bit 6 is a 0, then the data in the main memory page matches the data in the buffer. If bit 6 is a 1, then at least one bit of the data in the main memory page does not match the data in the buffer.

The device density is indicated using bits 5, 4, and 3 of the status register. For the AT45D041, the three bits are 0, 1, and 1. The decimal value of these three binary bits does not equate to the device density; the three bits represent a combinational code relating to differing densities of Serial DataFlash devices, allowing a total of eight different density configurations.

Read/Program Mode Summary

The modes listed above can be separated into two groups — modes which make use of the flash memory array (Group A) and modes which do not make use of the flash memory array (Group B).

Group A modes consist of:

1. Main memory page read
2. Main memory page to buffer 1 (or 2) transfer
3. Main memory page to buffer 1 (or 2) compare
4. Buffer 1 (or 2) to main memory page program with built-in erase
5. Buffer 1 (or 2) to main memory page program without built-in erase
6. Main memory page program
7. Auto page rewrite

Group B modes consist of:

1. Buffer 1 (or 2) read
2. Buffer 1 (or 2) write
3. Status read

If a Group A mode is in progress (not fully completed) then another mode in Group A should not be started. However, during this time in which a Group A mode is in progress, modes in Group B can be started.

This gives the Serial DataFlash the ability to virtually accommodate a continuous data stream. While data is being programmed into main memory from buffer 1, data can be loaded into buffer 2 (or vice versa). See application note AN-4 ("Using Atmel's Serial DataFlash") for more details.

Status Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RDY/$\overline{BUSY}$	COMP	0	1	1	X	X	X

HARDWARE PAGE WRITE PROTECT: If the $\overline{WP}$ pin is held low, the first 256 pages of the main memory cannot be reprogrammed. The only way to reprogram the first 256 pages is to first drive the protect pin high and then use the program commands previously mentioned.

$\overline{RESET}$: A low state on the reset pin ($\overline{RESET}$) will terminate the operation in progress and reset the internal state machine to an idle state. The device will remain in the reset condition as long as a low level is present on the $\overline{RESET}$ pin. Normal operation can resume once the $\overline{RESET}$ pin is brought back to a high level.

The device also incorporates an internal power-on reset circuit; therefore, there are no restrictions on the $\overline{RESET}$ pin during power-on sequences.

READY/$\overline{BUSY}$: This open drain output pin will be driven low when the device is busy in an internally self-timed operation. This pin, which is normally in a high state (through an external pull-up resistor), will be pulled low during programming operations, compare operations, and during page-to-buffer transfers.

The busy status indicates that the Flash memory array and one of the buffers cannot be accessed; read and write operations to the other buffer can still be performed.

Power On/Reset State

When power is first applied to the device, or when recovering from a reset condition, the device will default to SPI mode 3. In addition, the SO pin will bein a high impedance state, and a high to low transition on the $\overline{CS}$ pin will be required to start a valid instruction. The SPI mode will be automatically selected on every falling edge of $\overline{CS}$ by sampling the inactive clock state.

4

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC and AC Operating Range

		AT45D041
Operating Temperature (Case)	Com.	0°C to 70°C
	Ind.	-40°C to 85°C
V_{CC} Power Supply[1]		4.5V to 5.5V

Note: 1. After power is applied and V_{CC} is at the minimum specified data sheet value, the system should wait 20 ms before an operational mode is started.

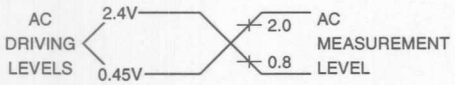
DC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{SB}	Standby Current	$\overline{CS}$, $\overline{RESET}$, $\overline{WP}$ = V_{IH}, all inputs at CMOS levels		20	40	µA
I_{CC1}	Active Current, Read Operation	f = 10 MHz; I_{OUT} = 0 mA; V_{CC} = 5.5V		15	25	mA
I_{CC2}	Active Current, Program/Erase Operation	V_{CC} = 5.5V		25	50	mA
I_{LI}	Input Load Current	V_{IN} = CMOS levels			10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = CMOS levels			10	µA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage		2.0			V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			0.45	V
V_{OH1}	Output High Voltage	I_{OH} = -400 µA	2.4			V
V_{OH2}	Output High Voltage	I_{OH} = -100 µA; V_{CC} = 4.5V	4.2			V

AC Characteristics

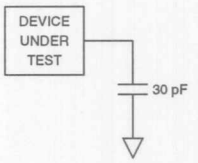
Symbol	Parameter	Min	Typ	Max	Units
f_{SCK}	SCK Frequency			10	MHz
t_{WH}	SCK High Time	40			ns
t_{WL}	SCK Low Time	40			ns
t_{CS}	Minimum $\overline{CS}$ High Time	250			ns
t_{CSS}	$\overline{CS}$ Setup Time	250			ns
t_{CSH}	$\overline{CS}$ Hold Time	250			ns
t_{CSB}	$\overline{CS}$ High to RDY/BUSY Low			200	ns
t_{SU}	Data In Setup Time	10			ns
t_H	Data In Hold Time	25			ns
t_{HO}	Output Hold Time	0			ns
t_{DIS}	Output Disable Time			75	ns
t_V	Output Valid			80	ns
t_{XFR}	Page to Buffer Transfer/Compare Time		80	150	µs
t_{EP}	Page Erase and Programming Time		10	20	ms
t_P	Page Programming Time		7	14	ms
t_{RST}	$\overline{RESET}$ Pulse Width	10			µs
t_{REC}	$\overline{RESET}$ Recovery Time			1	µs

Input Test Waveforms and Measurement Levels



t_R, t_F < 20 ns (10% to 90%)

Output Test Load

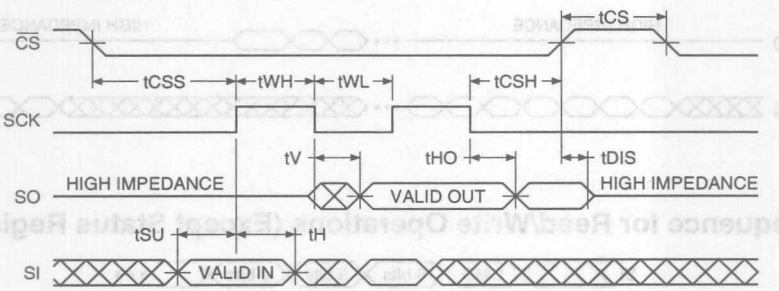


AC Waveforms

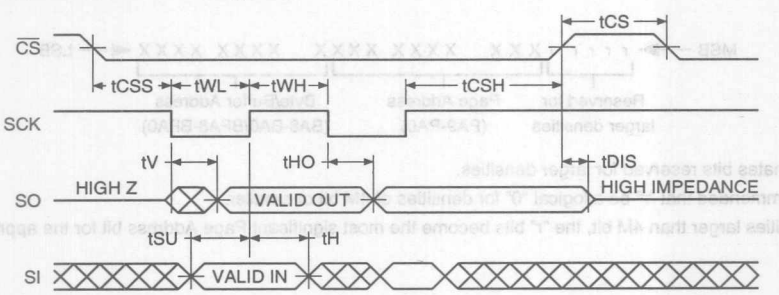
Two different timing diagrams are shown below. Waveform 1 shows the SCK signal being low when $\overline{CS}$ makes a high-to-low transition, and Waveform 2 shows the SCK signal being high when $\overline{CS}$ makes a high-to-low transition. Both wavforms show valid timing diagrams. The setup and hold times for the SI signal are referenced to the low-to-high transition on the SCK signal.

Waveform 1 shows timing that is also compatible with SPI Mode 0, and Waveform 2 shows timing that is compatible with SPI Mode 3.

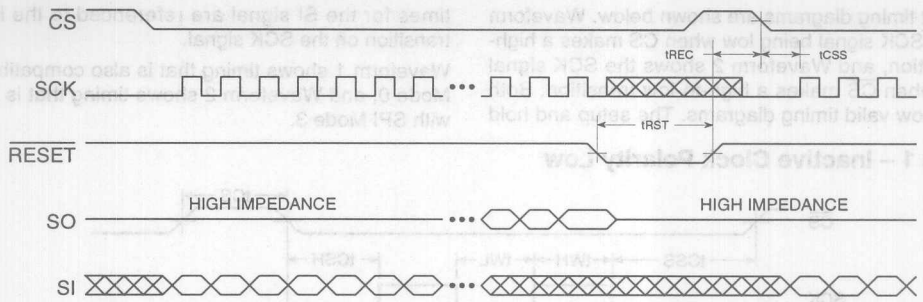
Waveform 1 – Inactive Clock Polarity Low



Waveform 2 – Inactive Clock Polarity High

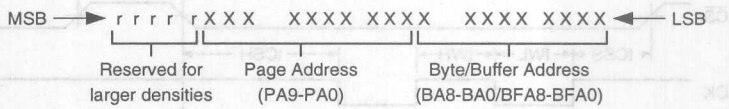


Reset Timing (Inactive Clock Polarity Low Shown)



Command Sequence for Read/Write Operations (Except Status Register Read)

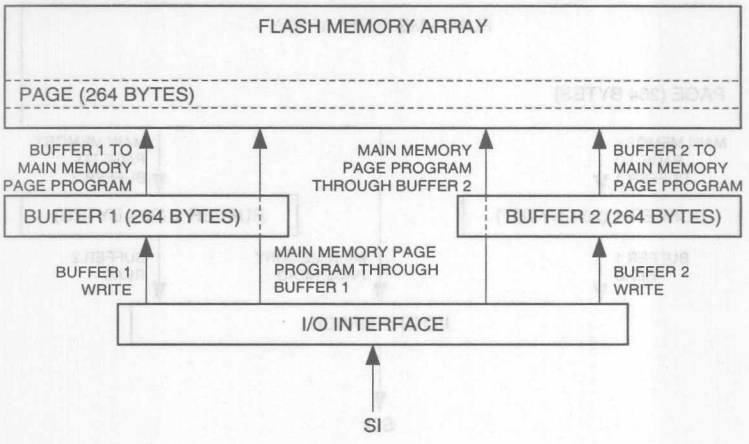




Notes: 1. "r" designates bits reserved for larger densities.
2. It is recommended that "r" be a logical "0" for densities of 4M bit or smaller.
3. For densities larger than 4M bit, the "r" bits become the most significant Page Address bit for the appropriate density.

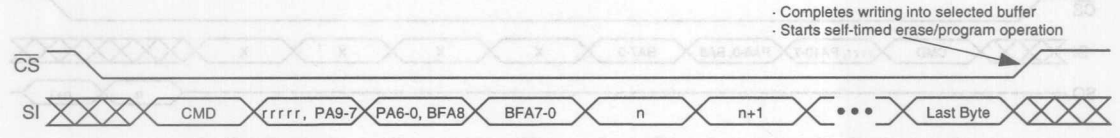
Write Operations

The following block diagram and waveforms illustrate the various write sequences available.

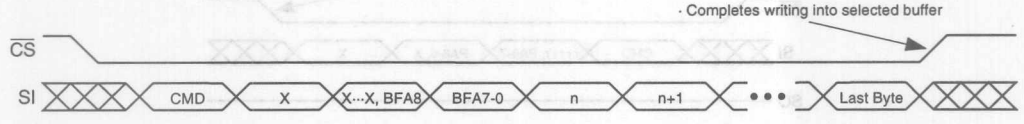


4

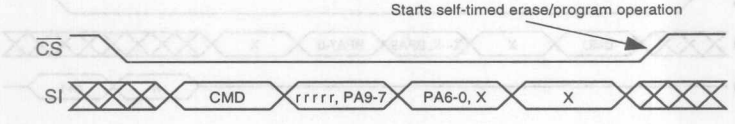
Main Memory Page Program through Buffers



Buffer Write



Buffer to Main Memory Page Program (Data from Buffer Programmed into Flash Page)

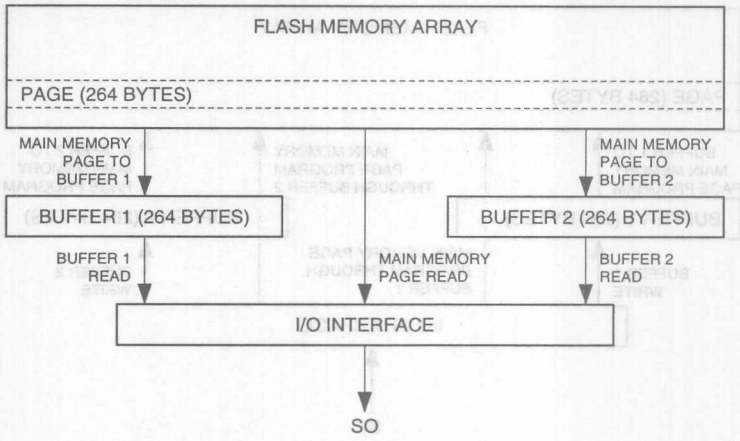


Each transition represents 8 bits and 8 clock cycles

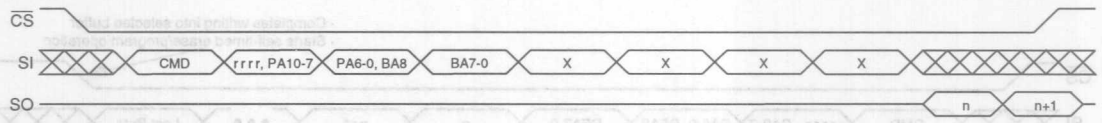
n = 1st byte read
n+1 = 2nd byte read

Read Operations

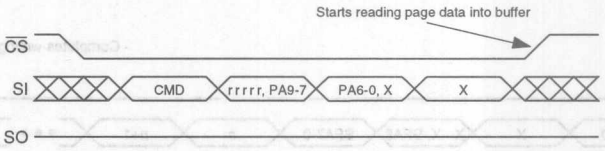
The following block diagram and waveforms illustrate the various read sequences available.



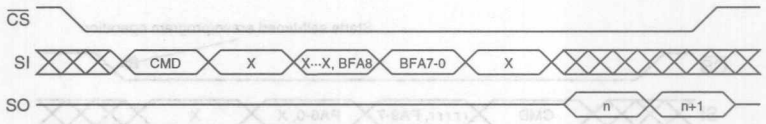
Main Memory Page Read



Main Memory Page to Buffer Transfer (Data from Flash Page Read into Buffer)



Buffer Read

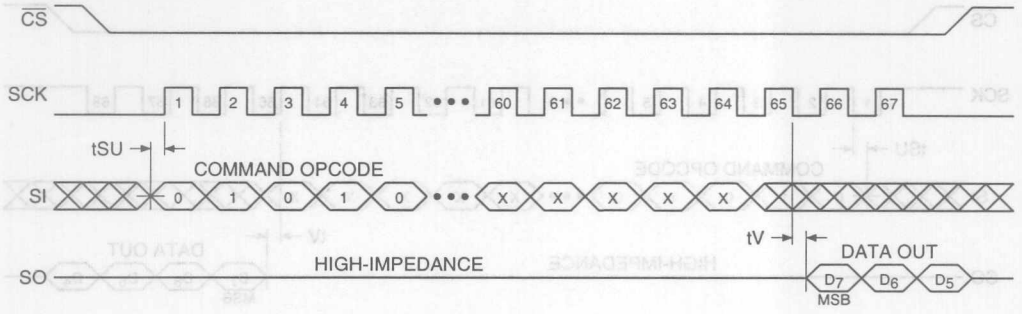


Each transition represents 8 bits and 8 clock cycles

n = 1st byte read
n+1 = 2nd byte read

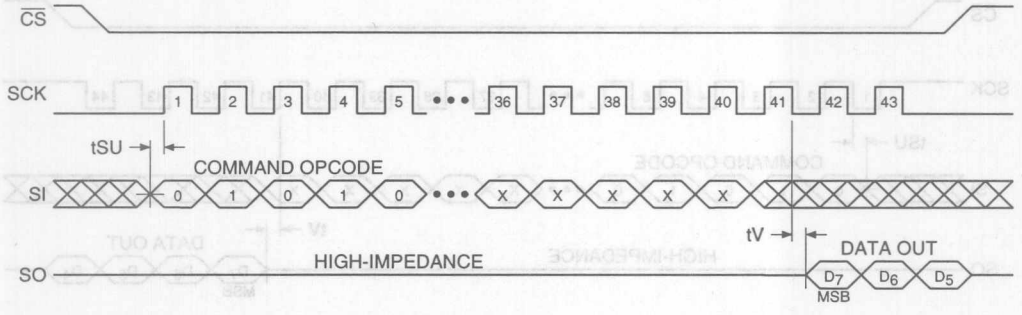
Detailed Bit-Level Read Timing – Inactive Clock Polarity Low

Main Memory Page Read

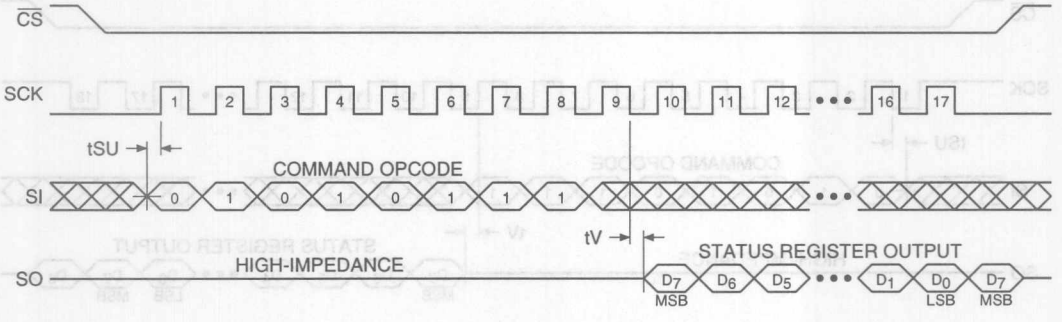


4

Buffer Read

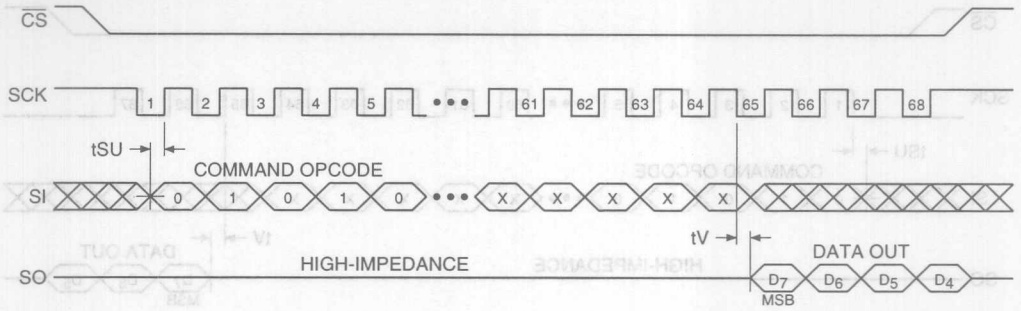


Status Register Read

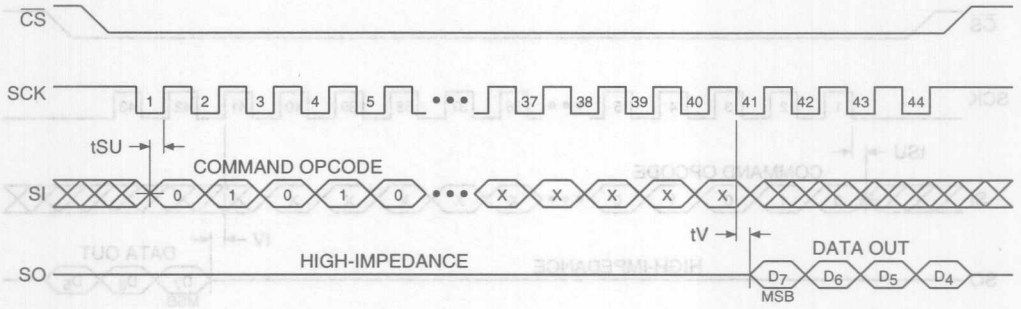


Detailed Bit-Level Read Timing – Inactive Clock Polarity High

Main Memory Page Read



Buffer Read



Status Register Read

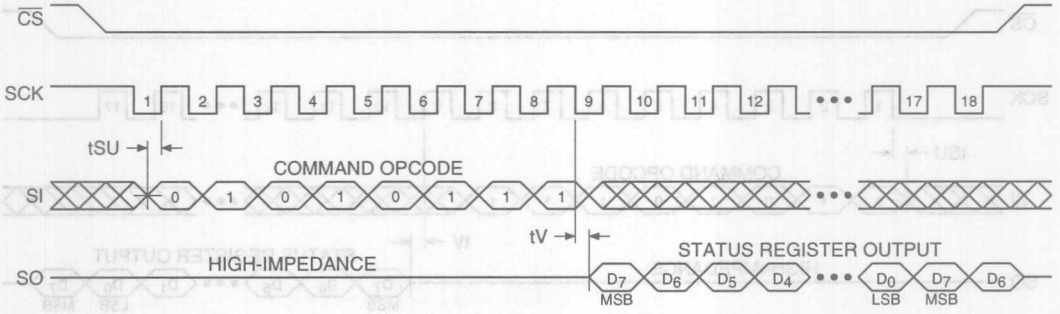


Table 1.

Main Memory Page Read	Buffer 1 Read	Buffer 2 Read	Main Memory Page to Buffer 1 Transfer	Main Memory Page to Buffer 2 Transfer	Main Memory Page to Buffer 1 Compare	Main Memory Page to Buffer 2 Compare	Buffer 1 Write	Buffer 2 Write
				Opcode				
52H	54H	56H	53H	55H	60H	61H	84H	87H
0	0	0	0	0	0	0	1	1
1	1	1	1	1	1	1	0	0
0	0	0	0	0	1	1	0	0
1	1	1	1	1	0	0	0	0
0	0	0	0	0	0	0	0	0
0	1	1	0	1	0	0	1	1
1	0	1	1	0	0	0	0	1
0	0	0	1	1	0	1	0	1
r	X	X	r	r	r	r	X	X
r	X	X	r	r	r	r	X	X
r	X	X	r	r	r	r	X	X
r	X	X	r	r	r	r	X	X
PA10	X	X	PA10	PA10	PA10	PA10	X	X
PA9	X	X	PA9	PA9	PA9	PA9	X	X
PA8	X	X	PA8	PA8	PA8	PA8	X	X
PA7	X	X	PA7	PA7	PA7	PA7	X	X
PA6	X	X	PA6	PA6	PA6	PA6	X	X
PA5	X	X	PA5	PA5	PA5	PA5	X	X
PA4	X	X	PA4	PA4	PA4	PA4	X	X
PA3	X	X	PA3	PA3	PA3	PA3	X	X
PA2	X	X	PA2	PA2	PA2	PA2	X	X
PA1	X	X	PA1	PA1	PA1	PA1	X	X
PA0	X	X	PA0	PA0	PA0	PA0	X	X
BA8	BFA8	BFA8	X	X	X	X	BFA8	BFA8
BA7	BFA7	BFA7	X	X	X	X	BFA7	BFA7
BA6	BFA6	BFA6	X	X	X	X	BFA6	BFA6
BA5	BFA5	BFA5	X	X	X	X	BFA5	BFA5
BA4	BFA4	BFA4	X	X	X	X	BFA4	BFA4
BA3	BFA3	BFA3	X	X	X	X	BFA3	BFA3
BA2	BFA2	BFA2	X	X	X	X	BFA2	BFA2
BA1	BFA1	BFA1	X	X	X	X	BFA1	BFA1
BA0	BFA0	BFA0	X	X	X	X	BFA0	BFA0
X	X	X						
X	X	X						
X	X	X						
X	X	X						
X	X	X						
X	X	X						
X	X	X						
X	X	X						
•								
•								
•								
X (64th bit)								

X (Don't Care)
r (reserved bits)

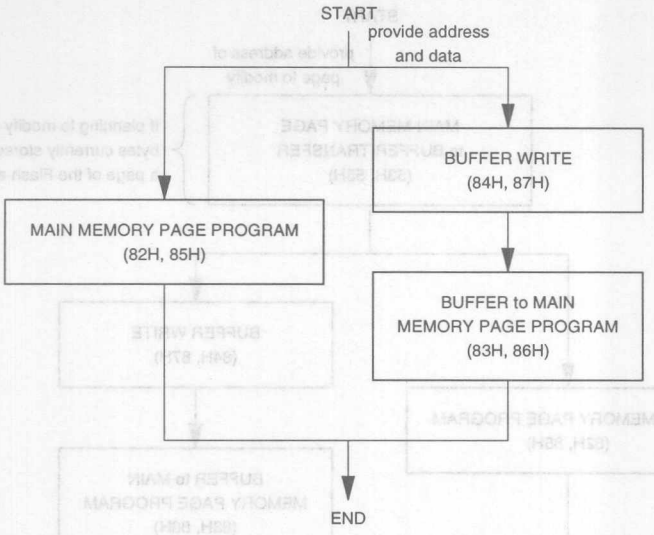
4

Table 2.

Buffer 1 to Main Memory Page Program with Built-In Erase	Buffer 2 to Main Memory Page Program with Built-In Erase	Buffer 1 to Main Memory Page Program without Built-In Erase	Buffer 2 to Main Memory Page Program without Built-In Erase	Main Memory Page Program Through Buffer 1	Main Memory Page Program Through Buffer 2	Auto Page Rewrite Through Buffer 1	Auto Page Rewrite Through Buffer 2	Status Register
Opcode								
83H	86H	88H	89H	82H	85H	58H	59H	57H
1	1	1	1	1	1	0	0	0
0	0	0	0	0	0	1	1	1
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1	1
0	0	1	1	0	0	1	1	0
0	1	0	0	0	1	0	0	1
1	1	0	0	1	0	0	0	1
1	0	0	1	0	1	0	1	1
r	r	r	r	r	r	r	r	
r	r	r	r	r	r	r	r	
r	r	r	r	r	r	r	r	
r	r	r	r	r	r	r	r	
PA10	PA10	PA10	PA10	PA10	PA10	PA10	PA10	
PA9	PA9	PA9	PA9	PA9	PA9	PA9	PA9	
PA8	PA8	PA8	PA8	PA8	PA8	PA8	PA8	
PA7	PA7	PA7	PA7	PA7	PA7	PA7	PA7	
PA6	PA6	PA6	PA6	PA6	PA6	PA6	PA6	
PA5	PA5	PA5	PA5	PA5	PA5	PA5	PA5	
PA4	PA4	PA4	PA4	PA4	PA4	PA4	PA4	
PA3	PA3	PA3	PA3	PA3	PA3	PA3	PA3	
PA2	PA2	PA2	PA2	PA2	PA2	PA2	PA2	
PA1	PA1	PA1	PA1	PA1	PA1	PA1	PA1	
PA0	PA0	PA0	PA0	PA0	PA0	PA0	PA0	
X	X	X	X	BA8	BA8	X	X	
X	X	X	X	BA7	BA7	X	X	
X	X	X	X	BA6	BA6	X	X	
X	X	X	X	BA5	BA5	X	X	
X	X	X	X	BA4	BA4	X	X	
X	X	X	X	BA3	BA3	X	X	
X	X	X	X	BA2	BA2	X	X	
X	X	X	X	BA1	BA1	X	X	
X	X	X	X	BA0	BA0	X	X	

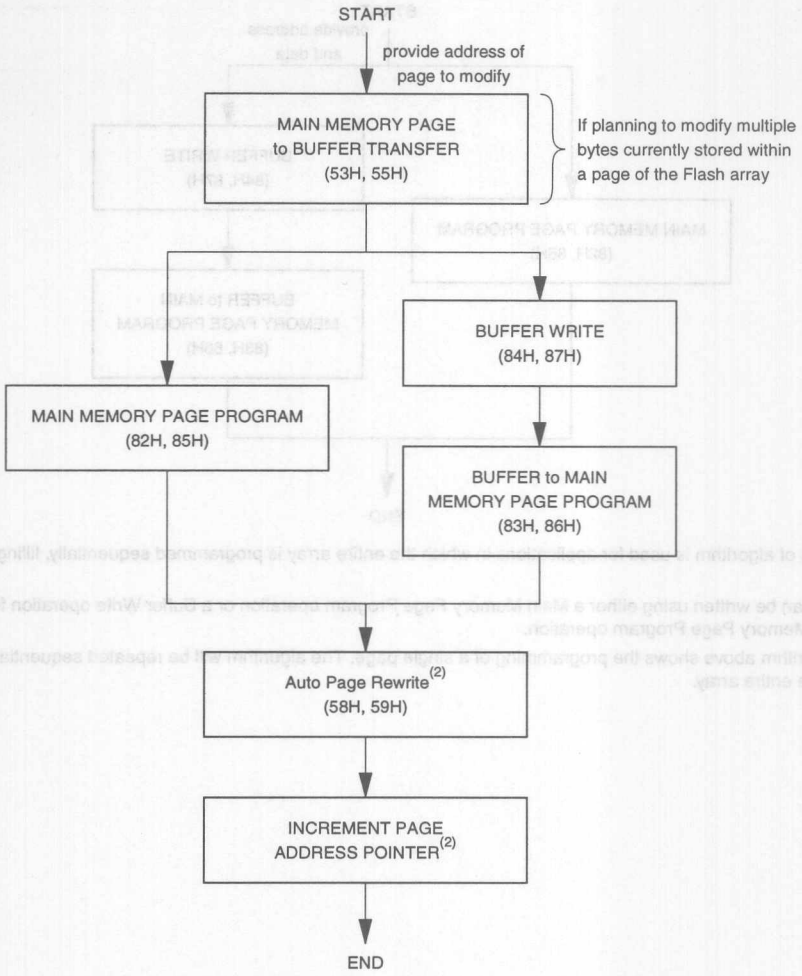
X (Don't Care)
r (reserved bits)

Figure 1. Algorithm for Programming or Reprogramming of the Entire Array Sequentially



Notes:
1. This type of algorithm is used for applications in which the entire array is programmed sequentially, filling the array page-by-page.
2. A page can be written using either a Main Memory Page Program operation or a Buffer Write operation followed by a Buffer to Main Memory Page Program operation.
3. The algorithm above shows the programming of a single page. The algorithm will be repeated sequentially for each page within the entire array.

Figure 2. Algorithm for Randomly Modifying Data



Notes:
1. To preserve data integrity, each page of the DataFlash memory array must be updated/rewritten at least once within every 10,000 cumulative page erase/program operations.
2. A Page Address Pointer must be maintained to indicate which page is to be rewritten. The Auto Page Rewrite command must use the address specified by the Page Address Pointer.
3. Other algorithms can be used to rewrite portions of the Flash array. Low power applications may choose to wait until 10,000 cumulative page erase/program operations have accumulated before rewriting all pages of the Flash array. See application note AN-4 ("Using Atmel's Serial DataFlash") for more details.

Ordering Information

f_{SCK} (MHz)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
10	25	0.04	AT45D041-JC AT45D041-RC AT45D041-TC	32J 28R 28T	Commercial (0°C to 70°C)
10	25	0.04	AT45D041-JI AT45D041-RI AT45D041-TI	32J 28R 28T	Industrial (-40°C to 85°C)

4

Package Type	
32J	32-Lead, Plastic J-Leaded Chip Carrier Package (PLCC)
28R	28-Lead, 0.330" Wide, Plastic Gull-Wing Small Outline Package (SOIC)
28T	28-Lead, Plastic Thin Small Outline Package (TSOP)

Ordering Information

f_{SCK} (MHz)	I_{CC} (mA) Active	I_{CC} (mA) Standby	Ordering Code	Package	Operation Range
10	25	0.01	AT45D041-JC AT45D041-RC AT45D041-TC	32J 28R 28T	Commercial (0°C to 70°C)
10	25	0.01	AT45D041-JI AT45D041-RI AT45D041-TI	32J 28R 28T	Industrial (-40°C to 85°C)

	Package Type
32J	32-Lead, Plastic J-Leaded Chip Carrier Package (PLCC)
28R	28-Lead, 0.330" Wide, Plastic Gull-Wing Small Outline Package (SOIC)
28T	28-Lead, Plastic Thin Small Outline Package (TSOP)

Features

- Single 4.5V - 5.5V Supply
- Serial Interface Architecture
- Page Program Operation
  - Single Cycle Reprogram (Erase and Program)
  - 4096 Pages (264 Bytes/Page) Main Memory
- Two 264-Byte SRAM Data Buffers – Allows Receiving of Data while Reprogramming of Nonvolatile Memory
- Internal Program and Control Timer
- Fast Page Program Time – 7 ms Typical
- 80 µs Typical Page to Buffer Transfer Time
- Low Power Dissipation
  - 15 mA Active Read Current Typical
  - 10 µA CMOS Standby Current Typical
- 10 MHz Max Clock Frequency
- Hardware Data Protection Feature
- Serial Peripheral Interface (SPI) Compatible – Modes 0 and 3
- CMOS and TTL Compatible Inputs and Outputs
- Commercial and Industrial Temperature Ranges

Description

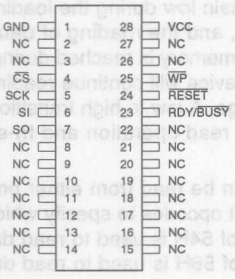
The AT45D081 is a 5-volt only, serial interface Flash memory suitable for in-system reprogramming. Its 8,650,752 bits of memory are organized as 4096 pages of 264-bytes each. In addition to the main memory, the AT45D081 also contains two data SRAM buffers of 264-bytes each. The buffers allow receiving of data while a page in the main memory is being reprogrammed. Unlike conventional Flash memories that are accessed randomly with multiple address lines and a parallel interface, the

(continued)

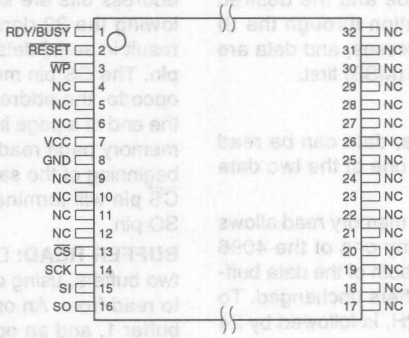
Pin Configurations

Pin Name	Function
$\overline{CS}$	Chip Select
SCK	Serial Clock
SI	Serial Input
SO	Serial Output
$\overline{WP}$	Hardware Page Write Protect Pin
$\overline{RESET}$	Chip Reset
RDY/$\overline{BUSY}$	Ready/Busy

SOIC



TSOP Top View
Type 1



8-Megabit 5-volt Only Serial DataFlash®

4

AT45D081

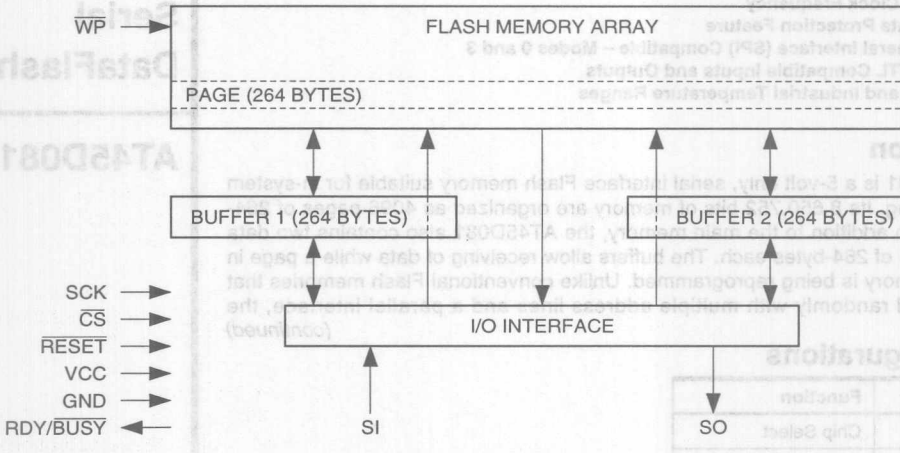
Rev. 0871B–10/98

DataFlash uses a serial interface to sequentially access its data. The simple serial interface facilitates hardware layout, increases system reliability, minimizes switching noise, and reduces package size and active pin count. The device is optimized for use in many commercial and industrial applications where high density, low pin count, low voltage, and low power are essential. Typical applications for the DataFlash are digital voice storage, image storage, and data storage. The device operates at clock frequencies up to 10 MHz with a typical active read current consumption of 15 mA.

To allow for simple in-system reprogrammability, the AT45D081 does not require high input voltages for programming. The device operates from a single power supply, 4.5V to 5.5V, for both the program and read operations. The AT45D081 is enabled through the chip select pin ($\overline{CS}$) and accessed via a three-wire interface consisting of the Serial Input (SI), Serial Output (SO), and the Serial Clock (SCK).

All programming cycles are self-timed, and no separate erase cycle is required before programming.

Block Diagram



Device Operation

The device operation is controlled by instructions from the host processor. The list of instructions and their associated opcodes are contained in Tables 1 and 2. A valid instruction starts with the falling edge of $\overline{CS}$ followed by the appropriate 8-bit opcode and the desired buffer or main memory address location. While the $\overline{CS}$ pin is low, toggling the SCK pin controls the loading of the opcode and the desired buffer or main memory address location through the SI (serial input) pin. All instructions, addresses, and data are transferred with the most significant bit (MSB) first.

Read

By specifying the appropriate opcode, data can be read from the main memory or from either one of the two data buffers.

MAIN MEMORY PAGE READ: A main memory read allows the user to read data directly from any one of the 4096 pages in the main memory, bypassing both of the data buffers and leaving the contents of the buffers unchanged. To start a page read, the 8-bit opcode, 52H, is followed by 24 address bits and 32 don't care bits. In the AT45D081, the first three address bits are reserved for larger density devices (see Notes on page 196), the next 12 address bits (PA11-PA0) specify the page address, and the next nine address bits (BA8-BA0) specify the starting byte address within the page. The 32 don't care bits which follow the 24 address bits are sent to initialize the read operation. Following the 32 don't care bits, additional pulses on SCK result in serial data being output on the SO (serial output) pin. The $\overline{CS}$ pin must remain low during the loading of the opcode, the address bits, and the reading of data. When the end of a page in main memory is reached during a main memory page read, the device will continue reading at the beginning of the same page. A low to high transition on the $\overline{CS}$ pin will terminate the read operation and tri-state the SO pin.

BUFFER READ: Data can be read from either one of the two buffers, using different opcodes to specify which buffer to read from. An opcode of 54H is used to read data from buffer 1, and an opcode of 56H is used to read data from

buffer 2. To perform a buffer read, the eight bits of the opcode must be followed by 15 don't care bits, nine address bits, and eight don't care bits. Since the buffer size is 264-bytes, nine address bits (BFA8-BFA0) are required to specify the first byte of data to be read from the buffer. The $\overline{CS}$ pin must remain low during the loading of the opcode, the address bits, the don't care bits, and the reading of data. When the end of a buffer is reached, the device will continue reading back at the beginning of the buffer. A low to high transition on the $\overline{CS}$ pin will terminate the read operation and tri-state the SO pin.

MAIN MEMORY PAGE TO BUFFER TRANSFER: A page of data can be transferred from the main memory to either buffer 1 or buffer 2. An 8-bit opcode, 53H for buffer 1 and 55H for buffer 2, is followed by the three reserved bits, 12 address bits (PA11-PA0) which specify the page in main memory that is to be transferred, and nine don't care bits. The $\overline{CS}$ pin must be low while toggling the SCK pin to load the opcode, the address bits, and the don't care bits from the SI pin. The transfer of the page of data from the main memory to the buffer will begin when the $\overline{CS}$ pin transitions from a low to a high state. During the transfer of a page of data (t_{XFR}), the status register can be read to determine whether the transfer has been completed or not.

MAIN MEMORY PAGE TO BUFFER COMPARE: A page of data in main memory can be compared to the data in buffer 1 or buffer 2. An 8-bit opcode, 60H for buffer 1 and 61H for buffer 2, is followed by 24 address bits consisting of the three reserved bits, 12 address bits (PA11-PA0) which specify the page in the main memory that is to be compared to the buffer, and nine don't care bits. The loading of the opcode and the address bits is the same as described previously. The $\overline{CS}$ pin must be low while toggling the SCK pin to load the opcode, the address bits, and the don't care bits from the SI pin. On the low to high transition of the $\overline{CS}$ pin, the 264 bytes in the selected main memory page will be compared with the 264 bytes in buffer 1 or buffer 2. During this time (t_{XFR}), the status register will indicate that the part is busy. On completion of the compare operation, bit 6 of the status register is updated with the result of the compare.

Program

BUFFER WRITE: Data can be shifted in from the SI pin into either buffer 1 or buffer 2. To load data into either buffer, an 8-bit opcode, 84H for buffer 1 or 87H for buffer 2, is followed by 15 don't care bits and nine address bits (BFA8-BFA0). The nine address bits specify the first byte in the buffer to be written. The data is entered following the address bits. If the end of the data buffer is reached, the device will wrap around back to the beginning of the buffer. Data will continue to be loaded into the buffer until a low to high transition is detected on the $\overline{CS}$ pin.

BUFFER TO MAIN MEMORY PAGE PROGRAM WITH BUILT-IN ERASE: Data written into either buffer 1 or buffer 2 can be programmed into the main memory. An 8-bit opcode, 83H for buffer 1 or 86H for buffer 2, is followed by the three reserved bits, 12 address bits (PA11-PA0) that specify the page in the main memory to be written, and nine additional don't care bits. When a low to high transition occurs on the $\overline{CS}$ pin, the part will first erase the selected page in main memory to all 1s and then program the data stored in the buffer into the specified page in the main memory. Both the erase and the programming of the page are internally self timed and should take place in a maximum time of t_{EP}. During this time, the status register will indicate that the part is busy.

BUFFER TO MAIN MEMORY PAGE PROGRAM WITHOUT BUILT-IN ERASE: A previously erased page within main memory can be programmed with the contents of either buffer 1 or buffer 2. An 8-bit opcode, 88H for buffer 1 or 89H for buffer 2, is followed by the three reserved bits, 12 address bits (PA11-PA0) that specify the page in the main memory to be written, and nine additional don't care bits. When a low to high transition occurs on the $\overline{CS}$ pin, the part will program the data stored in the buffer into the specified page in the main memory. It is necessary that the page in main memory that is being programmed has been previously programmed to all 1s (erased state). The programming of the page is internally self timed and should take place in a maximum time of t_P. During this time, the status register will indicate that the part is busy.

MAIN MEMORY PAGE PROGRAM: This operation is a combination of the Buffer Write and Buffer to Main Memory Page Program with Built-In Erase operations. Data is first shifted into buffer 1 or buffer 2 from the SI pin and then programmed into a specified page in the main memory. An 8-bit opcode, 82H for buffer 1 or 85H for buffer 2, is followed by the three reserved bits and 21 address bits. The 12 most significant address bits (PA11-PA0) select the page in the main memory where data is to be written, and the next nine address bits (BFA8-BFA0) select the first byte in the buffer to be written. After all address bits are shifted in, the part will take data from the SI pin and store it in one of the data buffers. If the end of the buffer is reached, the device will wrap around back to the beginning of the buffer. When there is a low to high transition on the $\overline{CS}$ pin, the part will first erase the selected page in main memory to all 1s and then program the data stored in the buffer into the specified page in the main memory. Both the erase and the programming of the page are internally self timed and should take place in a maximum of time t_{EP}. During this time, the status register will indicate that the part is busy.

AUTO PAGE REWRITE: This mode is only needed if multiple bytes within a page or multiple pages of data are modified in a random fashion. This mode is a combination of two operations: Main Memory Page to Buffer Transfer and

Buffer to Main Memory Page Program with Built-In Erase. A page of data is first transferred from the main memory to buffer 1 or buffer 2, and then the same data (from buffer 1 or buffer 2) is programmed back into its original page of main memory. An 8-bit opcode, 58H for buffer 1 or 59H for buffer 2, is followed by the three reserved bits, 12 address bits (PA11-PA0) that specify the page in main memory to be rewritten, and nine additional don't care bits. When a low to high transition occurs on the $\overline{CS}$ pin, the part will first transfer data from the page in main memory to a buffer and then program the data from the buffer back into same page of main memory. The operation is internally self-timed and should take place in a maximum time of t_{EP}. During this time, the status register will indicate that the part is busy.

If the main memory is programmed or reprogrammed sequentially page by page, then the programming algorithm shown in Figure 1 is recommended. Otherwise, if multiple bytes in a page or several pages are programmed randomly in the main memory, then the programming algorithm shown in Figure 2 is recommended.

STATUS REGISTER: The status register can be used to determine the device's ready/busy status, the result of a Main Memory Page to Buffer Compare operation, or the device density. To read the status register, an opcode of 57H must be loaded into the device. After the last bit of the opcode is shifted in, the eight bits of the status register, starting with the MSB (bit 7), will be shifted out on the SO pin during the next eight clock cycles. The five most-significant bits of the status register will contain device information, while the remaining three least-significant bits are reserved for future use and will have undefined values. After bit 0 of the status register has been shifted out, the sequence will repeat itself (as long as $\overline{CS}$ remains low and SCK is being toggled) starting again with bit 7. The data in the status register is constantly updated, so each repeating sequence will output new data.

Ready/busy status is indicated using bit 7 of the status register. If bit 7 is a 1, then the device is not busy and is ready to accept the next command. If bit 7 is a 0, then the device is in a busy state. The user can continuously poll bit 7 of the status register by stopping SCK once bit 7 has been output. The status of bit 7 will continue to be output on the SO pin, and once the device is no longer busy, the state of SO will change from 0 to 1. There are six operations which can cause the device to be in a busy state: Main Memory Page to Buffer Transfer, Main Memory Page to Buffer Compare, Buffer to Main Memory Page Program with Built-In Erase, Buffer to Main Memory Page Program without Built-In Erase, Main Memory Page Program, and Auto Page Rewrite.

The result of the most recent Main Memory Page to Buffer Compare operation is indicated using bit 6 of the status register. If bit 6 is a 0, then the data in the main memory page matches the data in the buffer. If bit 6 is a 1, then at least one bit of the data in the main memory page does not match the data in the buffer.

The device density is indicated using bits 5, 4, and 3 of the status register. For the AT45D081, the three bits are 1, 0, and 0. The decimal value of these three binary bits does not equate to the device density; the three bits represent a combinational code relating to differing densities of Serial DataFlash devices, allowing a total of eight different density configurations.

Read/Program Mode Summary

The modes listed above can be separated into two groups — modes which make use of the flash memory array (Group A) and modes which do not make use of the flash memory array (Group B).

Group A modes consist of:

1. Main memory page read
2. Main memory page to buffer 1 (or 2) transfer
3. Main memory page to buffer 1 (or 2) compare
4. Buffer 1 (or 2) to main memory page program with built-in erase
5. Buffer 1 (or 2) to main memory page program without built-in erase
6. Main memory page program
7. Auto page rewrite

Group B modes consist of:

1. Buffer 1 (or 2) read
2. Buffer 1 (or 2) write
3. Status read

If a Group A mode is in progress (not fully completed) then another mode in Group A should not be started. However, during this time in which a Group A mode is in progress, modes in Group B can be started.

This gives the Serial DataFlash the ability to virtually accommodate a continuous data stream. While data is being programmed into main memory from buffer 1, data can be loaded into buffer 2 (or vice versa). See application note AN-4 ("Using Atmel's Serial DataFlash") for more details.

Status Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RDY/$\overline{BUSY}$	COMP	1	0	0	X	X	X

HARDWARE PAGE WRITE PROTECT: If the $\overline{WP}$ pin is held low, the first 256 pages of the main memory cannot be reprogrammed. The only way to reprogram the first 256 pages is to first drive the protect pin high and then use the program commands previously mentioned. The $\overline{WP}$ pin is internally pulled high; therefore, connection of the $\overline{WP}$ pin is not necessary if this pin and feature will not be utilized. However, it is recommended that the $\overline{WP}$ pin be driven high externally whenever possible.

$\overline{RESET}$: A low state on the reset pin ($\overline{RESET}$) will terminate the operation in progress and reset the internal state machine to an idle state. The device will remain in the reset condition as long as a low level is present on the $\overline{RESET}$ pin. Normal operation can resume once the $\overline{RESET}$ pin is brought back to a high level.

The device also incorporates an internal power-on reset circuit, so there are no restrictions on the $\overline{RESET}$ pin during power-on sequences. The $\overline{RESET}$ pin is also internally pulled high; therefore, connection of the $\overline{RESET}$ pin is not necessary if this pin and feature will not be utilized. However, it is recommended that the $\overline{RESET}$ pin be driven high externally whenever possible.

READY/$\overline{BUSY}$: This open drain output pin will be driven low when the device is busy in an internally self-timed operation. This pin, which is normally in a high state (through an external pull-up resistor), will be pulled low during programming operations, compare operations, and during page-to-buffer transfers.

The busy status indicates that the Flash memory array and one of the buffers cannot be accessed; read and write operations to the other buffer can still be performed.

Power On/Reset State

When power is first applied to the device, or when recovering from a reset condition, the device will default to SPI mode 3. In addition, the SO pin will be in a high impedance state, and a high to low transition on the $\overline{CS}$ pin will be required to start a valid instruction. The SPI mode will be automatically selected on every falling edge of $\overline{CS}$ by sampling the inactive clock state.

4

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC and AC Operating Range

		AT45D081
Operating Temperature (Case)	Com.	0°C to 70°C
	Ind.	-40°C to 85°C
V_{CC} Power Supply[1]		4.5V to 5.5V

Note: 1. After power is applied and V_{CC} is at the minimum specified data sheet value, the system should wait 20 ms before an operational mode is started.

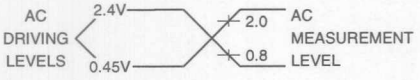
DC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{SB}	Standby Current	$\overline{CS}$, $\overline{RESET}$, $\overline{WP}$ = V_{IH}, all inputs at CMOS levels		10	20	µA
I_{CC1}	Active Current, Read Operation	f = 10 MHz; I_{OUT} = 0 mA; V_{CC} = 5.5V		15	25	mA
I_{CC2}	Active Current, Program/Erase Operation	V_{CC} = 5.5V		25	50	mA
I_{LI}	Input Load Current	V_{IN} = CMOS levels			10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = CMOS levels			10	µA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage		2.0			V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			0.45	V
V_{OH1}	Output High Voltage	I_{OH} = -400 µA	2.4			V
V_{OH2}	Output High Voltage	I_{OH} = -100 µA; V_{CC} = 4.5V	4.2			V

AC Characteristics

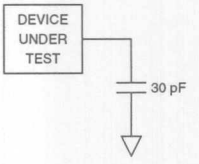
Symbol	Parameter	Min	Typ	Max	Units
f_{SCK}	SCK Frequency			10	MHz
t_{WH}	SCK High Time	40			ns
t_{WL}	SCK Low Time	40			ns
t_{CS}	Minimum $\overline{CS}$ High Time	250			ns
t_{CSS}	$\overline{CS}$ Setup Time	250			ns
t_{CSH}	$\overline{CS}$ Hold Time	250			ns
t_{CSB}	CS High to RDY/$\overline{BUSY}$ Low			200	ns
t_{SU}	Data In Setup Time	10			ns
t_H	Data In Hold Time	25			ns
t_{HO}	Output Hold Time	0			ns
t_{DIS}	Output Disable Time			75	ns
t_V	Output Valid			80	ns
t_{XFR}	Page to Buffer Transfer/Compare Time		80	150	µs
t_{EP}	Page Erase and Programming Time		10	20	ms
t_P	Page Programming Time		7	14	ms
t_{RST}	$\overline{RESET}$ Pulse Width	10			µs
t_{REC}	$\overline{RESET}$ Recovery Time			1	µs

Input Test Waveforms and Measurement Levels



t_R, t_F < 20 ns (10% to 90%)

Output Test Load

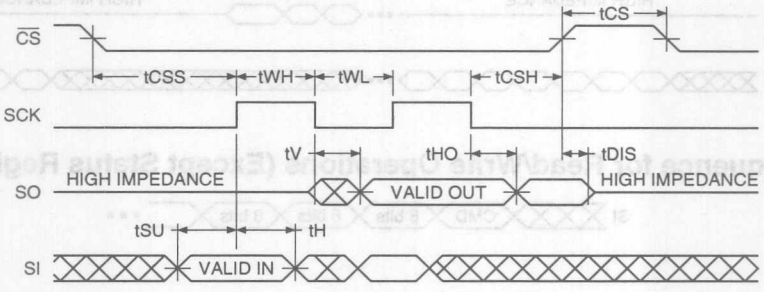


AC Waveforms

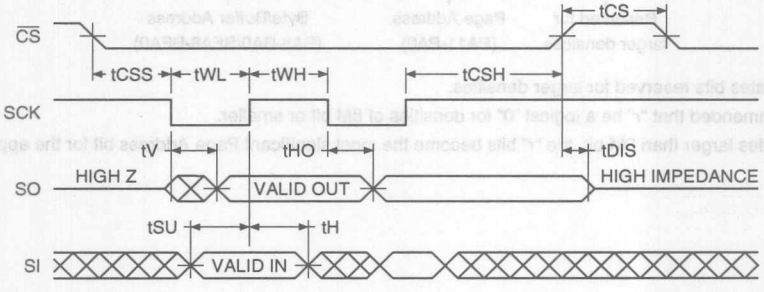
Two different timing diagrams are shown below. Waveform 1 shows the SCK signal being low when $\overline{CS}$ makes a high-to-low transition, and Waveform 2 shows the SCK signal being high when $\overline{CS}$ makes a high-to-low transition. Both wavforms show valid timing diagrams. The setup and hold times for the SI signal are referenced to the low-to-high transition on the SCK signal.

Waveform 1 shows timing that is also compatible with SPI Mode 0, and Waveform 2 shows timing that is compatible with SPI Mode 3.

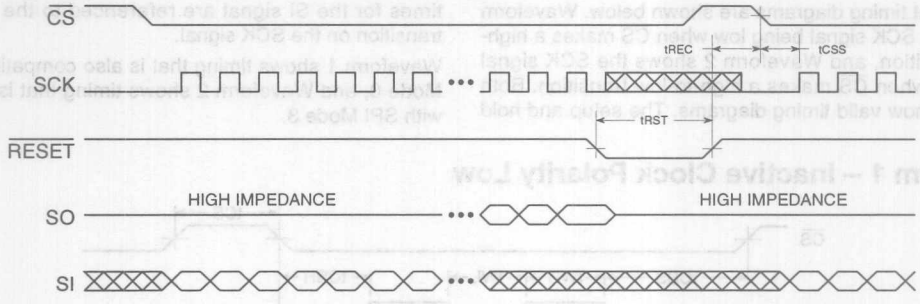
Waveform 1 – Inactive Clock Polarity Low



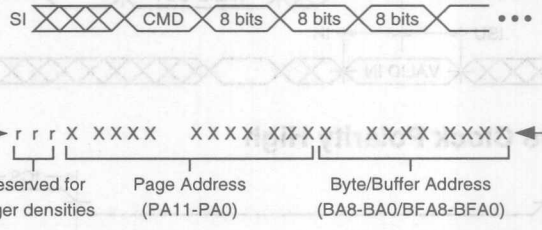
Waveform 2 – Inactive Clock Polarity High



Reset Timing (Inactive Clock Polarity Low Shown)



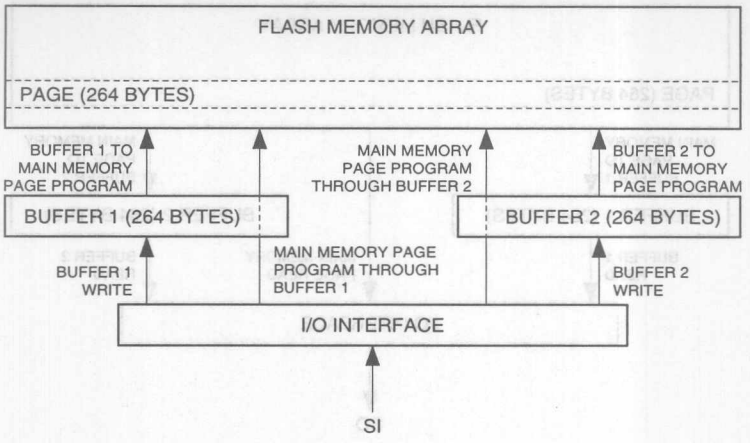
Command Sequence for Read/Write Operations (Except Status Register Read)



Notes:
1. "r" designates bits reserved for larger densities.
2. It is recommended that "r" be a logical "0" for densities of 8M bit or smaller.
3. For densities larger than 8M bit, the "r" bits become the most significant Page Address bit for the appropriate density.

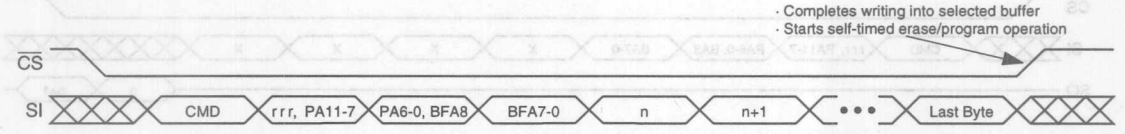
Write Operations

The following block diagram and waveforms illustrate the various write sequences available.

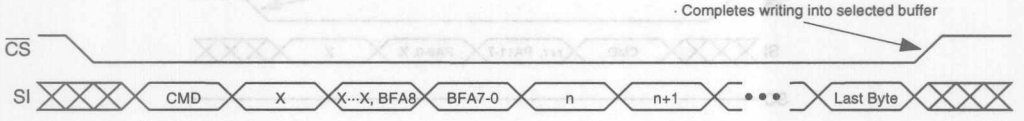


4

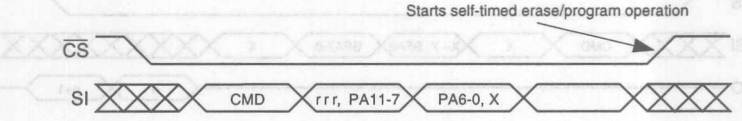
Main Memory Page Program through Buffers



Buffer Write



Buffer to Main Memory Page Program (Data from Buffer Programmed into Flash Page)

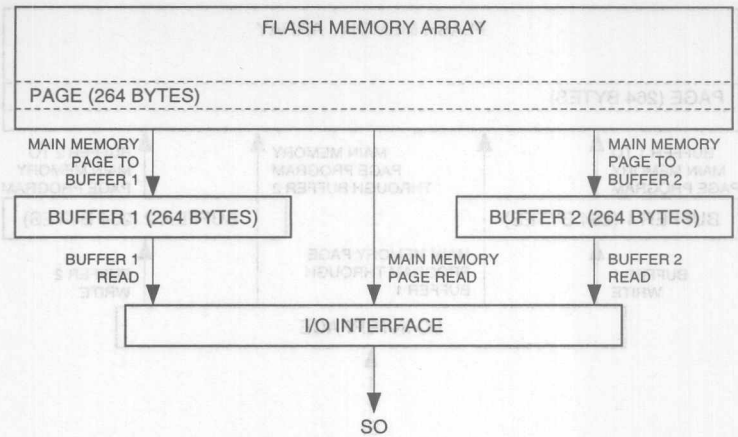


Each transition represents 8 bits and 8 clock cycles

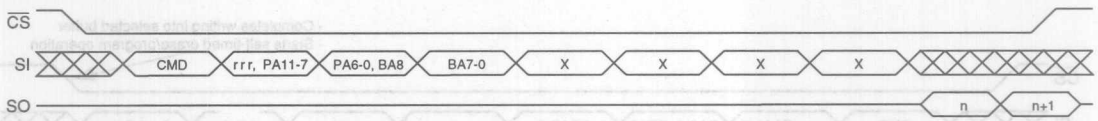
n = 1st byte read
n+1 = 2nd byte read

Read Operations

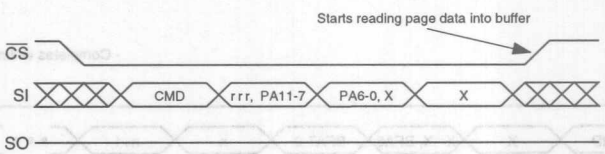
The following block diagram and waveforms illustrate the various read sequences available.



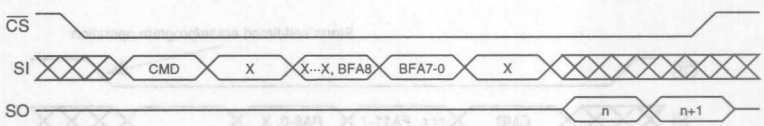
Main Memory Page Read



Main Memory Page to Buffer Transfer (Data from Flash Page Read into Buffer)



Buffer Read

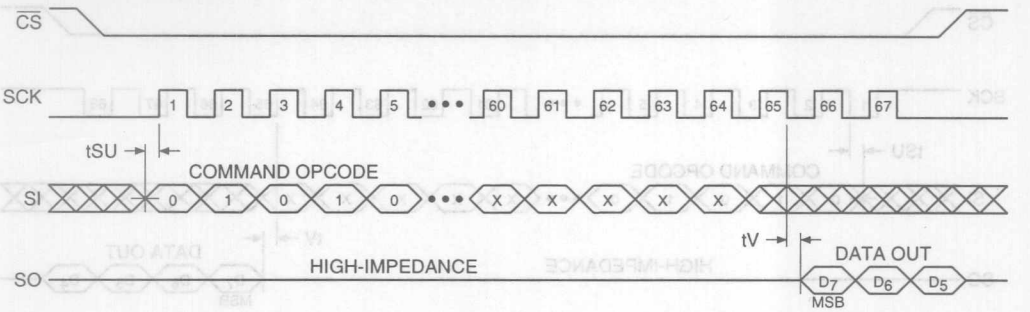


Each transition represents 8 bits and 8 clock cycles

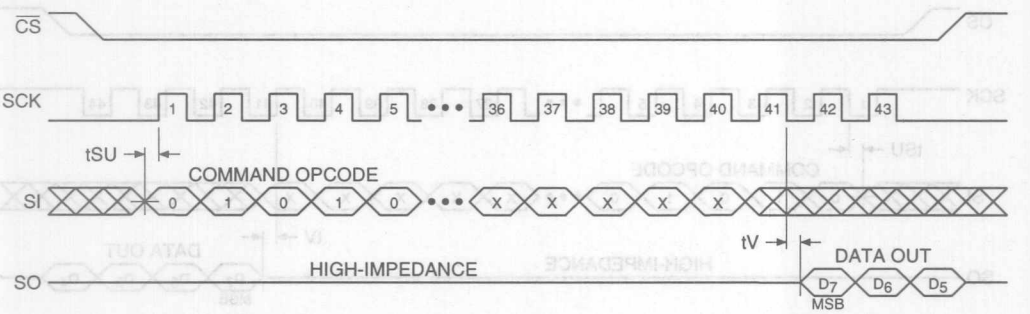
n = 1st byte read
n+1 = 2nd byte read

Detailed Bit-Level Read Timing – Inactive Clock Polarity Low

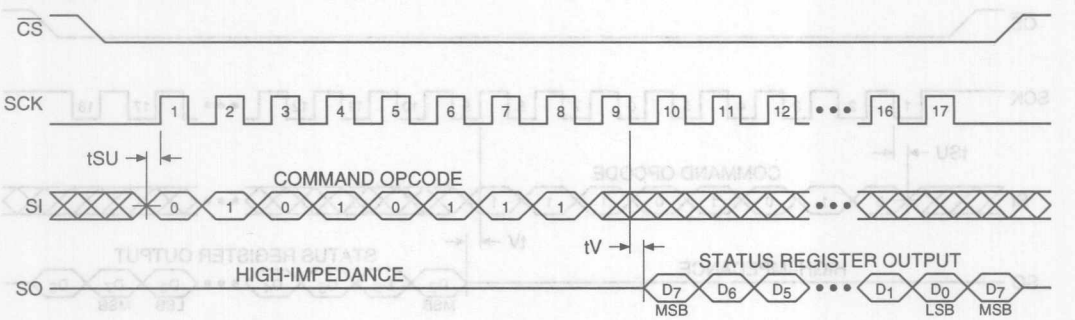
Main Memory Page Read



Buffer Read

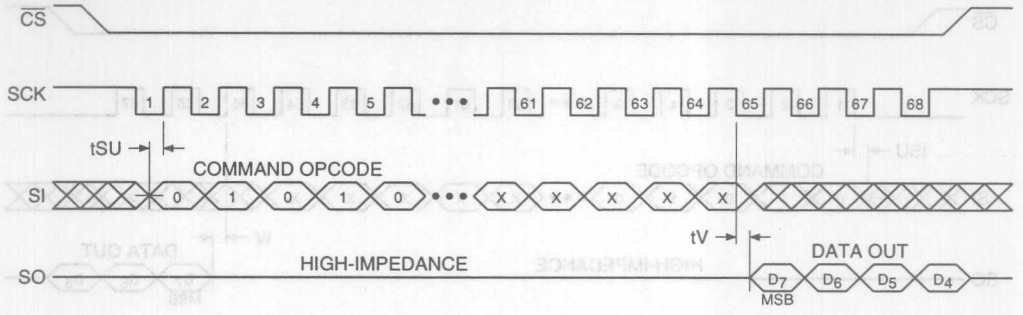


Status Register Read

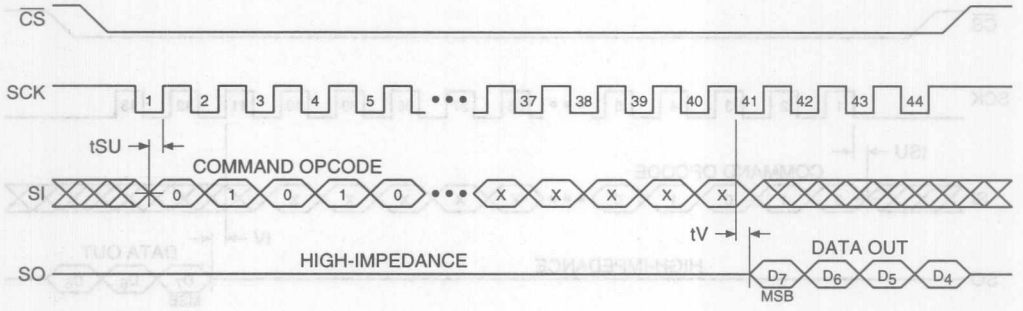


Detailed Bit-Level Read Timing – Inactive Clock Polarity High

Main Memory Page Read



Buffer Read



Status Register Read

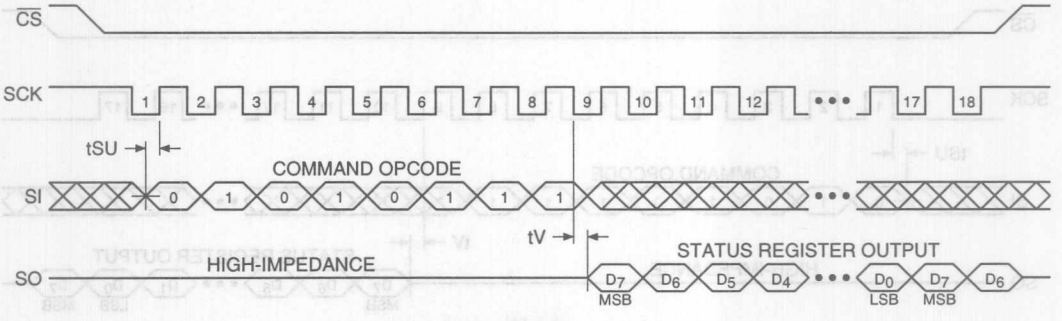


Table 1.

Main Memory Page Read	Buffer 1 Read	Buffer 2 Read	Main Memory Page to Buffer 1 Transfer	Main Memory Page to Buffer 2 Transfer	Main Memory Page to Buffer 1 Compare	Main Memory Page to Buffer 2 Compare	Buffer 1 Write	Buffer 2 Write
				Opcode				
52H	54H	56H	53H	55H	60H	61H	84H	87H
0	0	0	0	0	0	0	1	1
1	1	1	1	1	1	1	0	0
0	0	0	0	0	1	1	0	0
1	1	1	1	1	0	0	0	0
0	0	0	0	0	0	0	0	0
0	1	1	0	1	0	0	1	1
1	0	1	1	0	0	0	0	1
0	0	0	1	1	0	1	0	1
r	X	X	r	r	r	r	X	X
r	X	X	r	r	r	r	X	X
r	X	X	r	r	r	r	X	X
PA11	X	X	PA11	PA11	PA11	PA11	X	X
PA10	X	X	PA10	PA10	PA10	PA10	X	X
PA9	X	X	PA9	PA9	PA9	PA9	X	X
PA8	X	X	PA8	PA8	PA8	PA8	X	X
PA7	X	X	PA7	PA7	PA7	PA7	X	X
PA6	X	X	PA6	PA6	PA6	PA6	X	X
PA5	X	X	PA5	PA5	PA5	PA5	X	X
PA4	X	X	PA4	PA4	PA4	PA4	X	X
PA3	X	X	PA3	PA3	PA3	PA3	X	X
PA2	X	X	PA2	PA2	PA2	PA2	X	X
PA1	X	X	PA1	PA1	PA1	PA1	X	X
PA0	X	X	PA0	PA0	PA0	PA0	X	X
BA8	BFA8	BFA8	X	X	X	X	BFA8	BFA8
BA7	BFA7	BFA7	X	X	X	X	BFA7	BFA7
BA6	BFA6	BFA6	X	X	X	X	BFA6	BFA6
BA5	BFA5	BFA5	X	X	X	X	BFA5	BFA5
BA4	BFA4	BFA4	X	X	X	X	BFA4	BFA4
BA3	BFA3	BFA3	X	X	X	X	BFA3	BFA3
BA2	BFA2	BFA2	X	X	X	X	BFA2	BFA2
BA1	BFA1	BFA1	X	X	X	X	BFA1	BFA1
BA0	BFA0	BFA0	X	X	X	X	BFA0	BFA0
X	X	X						
X	X	X						
X	X	X						
X	X	X						
X	X	X						
X	X	X						
X	X	X						
X	X	X						
•								
•								
•								
X (64th bit)								

X (Don't Care)
r (reserved bits)

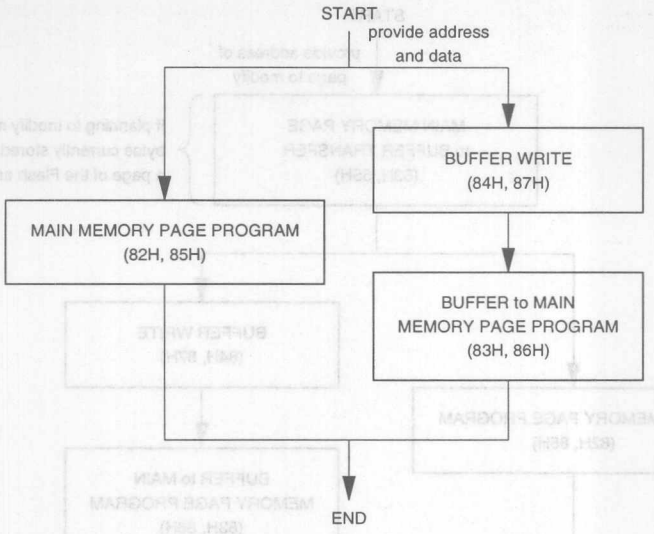
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Table 2.

Buffer 1 to Main Memory Page Program with Built-In Erase	Buffer 2 to Main Memory Page Program with Built-In Erase	Buffer 1 to Main Memory Page Program without Built-In Erase	Buffer 2 to Main Memory Page Program without Built-In Erase	Main Memory Page Program Through Buffer 1	Main Memory Page Program Through Buffer 2	Auto Page Rewrite Through Buffer 1	Auto Page Rewrite Through Buffer 2	Status Register
Opcode								
83H	86H	88H	89H	82H	85H	58H	59H	57H
1	1	1	1	1	1	0	0	0
0	0	0	0	0	0	1	1	1
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1	1
0	0	1	1	0	0	1	1	0
0	1	0	0	0	1	0	0	1
1	1	0	0	1	0	0	0	1
1	0	0	1	0	1	0	1	1
r	r	r	r	r	r	r	r	
r	r	r	r	r	r	r	r	
r	r	r	r	r	r	r	r	
PA11	PA11	PA11	PA11	PA11	PA11	PA11	PA11	
PA10	PA10	PA10	PA10	PA10	PA10	PA10	PA10	
PA9	PA9	PA9	PA9	PA9	PA9	PA9	PA9	
PA8	PA8	PA8	PA8	PA8	PA8	PA8	PA8	
PA7	PA7	PA7	PA7	PA7	PA7	PA7	PA7	
PA6	PA6	PA6	PA6	PA6	PA6	PA6	PA6	
PA5	PA5	PA5	PA5	PA5	PA5	PA5	PA5	
PA4	PA4	PA4	PA4	PA4	PA4	PA4	PA4	
PA3	PA3	PA3	PA3	PA3	PA3	PA3	PA3	
PA2	PA2	PA2	PA2	PA2	PA2	PA2	PA2	
PA1	PA1	PA1	PA1	PA1	PA1	PA1	PA1	
PA0	PA0	PA0	PA0	PA0	PA0	PA0	PA0	
X	X	X	X	BA8	BA8	X	X	
X	X	X	X	BA7	BA7	X	X	
X	X	X	X	BA6	BA6	X	X	
X	X	X	X	BA5	BA5	X	X	
X	X	X	X	BA4	BA4	X	X	
X	X	X	X	BA3	BA3	X	X	
X	X	X	X	BA2	BA2	X	X	
X	X	X	X	BA1	BA1	X	X	
X	X	X	X	BA0	BA0	X	X	

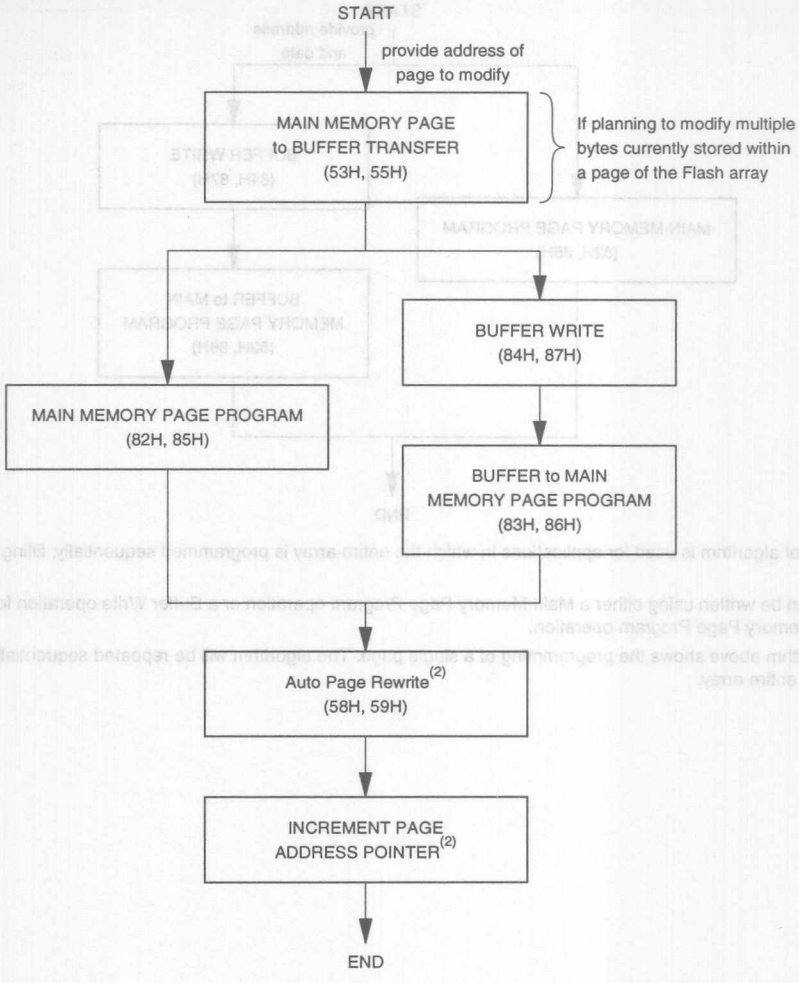
X (Don't Care)
r (reserved bits)

Figure 1. Algorithm for Programming or Reprogramming of the Entire Array Sequentially



Notes:
1. This type of algorithm is used for applications in which the entire array is programmed sequentially, filling the array page-by-page.
2. A page can be written using either a Main Memory Page Program operation or a Buffer Write operation followed by a Buffer to Main Memory Page Program operation.
3. The algorithm above shows the programming of a single page. The algorithm will be repeated sequentially for each page within the entire array.

Figure 2. Algorithm for Randomly Modifying Data



Notes:
1. To preserve data integrity, each page of the DataFlash memory array must be updated/rewritten at least once within every 10,000 cumulative page erase/program operations.
2. A Page Address Pointer must be maintained to indicate which page is to be rewritten. The Auto Page Rewrite command must use the address specified by the Page Address Pointer.
3. Other algorithms can be used to rewrite portions of the Flash array. Low power applications may choose to wait until 10,000 cumulative page erase/program operations have accumulated before rewriting all pages of the Flash array. See application note AN-4 ("Using Atmel's Serial DataFlash") for more details.

Ordering Information

f_{SCK} (MHz)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
10	25	0.02	AT45D081-RC AT45D081-TC	28R 32T	Commercial (0°C to 70°C)
10	25	0.02	AT45D081-RI AT45D081-TI	28R 32T	Industrial (-40°C to 85°C)

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Package Type	
28R	28-Lead, 0.330" Wide, Plastic Gull-Wing Small Outline Package (SOIC)
32T	32-Lead, Plastic Thin Small Outline Package (TSOP)

Ordering Information

f_{SCK} (MHz)	I_{CC} (mA)		Ordering Code	Package	Operation Range
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Package Type	
28R	28-Lead, 0.330" Wide, Plastic Gull-Wing Small Outline Package (SOIC)
28T	28-Lead, Plastic Thin Small Outline Package (TSOP)

Features

- Single 4.5V - 5.5V Supply
- Serial Interface Architecture
- Page Program Operation
  - Single Cycle Reprogram (Erase and Program)
  - 4096 Pages (528 Bytes/Page) Main Memory
- Optional Page and Block Erase Operations
- Two 528-Byte SRAM Data Buffers – Allows Receiving of Data while Reprogramming of Nonvolatile Memory
- Internal Program and Control Timer
- Fast Page Program Time – 7 ms Typical
- 120 µs Typical Page to Buffer Transfer Time
- Low Power Dissipation
  - 15 mA Active Read Current Typical
  - 10 µA CMOS Standby Current Typical
- 15 MHz Max Clock Frequency
- Hardware Data Protection Feature
- Serial Peripheral Interface (SPI) Compatible – Modes 0 and 3
- CMOS and TTL Compatible Inputs and Outputs
- Commercial and Industrial Temperature Ranges

Description

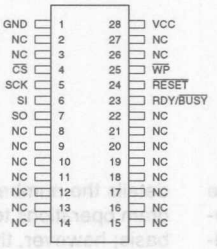
The AT45D161 is a 5-volt only, serial interface Flash memory suitable for in-system reprogramming. Its 17,301,504 bits of memory are organized as 4096 pages of 528 bytes each. In addition to the main memory, the AT45D161 also contains two SRAM data buffers of 528 bytes each. The buffers allow receiving of data while a page in the main memory is being reprogrammed. Unlike conventional Flash memories that are

(continued)

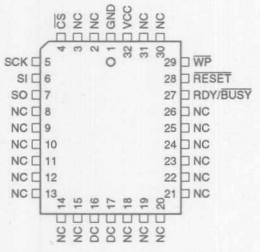
Pin Configurations

Pin Name	Function
$\overline{CS}$	Chip Select
SCK	Serial Clock
SI	Serial Input
SO	Serial Output
$\overline{WP}$	Hardware Page Write Protect Pin
$\overline{RESET}$	Chip Reset
RDY/$\overline{BUSY}$	Ready/Busy

SOIC

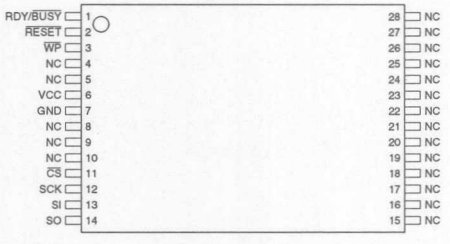


PLCC



Note: PLCC package pins 16 and 17 are DON'T CONNECT

TSOP Top View
Type 1



16-Megabit 5-volt Only Serial DataFlash®

4

AT45D161 Preliminary

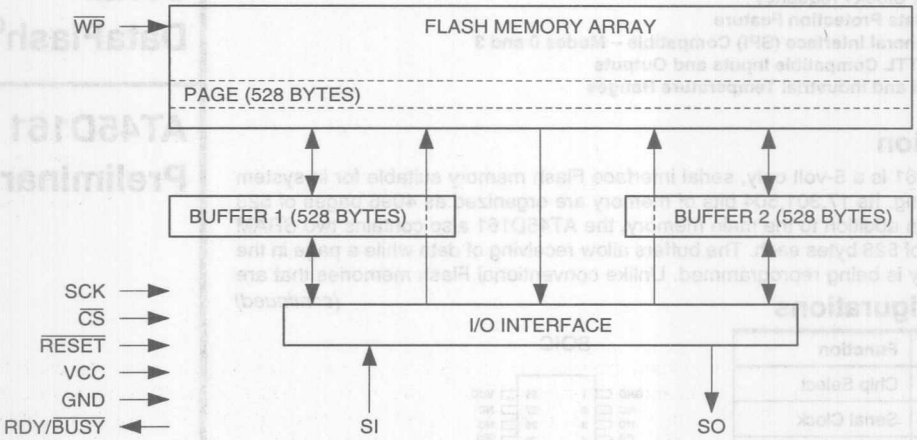
Rev. 1081A–06/98

accessed randomly with multiple address lines and a parallel interface, the DataFlash uses a serial interface to sequentially access its data. The simple serial interface facilitates hardware layout, increases system reliability, minimizes switching noise, and reduces package size and active pin count. The device is optimized for use in many commercial and industrial applications where high density, low pin count, low voltage, and low power are essential. Typical applications for the DataFlash are digital voice storage, image storage, and data storage. The device operates at clock frequencies up to 15 MHz with a typical active read current consumption of 15 mA.

To allow for simple in-system reprogrammability, the AT45D161 does not require high input voltages for programming. The device operates from a single power supply, 4.5V to 5.5V, for both the program and read operations. The AT45D161 is enabled through the chip select pin ($\overline{CS}$) and accessed via a three-wire interface consisting of the Serial Input (SI), Serial Output (SO), and the Serial Clock (SCK).

All programming cycles are self-timed, and no separate erase cycle is required before programming.

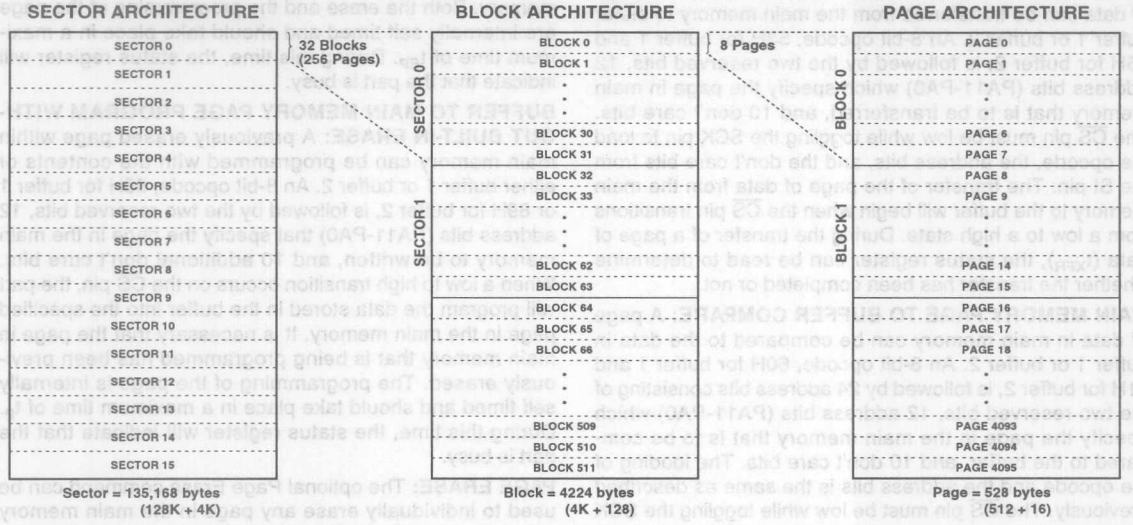
Block Diagram



Memory Array

To provide optimal flexibility, the memory array of the AT45D161 is divided into three levels of granularity comprising of sectors, blocks, and pages. The Memory Architecture Diagram illustrates the breakdown of each level and details the number of pages per sector and block. All program operations to the DataFlash occur on a page by page basis; however, the optional erase operations can be performed at the block or page level.

Memory Architecture Diagram



Device Operation

The device operation is controlled by instructions from the host processor. The list of instructions and their associated opcodes are contained in Table 1 and Table 2. A valid instruction starts with the falling edge of $\overline{CS}$ followed by the appropriate 8-bit opcode and the desired buffer or main memory address location. While the $\overline{CS}$ pin is low, toggling the SCK pin controls the loading of the opcode and the desired buffer or main memory address location through the SI (serial input) pin. All instructions, addresses, and data are transferred with the most significant bit (MSB) first.

Read

By specifying the appropriate opcode, data can be read from the main memory or from either one of the two data buffers.

MAIN MEMORY PAGE READ: A main memory read allows the user to read data directly from any one of the 4096 pages in the main memory, bypassing both of the data buffers and leaving the contents of the buffers unchanged. To start a page read, the 8-bit opcode, 52H, is followed by 24 address bits and 32 don't care bits. In the AT45D161, the first two address bits are reserved for larger density devices (see Notes on page 216), the next 12 address bits (PA11-PA0) specify the page address, and the next 10 address bits (BA9-BA0) specify the starting byte address within the page. The 32 don't care bits which follow the 24 address bits are sent to initialize the read operation. Following the 32 don't care bits, additional pulses on SCK result in serial data being output on the SO (serial output) pin. The $\overline{CS}$ pin must remain low during the loading of the opcode, the address bits, and the reading of data. When the end of a page in main memory is reached during a main memory page read, the device will continue reading at the beginning of the same page. A low to high transition on the $\overline{CS}$ pin will terminate the read operation and tri-state the SO pin.

BUFFER READ: Data can be read from either one of the two buffers, using different opcodes to specify which buffer to read from. An opcode of 54H is used to read data from buffer 1, and an opcode of 56H is used to read data from buffer 2. To perform a buffer read, the eight bits of the opcode must be followed by 14 don't care bits, 10 address bits, and eight don't care bits. Since the buffer size is 528-bytes, 10 address bits (BFA9-BFA0) are required to specify the first byte of data to be read from the buffer. The $\overline{CS}$ pin must remain low during the loading of the opcode, the address bits, the don't care bits, and the reading of data. When the end of a buffer is reached, the device will continue reading back at the beginning of the buffer. A low to

high transition on the $\overline{CS}$ pin will terminate the read operation and tri-state the SO pin.

MAIN MEMORY PAGE TO BUFFER TRANSFER: A page of data can be transferred from the main memory to either buffer 1 or buffer 2. An 8-bit opcode, 53H for buffer 1 and 55H for buffer 2, is followed by the two reserved bits, 12 address bits (PA11-PA0) which specify the page in main memory that is to be transferred, and 10 don't care bits. The $\overline{CS}$ pin must be low while toggling the SCK pin to load the opcode, the address bits, and the don't care bits from the SI pin. The transfer of the page of data from the main memory to the buffer will begin when the $\overline{CS}$ pin transitions from a low to a high state. During the transfer of a page of data (t_{XFR}), the status register can be read to determine whether the transfer has been completed or not.

MAIN MEMORY PAGE TO BUFFER COMPARE: A page of data in main memory can be compared to the data in buffer 1 or buffer 2. An 8-bit opcode, 60H for buffer 1 and 61H for buffer 2, is followed by 24 address bits consisting of the two reserved bits, 12 address bits (PA11-PA0) which specify the page in the main memory that is to be compared to the buffer, and 10 don't care bits. The loading of the opcode and the address bits is the same as described previously. The $\overline{CS}$ pin must be low while toggling the SCK pin to load the opcode, the address bits, and the don't care bits from the SI pin. On the low to high transition of the $\overline{CS}$ pin, the 528 bytes in the selected main memory page will be compared with the 528 bytes in buffer 1 or buffer 2. During this time (t_{XFR}), the status register will indicate that the part is busy. On completion of the compare operation, bit 6 of the status register is updated with the result of the compare.

Program

BUFFER WRITE: Data can be shifted in from the SI pin into either buffer 1 or buffer 2. To load data into either buffer, an 8-bit opcode, 84H for buffer 1 or 87H for buffer 2, is followed by 14 don't care bits and 10 address bits (BFA9-BFA0). The 10 address bits specify the first byte in the buffer to be written. The data is entered following the address bits. If the end of the data buffer is reached, the device will wrap around back to the beginning of the buffer. Data will continue to be loaded into the buffer until a low to high transition is detected on the $\overline{CS}$ pin.

BUFFER TO MAIN MEMORY PAGE PROGRAM WITH BUILT-IN ERASE: Data written into either buffer 1 or buffer 2 can be programmed into the main memory. An 8-bit opcode, 83H for buffer 1 or 86H for buffer 2, is followed by the two reserved bits, 12 address bits (PA11-PA0) that specify the page in the main memory to be written, and 10 additional don't care bits. When a low to high transition occurs on the $\overline{CS}$ pin, the part will first erase the selected page in main memory to all 1s and then program the data stored in the buffer into the specified page in the main memory. Both the erase and the programming of the page are internally self timed and should take place in a maximum time of t_{EP}. During this time, the status register will indicate that the part is busy.

BUFFER TO MAIN MEMORY PAGE PROGRAM WITHOUT BUILT-IN ERASE: A previously erased page within main memory can be programmed with the contents of either buffer 1 or buffer 2. An 8-bit opcode, 88H for buffer 1 or 89H for buffer 2, is followed by the two reserved bits, 12 address bits (PA11-PA0) that specify the page in the main memory to be written, and 10 additional don't care bits. When a low to high transition occurs on the $\overline{CS}$ pin, the part will program the data stored in the buffer into the specified page in the main memory. It is necessary that the page in main memory that is being programmed has been previously erased. The programming of the page is internally self timed and should take place in a maximum time of t_P. During this time, the status register will indicate that the part is busy.

PAGE ERASE: The optional Page Erase command can be used to individually erase any page in the main memory array allowing the Buffer to Main Memory Page Program without Built-In Erase command to be utilized at a later time. To perform a Page Erase, an opcode of 81H must be loaded into the device, followed by two reserved bits, 12 address bits (PA11-PA0), and 10 don't care bits. The 12 address bits are used to specify which page of the memory array is to be erased. When a low to high transition occurs on the $\overline{CS}$ pin, the part will erase the selected page to 1s. The erase operation is internally self-timed and should take place in a maximum time of t_{PE}. During this time, the status register will indicate that the part is busy.

BLOCK ERASE: A block of eight pages can be erased at one time allowing the Buffer to Main Memory Page Program without Built-In Erase command to be utilized to reduce programming times when writing large amounts of data to the device. To perform a Block Erase, an opcode of 50H must be loaded into the device, followed by two reserved bits, nine address bits (PA11-PA3), and 13 don't care bits. The nine address bits are used to specify which block of eight pages is to be erased. When a low to high transition occurs on the $\overline{CS}$ pin, the part will erase the selected block of eight pages to 1s. The erase operation is internally self-timed and should take place in a maximum time of t_{BE}. During this time, the status register will indicate that the part is busy.

Block Erase Addressing

PA11	PA10	PA9	PA8	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	Block
0	0	0	0	0	0	0	0	0	X	X	X	0
0	0	0	0	0	0	0	0	1	X	X	X	1
0	0	0	0	0	0	0	1	0	X	X	X	2
0	0	0	0	0	0	0	1	1	X	X	X	3
•	•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•	•
1	1	1	1	1	1	1	0	0	X	X	X	508
1	1	1	1	1	1	1	0	1	X	X	X	509
1	1	1	1	1	1	1	1	0	X	X	X	510
1	1	1	1	1	1	1	1	1	X	X	X	511

MAIN MEMORY PAGE PROGRAM: This operation is a combination of the Buffer Write and Buffer to Main Memory Page Program with Built-In Erase operations. Data is first shifted into buffer 1 or buffer 2 from the SI pin and then programmed into a specified page in the main memory. An 8-bit opcode, 82H for buffer 1 or 85H for buffer 2, is followed by the two reserved bits and 22 address bits. The 12 most significant address bits (PA11-PA0) select the page in the main memory where data is to be written, and the next 10 address bits (BFA9-BFA0) select the first byte in the buffer to be written. After all address bits are shifted in, the part will take data from the SI pin and store it in one of the data buffers. If the end of the buffer is reached, the device will wrap around back to the beginning of the buffer. When there is a low to high transition on the $\overline{CS}$ pin, the part will first erase the selected page in main memory to all 1s and then program the data stored in the buffer into the specified page in the main memory. Both the erase and the programming of the page are internally self timed and should take place in a maximum of time t_{EP}. During this time, the status register will indicate that the part is busy.

AUTO PAGE REWRITE: This mode is only needed if multiple bytes within a page or multiple pages of data are modified in a random fashion. This mode is a combination of two operations: Main Memory Page to Buffer Transfer and Buffer to Main Memory Page Program with Built-In Erase. A page of data is first transferred from the main memory to buffer 1 or buffer 2, and then the same data (from buffer 1 or buffer 2) is programmed back into its original page of main memory. An 8-bit opcode, 58H for buffer 1 or 59H for buffer 2, is followed by the two reserved bits, 12 address bits (PA11-PA0) that specify the page in main memory to be rewritten, and 10 additional don't care bits. When a low to high transition occurs on the $\overline{CS}$ pin, the part will first transfer data from the page in main memory to a buffer and then program the data from the buffer back into same page of main memory. The operation is internally self-timed and should take place in a maximum time of t_{EP}. During this time, the status register will indicate that the part is busy.

If a sector is programmed or reprogrammed sequentially page by page, then the programming algorithm shown in Figure 1 is recommended. Otherwise, if multiple bytes in a page or several pages are programmed randomly in a sector, then the programming algorithm shown in Figure 2 is recommended.

STATUS REGISTER: The status register can be used to determine the device's ready/busy status, the result of a Main Memory Page to Buffer Compare operation, or the device density. To read the status register, an opcode of 57H must be loaded into the device. After the last bit of the opcode is shifted in, the eight bits of the status register, starting with the MSB (bit 7), will be shifted out on the SO pin during the next eight clock cycles. The five most-significant bits of the status register will contain device information, while the remaining three least-significant bits are reserved for future use and will have undefined values. After bit 0 of the status register has been shifted out, the sequence will repeat itself (as long as $\overline{CS}$ remains low and SCK is being toggled) starting again with bit 7. The data in the status register is constantly updated, so each repeating sequence will output new data.

Ready/busy status is indicated using bit 7 of the status register. If bit 7 is a 1, then the device is not busy and is ready to accept the next command. If bit 7 is a 0, then the device is in a busy state. The user can continuously poll bit 7 of the status register by stopping SCK once bit 7 has been output. The status of bit 7 will continue to be output on the SO pin, and once the device is no longer busy, the state of SO will change from 0 to 1. There are eight operations which can

cause the device to be in a busy state: Main Memory Page to Buffer Transfer, Main Memory Page to Buffer Compare, Buffer to Main Memory Page Program with Built-In Erase, Buffer to Main Memory Page Program without Built-In Erase, Page Erase, Block Erase, Main Memory Page Program, and Auto Page Rewrite.

The result of the most recent Main Memory Page to Buffer Compare operation is indicated using bit 6 of the status register. If bit 6 is a 0, then the data in the main memory page matches the data in the buffer. If bit 6 is a 1, then at least one bit of the data in the main memory page does not match the data in the buffer.

The device density is indicated using bits 5, 4, and 3 of the status register. For the AT45D161, the three bits are 1, 0, and 1. The decimal value of these three binary bits does not equate to the device density; the three bits represent a combinational code relating to differing densities of Serial DataFlash devices, allowing a total of eight different density configurations.

Read/Program Mode Summary

The modes listed above can be separated into two groups — modes which make use of the flash memory array (Group A) and modes which do not make use of the flash memory array (Group B).

Group A modes consist of:

1. Main Memory Page Read
2. Main Memory Page to Buffer 1 (or 2) Transfer
3. Main Memory Page to Buffer 1 (or 2) Compare
4. Buffer 1 (or 2) to Main Memory Page Program With Built-In Erase
5. Buffer 1 (or 2) to Main Memory Page Program Without Built-In Erase
6. Page Erase
7. Block Erase
8. Main Memory Page Program
9. Auto Page Rewrite

Group B modes consist of:

1. Buffer 1 (or 2) Read
2. Buffer 1 (or 2) Write
3. Status Register Read

If a Group A mode is in progress (not fully completed) then another mode in Group A should not be started. However, during this time in which a Group A mode is in progress, modes in Group B can be started.

Status Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RDY/$\overline{\text{BUSY}}$	COMP	1	0	1	X	X	X

This gives the Serial DataFlash the ability to virtually accommodate a continuous data stream. While data is being programmed into main memory from buffer 1, data can be loaded into buffer 2 (or vice versa). See application note AN-4 ("Using Atmel's Serial DataFlash") for more details.

HARDWARE PAGE WRITE PROTECT: If the $\overline{\text{WP}}$ pin is held low, the first 256 pages of the main memory cannot be reprogrammed. The only way to reprogram the first 256 pages is to first drive the protect pin high and then use the program commands previously mentioned. The $\overline{\text{WP}}$ pin is internally pulled high; therefore, connection of the $\overline{\text{WP}}$ pin is not necessary if this pin and feature will not be utilized. However, it is recommended that the $\overline{\text{WP}}$ pin be driven high externally whenever possible.

$\overline{\text{RESET}}$: A low state on the reset pin ($\overline{\text{RESET}}$) will terminate the operation in progress and reset the internal state machine to an idle state. The device will remain in the reset condition as long as a low level is present on the $\overline{\text{RESET}}$ pin. Normal operation can resume once the $\overline{\text{RESET}}$ pin is brought back to a high level.

The device incorporates an internal power-on reset circuit, so there are no restrictions on the $\overline{\text{RESET}}$ pin during power-on sequences. The $\overline{\text{RESET}}$ pin is also internally pulled high; therefore, connection of the $\overline{\text{RESET}}$ pin is not necessary if this pin and feature will not be utilized. However, it is recommended that the $\overline{\text{RESET}}$ pin be driven high externally whenever possible.

READY/$\overline{\text{BUSY}}$: This open drain output pin will be driven low when the device is busy in an internally self-timed operation. This pin, which is normally in a high state (through an external pull-up resistor), will be pulled low during programming operations, compare operations, and during page-to-buffer transfers.

The busy status indicates that the Flash memory array and one of the buffers cannot be accessed; read and write operations to the other buffer can still be performed.

Power On/Reset State

When power is first applied to the device, or when recovering from a reset condition, the device will default to SPI mode 3. In addition, the SO pin will be in a high impedance state, and a high to low transition on the $\overline{\text{CS}}$ pin will be required to start a valid instruction. The SPI mode will be automatically selected on every falling edge of $\overline{\text{CS}}$ by sampling the inactive clock state.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC and AC Operating Range

		AT45D161
Operating Temperature (Case)	Com.	0°C to 70°C
	Ind.	-40°C to 85°C
V_{CC} Power Supply[1]		4.5V to 5.5V

Notes: 1. After power is applied and V_{CC} is at the minimum specified data sheet value, the system should wait 20 ms before an operational mode is started.

4

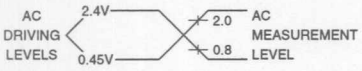
DC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{SB}	Standby Current	$\overline{CS}$, $\overline{RESET}$, $\overline{WP}$ = V_{IH}, all inputs at CMOS levels		10	20	µA
I_{CC1}	Active Current, Read Operation	f = 15 MHz; I_{OUT} = 0 mA; V_{CC} = 5.5V		15	25	mA
I_{CC2}	Active Current, Program/Erase Operation	V_{CC} = 5.5V		25	50	mA
I_{LI}	Input Load Current	V_{IN} = CMOS levels			10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = CMOS levels			10	µA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage		2.0			V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			0.45	V
V_{OH1}	Output High Voltage	I_{OH} = -400 µA	2.4			V
V_{OH2}	Output High Voltage	I_{OH} = -100 µA; V_{CC} = 4.5V	4.2			V

AC Characteristics

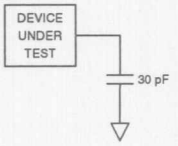
Symbol	Parameter	Min	Typ	Max	Units
f_{SCK}	SCK Frequency			15	MHz
t_{WH}	SCK High Time	30			ns
t_{WL}	SCK Low Time	30			ns
t_{CS}	Minimum $\overline{CS}$ High Time	250			ns
t_{CSS}	$\overline{CS}$ Setup Time	250			ns
t_{CSH}	$\overline{CS}$ Hold Time	250			ns
t_{CSB}	$\overline{CS}$ High to RDY/$\overline{BUSY}$ Low			200	ns
t_{SU}	Data In Setup Time	10			ns
t_H	Data In Hold Time	15			ns
t_{HO}	Output Hold Time	0			ns
t_{DIS}	Output Disable Time			20	ns
t_V	Output Valid			25	ns
t_{XFR}	Page to Buffer Transfer/Compare Time		250	350	µs
t_{EP}	Page Erase and Programming Time		10	20	ms
t_P	Page Programming Time		7	15	ms
t_{PE}	Page Erase Time		6	10	ms
t_{BE}	Block Erase Time		7	15	ms
t_{RST}	$\overline{RESET}$ Pulse Width	10			µs
t_{REC}	$\overline{RESET}$ Recovery Time			1	µs

Input Test Waveforms and Measurement Levels



t_R, t_F < 5 ns (10% to 90%)

Output Test Load

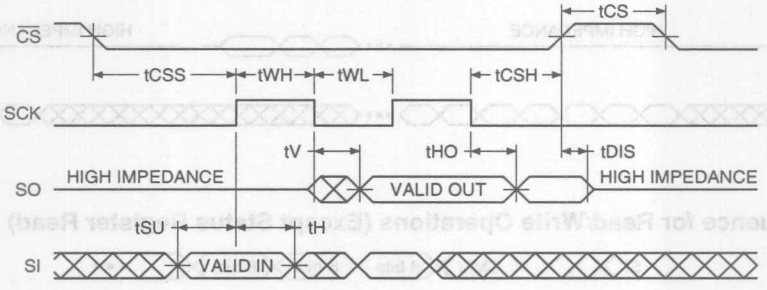


AC Waveforms

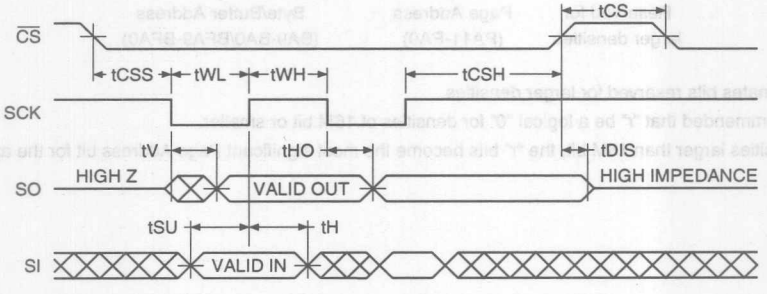
Two different timing diagrams are shown below. Waveform 1 shows the SCK signal being low when $\overline{CS}$ makes a high-to-low transition, and Waveform 2 shows the SCK signal being high when $\overline{CS}$ makes a high-to-low transition. Both waveforms show valid timing diagrams. The setup and hold times for the SI signal are referenced to the low-to-high transition on the SCK signal.

Waveform 1 shows timing that is also compatible with SPI Mode 0, and Waveform 2 shows timing that is compatible with SPI Mode 3.

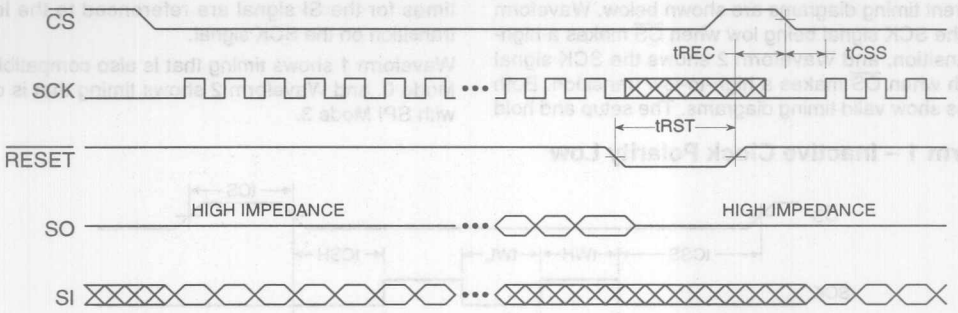
Waveform 1 – Inactive Clock Polarity Low



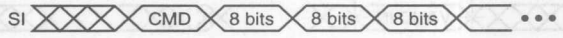
Waveform 2 – Inactive Clock Polarity High

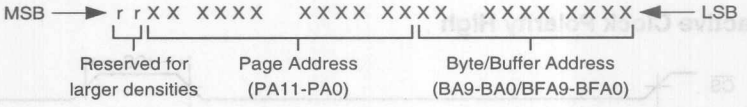


Reset Timing (Inactive Clock Polarity Low Shown)



Command Sequence for Read/Write Operations (Except Status Register Read)

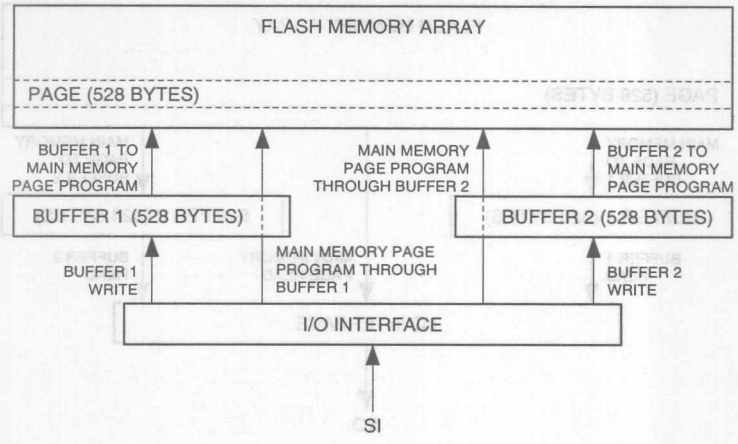




Notes: 1. "r" designates bits reserved for larger densities.
2. It is recommended that "r" be a logical "0" for densities of 16M bit or smaller.
3. For densities larger than 16M bit, the "r" bits become the most significant Page Address bit for the appropriate density.

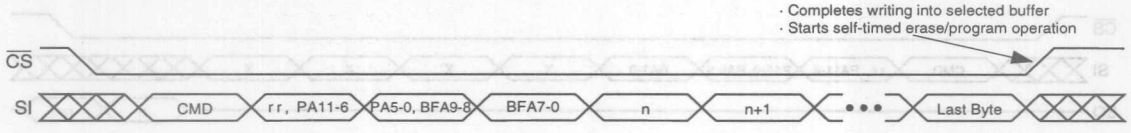
Write Operations

The following block diagram and waveforms illustrate the various write sequences available.

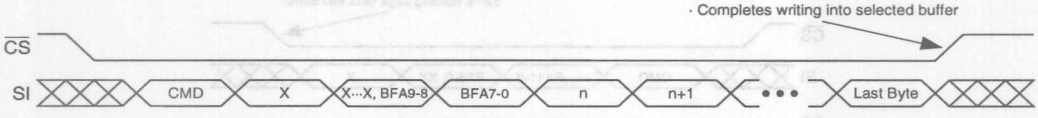


4

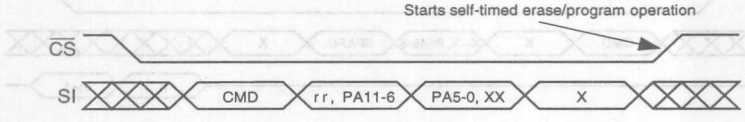
Main Memory Page Program through Buffers



Buffer Write



Buffer to Main Memory Page Program (Data from Buffer Programmed into Flash Page)

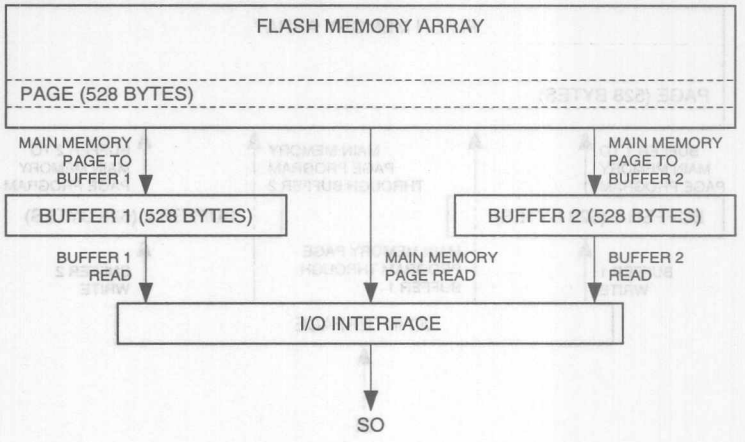


Each transition represents 8 bits and 8 clock cycles

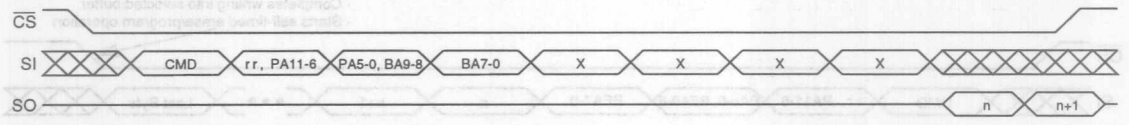
n = 1st byte read
n+1 = 2nd byte read

Read Operations

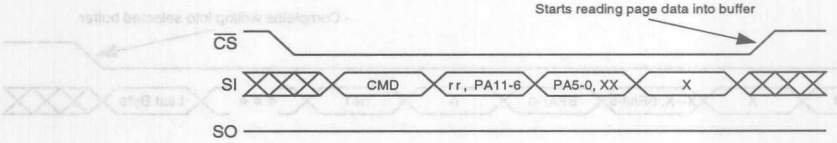
The following block diagram and waveforms illustrate the various read sequences available.



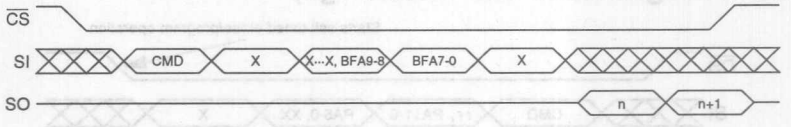
Main Memory Page Read



Main Memory Page to Buffer Transfer (Data from Flash Page Read into Buffer)



Buffer Read

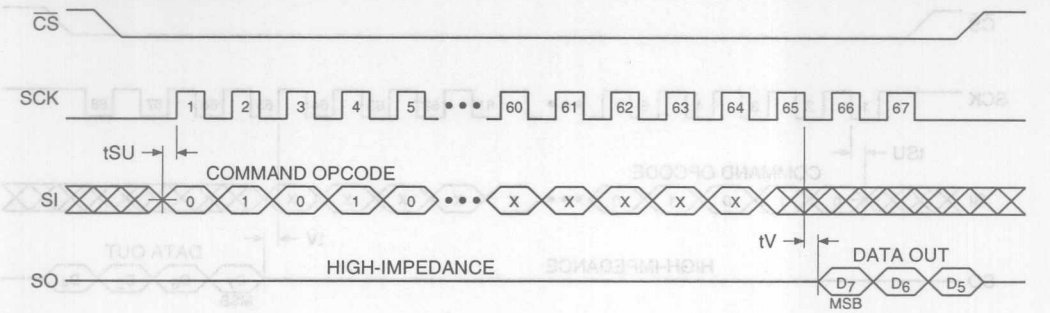


Each transition represents 8 bits and 8 clock cycles

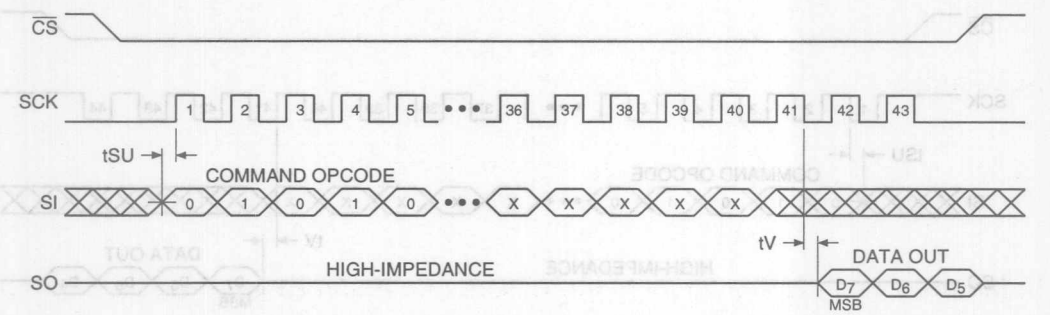
n = 1st byte written
n+1 = 2nd byte written

Detailed Bit-Level Read Timing – Inactive Clock Polarity Low

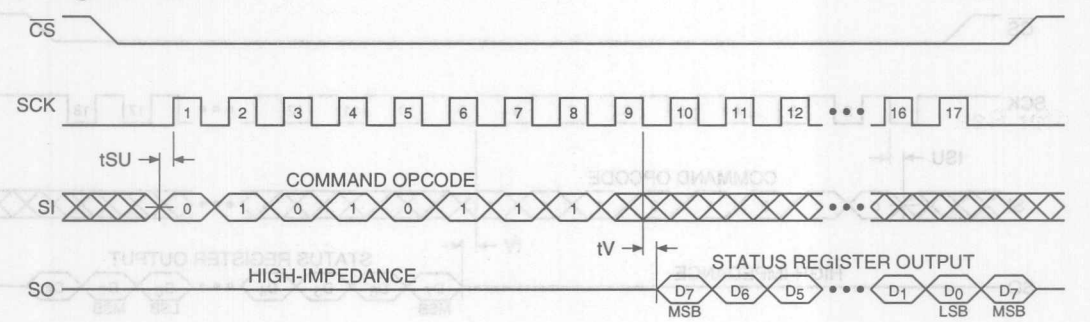
Main Memory Page Read



Buffer Read

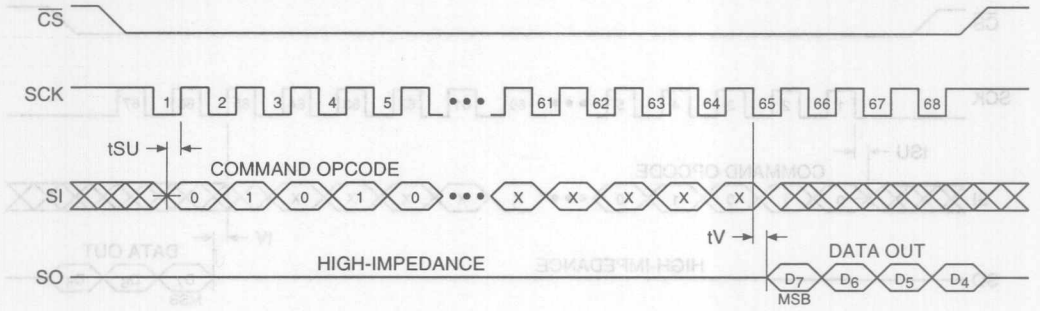


Status Register Read

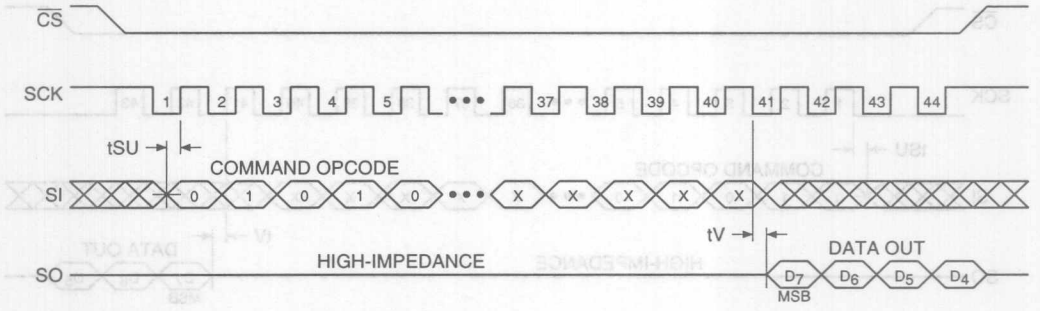


Detailed Bit-Level Read Timing – Inactive Clock Polarity High

Main Memory Page Read



Buffer Read



Status Register Read

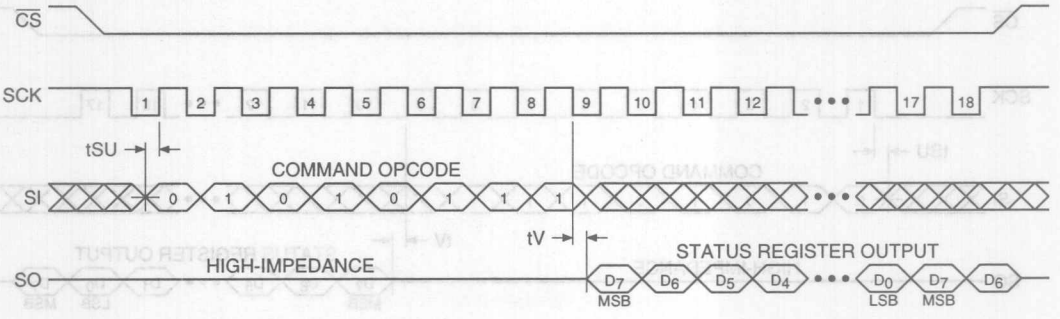


Table 1.

Main Memory Page Read	Buffer 1 Read	Buffer 2 Read	Main Memory Page to Buffer 1 Transfer	Main Memory Page to Buffer 2 Transfer	Main Memory Page to Buffer 1 Compare	Main Memory Page to Buffer 2 Compare	Buffer 1 Write	Buffer 2 Write
Opcode								
52H	54H	56H	53H	55H	60H	61H	84H	87H
0	0	0	0	0	0	0	1	1
1	1	1	1	1	1	1	0	0
0	0	0	0	0	1	1	0	0
1	1	1	1	1	0	0	0	0
0	0	0	0	0	0	0	0	0
0	1	1	0	1	0	0	1	1
1	0	1	1	0	0	0	0	1
0	0	0	1	1	0	1	0	1
r	X	X	r	r	r	r	X	X
r	X	X	r	r	r	r	X	X
PA11	X	X	PA11	PA11	PA11	PA11	X	X
PA10	X	X	PA10	PA10	PA10	PA10	X	X
PA9	X	X	PA9	PA9	PA9	PA9	X	X
PA8	X	X	PA8	PA8	PA8	PA8	X	X
PA7	X	X	PA7	PA7	PA7	PA7	X	X
PA6	X	X	PA6	PA6	PA6	PA6	X	X
PA5	X	X	PA5	PA5	PA5	PA5	X	X
PA4	X	X	PA4	PA4	PA4	PA4	X	X
PA3	X	X	PA3	PA3	PA3	PA3	X	X
PA2	X	X	PA2	PA2	PA2	PA2	X	X
PA1	X	X	PA1	PA1	PA1	PA1	X	X
PA0	X	X	PA0	PA0	PA0	PA0	X	X
BA9	BFA9	BFA9	X	X	X	X	BFA9	BFA9
BA8	BFA8	BFA8	X	X	X	X	BFA8	BFA8
BA7	BFA7	BFA7	X	X	X	X	BFA7	BFA7
BA6	BFA6	BFA6	X	X	X	X	BFA6	BFA6
BA5	BFA5	BFA5	X	X	X	X	BFA5	BFA5
BA4	BFA4	BFA4	X	X	X	X	BFA4	BFA4
BA3	BFA3	BFA3	X	X	X	X	BFA3	BFA3
BA2	BFA2	BFA2	X	X	X	X	BFA2	BFA2
BA1	BFA1	BFA1	X	X	X	X	BFA1	BFA1
BA0	BFA0	BFA0	X	X	X	X	BFA0	BFA0
X	X	X						
X	X	X						
X	X	X						
X	X	X						
X	X	X						
X	X	X						
X	X	X						
X	X	X						
•								
•								
•								
X (64th bit)								

X (Don't Care)
r (reserved bits)

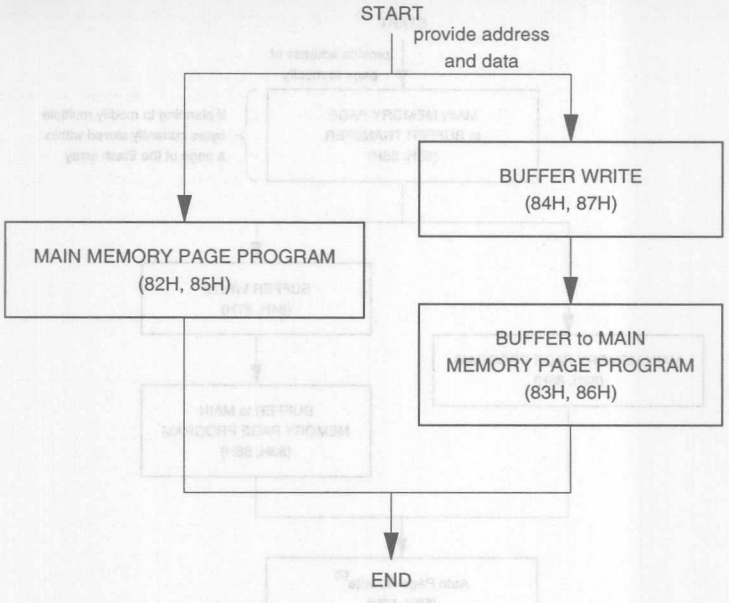
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Table 2.

Buffer 1 to Main Memory Page Program with Built In Erase	Buffer 2 to Main Memory Page Program with Built-In Erase	Buffer 1 to Main Memory Page Program without Built-In Erase	Buffer 2 to Main Memory Page Program without Built-In Erase	Page Erase	Block Erase	Main Memory Page Program Through Buffer 1	Main Memory Page Program Through Buffer 2	Auto Page Rewrite Through Buffer 1	Auto Page Rewrite Through Buffer 2	Status Register
Opcode										
83H	86H	88H	89H	81H	50H	82H	85H	58H	59H	57H
1	1	1	1	1	0	1	1	0	0	0
0	0	0	0	0	1	0	0	1	1	1
0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	1	0	0	1	1	1
0	0	1	1	0	0	0	0	1	1	0
0	1	0	0	0	0	0	1	0	0	1
1	1	0	0	0	0	1	0	0	0	1
1	0	0	1	1	0	0	1	0	1	1
r	r	r	r	r	r	r	r	r	r	
r	r	r	r	r	r	r	r	r	r	
PA11	PA11	PA11	PA11	PA11	PA11	PA11	PA11	PA11	PA11	
PA10	PA10	PA10	PA10	PA10	PA10	PA10	PA10	PA10	PA10	
PA9	PA9	PA9	PA9	PA9	PA9	PA9	PA9	PA9	PA9	
PA8	PA8	PA8	PA8	PA8	PA8	PA8	PA8	PA8	PA8	
PA7	PA7	PA7	PA7	PA7	PA7	PA7	PA7	PA7	PA7	
PA6	PA6	PA6	PA6	PA6	PA6	PA6	PA6	PA6	PA6	
PA5	PA5	PA5	PA5	PA5	PA5	PA5	PA5	PA5	PA5	
PA4	PA4	PA4	PA4	PA4	PA4	PA4	PA4	PA4	PA4	
PA3	PA3	PA3	PA3	PA3	PA3	PA3	PA3	PA3	PA3	
PA2	PA2	PA2	PA2	PA2	X	PA2	PA2	PA2	PA2	
PA1	PA1	PA1	PA1	PA1	X	PA1	PA1	PA1	PA1	
PA0	PA0	PA0	PA0	PA0	X	PA0	PA0	PA0	PA0	
X	X	X	X	X	X	BFA9	BFA9	X	X	
X	X	X	X	X	X	BFA8	BFA8	X	X	
X	X	X	X	X	X	BFA7	BFA7	X	X	
X	X	X	X	X	X	BFA6	BFA6	X	X	
X	X	X	X	X	X	BFA5	BFA5	X	X	
X	X	X	X	X	X	BFA4	BFA4	X	X	
X	X	X	X	X	X	BFA3	BFA3	X	X	
X	X	X	X	X	X	BFA2	BFA2	X	X	
X	X	X	X	X	X	BFA1	BFA1	X	X	
X	X	X	X	X	X	BFA0	BFA0	X	X	

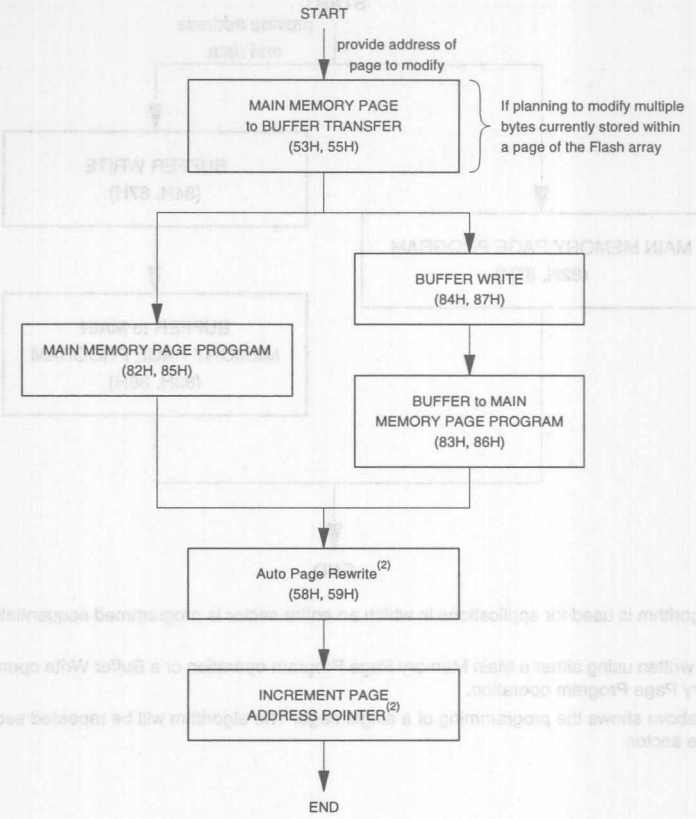
X (Don't Care)
r (reserved bits)

Figure 1. Algorithm for Programming or Reprogramming of an Entire Sector Sequentially



Notes:
1. This type of algorithm is used for applications in which an entire sector is programmed sequentially, filling the sector page-by-page.
2. A page can be written using either a Main Memory Page Program operation or a Buffer Write operation followed by a Buffer to Main Memory Page Program operation.
3. The algorithm above shows the programming of a single page. The algorithm will be repeated sequentially for each page within the entire sector.

Figure 2. Algorithm for Randomly Modifying Data



Notes:
1. To preserve data integrity, each page of a DataFlash sector (256 pages per sector) must be updated/rewritten at least once within every 10,000 cumulative page erase/program operations within that sector.
2. A Page Address Pointer must be maintained to indicate which page is to be rewritten. The Auto Page Rewrite command must use the address specified by the Page Address Pointer.
3. Other algorithms can be used to rewrite portions of the Flash array. Low power applications may choose to wait until 10,000 cumulative page erase/program operations have accumulated before rewriting all 256 pages of the sector. See application note AN-4 ("Using Atmel's Serial DataFlash") for more details.

Sector Addressing

PA11	PA10	PA9	PA8	Sector
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

Ordering Information

f_{SCK} (MHz)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
15	25	0.02	AT45D161-JC AT45D161-RC AT45D161-TC	32J 28R 28T	Commercial (0°C to 70°C)
15	25	0.02	AT45D161-JI AT45D161-RI AT45D161-TI	32J 28R 28T	Industrial (-40°C to 85°C)

Package Type	
32J	32-Lead, Plastic J-Leaded Chip Carrier (PLCC)
28R	28-Lead, 0.330" Wide, Plastic Gull Wing Small Outline (SOIC)
28T	28-Lead, Plastic Thin Small Outline Package (TSOP)

Ordering Information

f_{SCK} (MHz)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
15	25	0.02	AT45D161-JC AT45D161-RC AT45D161-TC	32J 28R 28T	Commercial (0°C to 70°C)
15	25	0.02	AT45D161-JI AT45D161-RI AT45D161-TI	32J 28R 28T	Industrial (-40°C to 85°C)

	Package Type
32J	32-Lead, Plastic J-Leaded Chip Carrier (PLCC)
28R	28-Lead, 0.330" Wide, Plastic Gull Wing Small Outline (SOIC)
28T	28-Lead, Plastic Thin Small Outline Package (TSOP)

Using Atmel's Serial DataFlash®

Introduction

In the past, engineers have struggled to use Flash memory for data storage applications. The traditional Flash memory devices, with their large page sizes of 4K to 128K bytes, make it difficult to change a few bytes. Typically, system designers must include external RAM buffers to shadow the Flash memory page's contents to make the data modifications.

Atmel's Serial DataFlash is a new Flash family designed specifically for data storage applications. Its small page size of 264 bytes for densities of 8M and smaller, provides the system designer with a high level of flexibility and completely simplifies the process of data modifications. Furthermore, the Serial DataFlash incorporates a simple serial interface which facilitates hardware layout, increases system reliability, and minimizes switching noise.

The Serial DataFlash is perfectly suited for digital voice-, image-, and data-storage applications, especially where low power consumption is required. In these storage applications, the Serial DataFlash's small page size not only makes it easier to manipulate data, it also increases storage efficiency. The list below shows some typical applications for the Serial DataFlash.

Digital Voice Storage Applications:

- Digital answering machines
- Voice memo functions in cellular phones
- Voice storage in pagers
- Portable voice memo recorders
- Portable dictation recorders

Image Storage Applications:

- Image storage for digital cameras
- Scanned fax storage for delayed fax sending/receiving

Data Storage Applications:

- "Saved game and high score" data for video game systems
- Phone number and text message storage in pagers
- Data storage in PDAs
- Data acquisition systems

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Rev. 0842B–10/98

Serial DataFlash®

Application Note

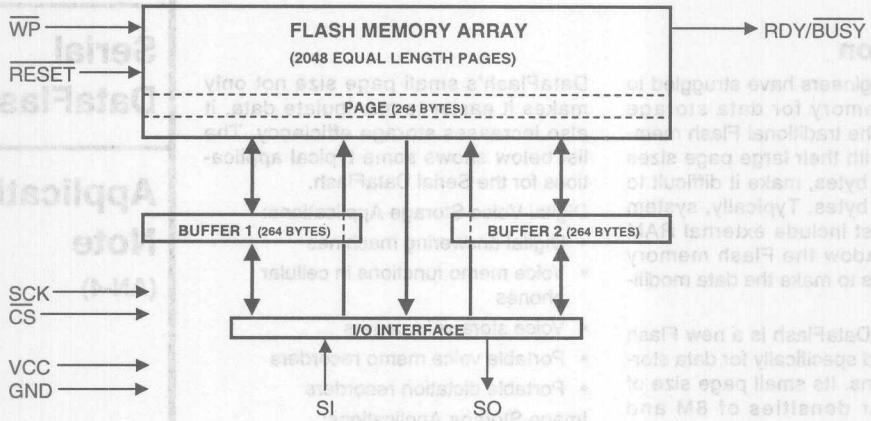
(AN-4)

4

Functional Description

The block diagram of Atmel's Serial DataFlash memory shows that the device consists of a Flash memory array, two data buffers, and a simple I/O interface (Figure 1). Unlike conventional Flash memories that are accessed randomly with multiple address lines and a parallel interface, the Serial DataFlash uses a serial interface to sequentially access its data. The serial interface, used to transfer both address and data information, provides a true upgrade/downgrade path

Figure 1. Atmel's AT45D041 Serial DataFlash consists of a Flash memory array, two buffers, and a simple I/O interface.



Serial DataFlash Array

The Flash memory array of the AT45D041, the first device in the Serial DataFlash family, comprises 2048 equal length pages. The AT45D041's page size is 264 bytes, rather than 256 bytes. Therefore, the total density (4,325,376 bits) of the device is 128K bits larger than 4M bits.

System designers can use all of a page's 264 bytes for storing data. Alternatively, the 8 extra bytes per page can be used for error detection and correction mechanisms (EDC) or associated control information, such as pointers, flags, and phone message routing directions. This information, which is potentially vital to the operation of the system, can be used by the microcontroller or processor to determine how to utilize the data stored within the associated page.

For example, in a digital voice messaging system, the AT45D041 pages store the compressed data of digitized voice messages. A page's control information could contain a mailbox number indicating which user can access the voice message stored within that page. Additionally, the system could set a priority level flag to denote that the message is urgent. If the message spans more than one Flash page, the system can store a pointer to indicate which page contains the next portion of the message. The extra 8 bytes of each AT45D041 page provides an area to store this type of control information, greatly enhancing the capability of the system.

The device also provides the ability to securely store critical, infrequently updated information via the Write Protect pin ($\overline{WP}$). When $\overline{WP}$ is held low, the first 256 pages of the array are protected and cannot be programmed. Infrequently updated information, from the digital voice messaging example described above, could be user identification or parameters such as the permitted message length, a message's retention period, and the number of messages a particular user can have. The protected area could also be used to store information such as voice menu prompts, time/date information, secure data or coefficient look-up tables.

Data Buffers Increase Performance

The AT45D041 incorporates two on-chip, bi-directional buffers to expedite the flow of data to and from the device. These buffers provide a built-in "pseudo" cache memory and allow the AT45D041 device to receive data during erase/program operations. Each buffer is 264 bytes long, the same size as a Flash page, and function independently from each other. The system may also use the data buffers as "scratch pad" memory for reads and writes. Therefore, these on-chip buffers may eliminate the need to use off-

chip RAM or RAM contained within the microcontroller or processor.

The AT45D041's buffers are static RAMs (SRAM) and therefore, data stored within the buffers is not guaranteed if the supply voltage drops below the specified minimum operating level. However, the buffers' static nature eliminates the need for refreshing, and data will not change until new data is loaded into the buffers. When loading new data, only those bytes specified to be overwritten will change; the remaining bytes are unaffected. For example, if the user loads only 200 bytes into a buffer, the remaining 64 bytes will still retain their previous values.

Serial Interface Simplifies Upgradability

The sequential access, serial interface scheme employed through the Serial DataFlash's pinout enables a practically limit-free upgrade path for either density or word-width. Conventional random access, parallel interface Flash must use dedicated address pins to interface to the system microcontroller or processor. As density requirements increase, address lines must be added, in turn increasing the number of pins and the size of the device's package. Likewise, a parallel interface Flash requires dedicated I/O pins, and as word-widths increase to 16 or 32 bits, I/O pins must be added, again impacting the package's size.

The Serial DataFlash interfaces with other devices using only seven signal leads, three of which are dedicated to the serial bus (SCK, SI, and SO). The remaining signal leads on the Serial DataFlash include a chip select ($\overline{CS}$), chip reset input ($\overline{RESET}$), a write protect input ($\overline{WP}$), and a ready/busy output (RDY/$\overline{BUSY}$).

Functional Operation of the SPI

The Serial DataFlash can be used with any type of microcontroller, but the interface of the device is also compatible with SPI modes 0 and 3 to provide simple interconnections with the increasingly popular SPI microcontrollers.

SPI is a serial interface protocol, utilizing 8-bit words, useful in communicating with external devices such as serial EEPROMs and the Serial DataFlash. Prior to the availability of SPI EEPROMs, engineers used the standard Microwire EEPROMs to interface with the SPI port on microcontrollers. While the SPI port on microcontrollers was capable of running at 2.1 MHz, it was limited by the EEPROM's 1 MHz operating rate. It wasn't until recently that EEPROMs, such as Atmel's AT25010/020/040 Serial CMOS EEPROMs, became available with the SPI standard interface. Due to SPI's faster clock speed and interface compatibility, this EEPROM device is increasing in popularity; the same applies to the Serial DataFlash.

Controlling Data Flow

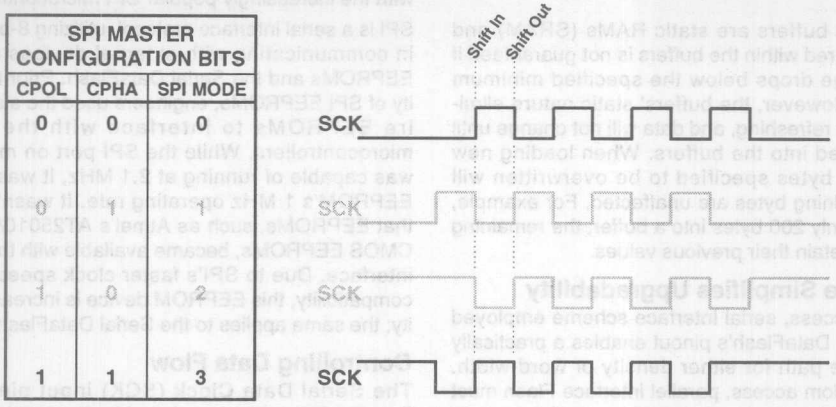
The Serial Data Clock (SCK) input pin of the Serial DataFlash must be generated by the master microcontroller or processor, or in some instances a free-running oscillator. All programming cycles in the Serial DataFlash are completely self-timed, so the SCK signal only controls the clocking of data into and out of the device.

The $\overline{CS}$ pin on the Serial DataFlash functions the same as that of a chip select pin on any memory device. Driving $\overline{CS}$ LOW selects the device; driving $\overline{CS}$ HIGH deselects the device and puts the device into a quiescent state. When $\overline{CS}$ is deselected, the Serial DataFlash ignores any data present on the Serial Data Input (SI) pin, and the Serial Data Output (SO) pin remains in a high-impedance state. The $\overline{CS}$ pin also functions as a trigger to initiate the internal self-timed read and write sequences. The specifics for each sequence and how $\overline{CS}$ relates to them are discussed in the "Read Operations" and "Program Operations" section of the application note.

Table 1. Features of the Serial DataFlash Interface

Maximum Bus Speed	10 MHz
Number of Active Pins	3 or 4
Maximum Memory Size	N/A
Data Size	8 bits
Block Write Capability	Yes
Sequential Read Capability	Yes
Number of Devices on Bus	Limited by Port Pins
Supported SPI Modes	0 and 3

Figure 2. SPI mode determines which edge of the clock signal controls the data transfer direction.



Note: The shifting out of data does not occur on the falling edge of the same clock cycle as data shifting in, but rather the falling edge of the next clock cycle.

SPI Operating Modes

SPI has four operating modes: 0, 1, 2, and 3. The SPI operating mode determines the clock phase and polarity for transmitting or receiving data. In other words, the mode determines which edge of the clock signal controls the direction of data transfer (Figure 2).

The Serial DataFlash only supports the most commonly used SPI modes, 0 and 3. With these modes, the rising edge of the SCK signal always clocks data in, while the falling edge always clocks data out. Supporting only modes 0 and 3 eliminates the need to integrate special mode select registers within the Serial DataFlash. Examining the clock waveforms in Figure 2, observe that the difference between modes 0 and 3 is the level where SCK starts. When the Serial DataFlash sees a rising edge transition on SCK, this is the indication to latch data in. As long as the designer follows these clock signal conventions, any type of microcontroller or processor may be used as the SPI master — *the Serial DataFlash is not limited to interfacing with SPI-compatible devices.*

Interfacing the Serial DataFlash to a Microcontroller

Atmel's AT89S8252 is an MCS-51 compatible microcontroller with a Serial Peripheral Interface. It supports full-duplex, 3-wire synchronous data transfer with a 6 MHz maximum bit frequency. By enabling the AT89S8252's SPI feature, port 1 pins P1.5-P1.7 can be connected to the Serial DataFlash. This microcontroller contains a series of Special Function Registers (SFRs). Among these SFRs is the SPI Control Register located at SFR address D5H (Table 2). Bits CPOL and CPHA control the SPI mode, while bits SPR0 and SPR1 control the data rate (Table 3).

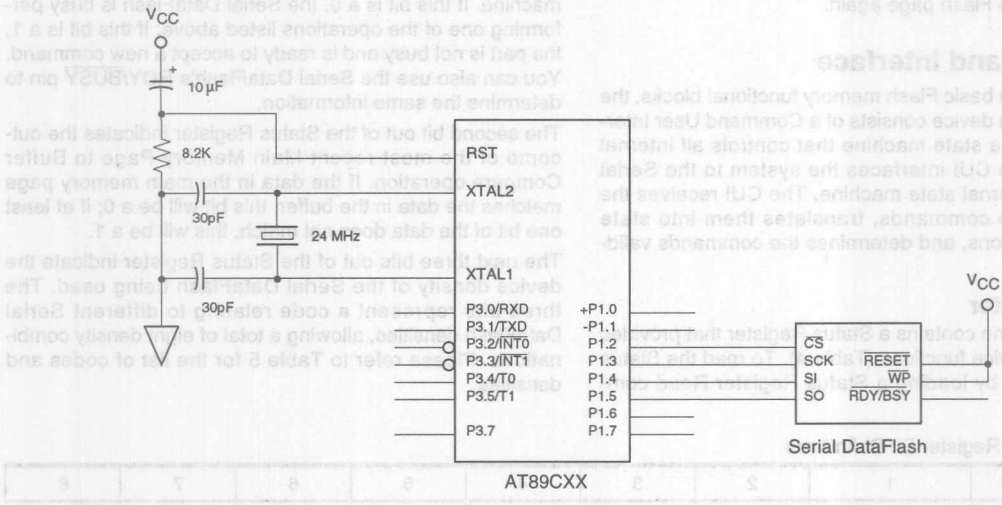
Table 2. SPI Control Register

AT89S8252 Microcontroller, SPI Control Register: SFR Address D5H								
Bit	SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0
	7	6	5	4	3	2	1	0

Table 3. SPI Control Register Bit Definitions

Symbol	Function
SPIE	SPI Interrupt Enable
SPE	SPI Enable: SPI = 1 enables the SPI channel and connects SS, MOSI, and SC to pins P1.4-P1.7 SPI = 0 disables the SPI channel
DORD	Data Order
MSTR	Master/Slave Select
CPOL	Clock Polarity: CPOL = 1, SCK is high when idle CPOL = 0, SCK of the master device is low when not transmitting
CPHA	Clock Phase. The CPHA bit, together with the CPOL bit, controls the clock and data relationship between master and slave
SPR0 SPR1	SPI Clock Rate Select

Figure 3. The Serial DataFlash can be connected to any microcontroller with the ability to provide a clock signal.



Alternatively, any microcontroller with individually controlled port pins can provide the proper serial interface for the Serial DataFlash. As shown in Figure 3, Atmel's AT89CXX can be connected to the Serial DataFlash. The microcontroller can clock data into the Serial DataFlash at rates up to 10 MHz; whereas the limit on a strict SPI implementation is only 2.1 MHz.

The Reset Function

The Serial DataFlash has a reset function that causes any operation currently in progress to be terminated and forces the device's internal state machine into an idle state. The reset function is activated by holding the device's $\overline{\text{RESET}}$ pin LOW. This feature can be used as a safeguard against system power glitches or when the system supply monitor circuitry detects the supply voltage going below the minimum operating limit. Resetting the Serial DataFlash during these operating conditions prevents any erroneous opera-

tions which could result in data corruption (for more information see section on "Write Protection Mechanisms").

If the Serial DataFlash is reset before the completion of a page program/erase operation, then the data in the page being programmed or erased cannot be guaranteed; the Serial DataFlash must finish the entire operation in order for all data in the page to be valid. If the user wants to ensure that a valid program/erase operation has been performed before resetting the device, then the system must either wait the maximum t_{EP} or t_P time, poll the RDY/$\overline{BUSY}$ pin, or poll the status register (see section on "Status Register") to determine the completion of the program/erase operation.

If the system must service a higher level interrupt and must reset the Serial DataFlash before the completion of the program/erase operation, then the system can later program the Flash page again with the same data. Resetting the device will not alter the contents of the internal RAM buffers, so the buffer used to perform the initial program/erase operation before the device was reset will still retain the same data. Therefore, a simple Buffer to Main Memory Page Program with Built-In Erase command can be issued to reprogram the Flash page again.

The Command Interface

In addition to the basic Flash memory functional blocks, the Serial DataFlash device consists of a Command User Interface (CUI) and a state machine that controls all internal operations. The CUI interfaces the system to the Serial DataFlash's internal state machine. The CUI receives the user's software commands, translates them into state machine operations, and determines the commands validity.

Status Register

The state machine contains a Status Register that provides feedback on device functions (Table 4). To read the Status Register, begin by loading a Status Register Read command (opcode 57H) into the Serial DataFlash. Next, read eight bits of data from the SO pin. It is not possible to write data into the Status Register, so data will be output after the last bit of the opcode is clocked into the device.

The first bit to be output from the Status Register will be bit 7, the most-significant bit (MSB). Valid data will continue being output through bit 3, while bits 2, 1, and 0 will have unknown values since they are reserved for future use. After bit 0 of the Status Register has been output, the sequence will repeat itself (as long as $\overline{CS}$ remains LOW) starting again with bit 7. The data in the Status Register is always being updated, so each repeating sequence will contain new data.

You can use the Status Register to determine if the Serial DataFlash is busy or not. The part will be busy during a Main Memory Page to Buffer Transfer, Main Memory Page to Buffer Compare, Buffer to Main Memory Page Program with Built-In Erase, Buffer to Main Memory Page Program without Built-In Erase, Main Memory Page Program, or an Auto Page Rewrite operation. The first bit (MSB) out of the Status Register indicates the ready/busy status, which is derived from the operational status of the internal state machine. If this bit is a 0, the Serial DataFlash is busy performing one of the operations listed above; if this bit is a 1, the part is not busy and is ready to accept a new command. You can also use the Serial DataFlash's RDY/$\overline{BUSY}$ pin to determine the same information.

The second bit out of the Status Register indicates the outcome of the most recent Main Memory Page to Buffer Compare operation. If the data in the main memory page matches the data in the buffer, this bit will be a 0; if at least one bit of the data does not match, this will be a 1.

The next three bits out of the Status Register indicate the device density of the Serial DataFlash being used. The three bits represent a code relating to different Serial DataFlash densities, allowing a total of eight density combinations. Please refer to Table 5 for the list of codes and densities.

Table 4. Status Register Bit Definitions

Order shifted out	1	2	3	4	5	6	7	8
Status Register Bit	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
	RDY/$\overline{BUSY}$	Compare	Density Code			Reserved for future use		

Table 5. Status Register Density Codes

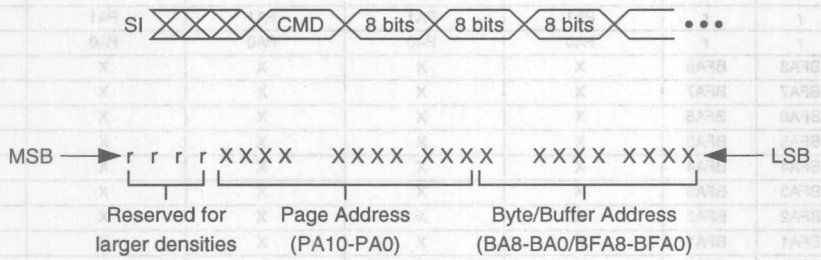
BIT 5	BIT 4	BIT 3	DEVICE DENSITY
0	0	0	512K
0	0	1	1M
0	1	0	2M
0	1	1	4M
1	0	0	8M
1	0	1	16M
1	1	0	32M
1	1	1	64M

Command Table

To begin an operation on the Serial DataFlash, the system must send a command to the device. Table 6 shows the bit sequence to follow for each Serial DataFlash operation. All operations (except for Status Register Read) start with an opcode followed by three address bytes that are clocked into the Serial DataFlash.

The three address bytes (24 bits) are used to address the memory array or buffers for the AT45D041. As shown in Figure 4, the four MSB bits are *Reserved* bits; bits 5-15 denote a page number; bits 16-24 denote a specific byte address within the 264-byte page or buffer. This 24-bit addressing scheme allows the system to address up to 64M bytes. The four *Reserved* bits of the AT45D041 will be address bits for larger density devices and should be zero to ensure upwards compatibility.

Figure 4. Command Sequence for AT45D041 Read/Write Operations (Except Status Register Read).



Notes: 1. "r" designates bits reserved for larger densities.
2. It is recommended that "r" be a logical "0" for densities of 4M bit or smaller.
3. For densities larger than 4M bit, the "r" bits become the most significant Page Address bit for the appropriate density.

Table 6.

Main Memory Page Read	Buffer 1 Read	Buffer 2 Read	Main Memory Page to Buffer 1 Transfer	Main Memory Page to Buffer 2 Transfer	Main Memory Page to Buffer 1 Compare	Main Memory Page to Buffer 2 Compare	Buffer 1 Write	Buffer 2 Write
Opcode								
52H	54H	56H	53H	55H	60H	61H	84H	87H
0	0	0	0	0	0	0	1	1
1	1	1	1	1	1	1	0	0
0	0	0	0	0	1	1	0	0
1	1	1	1	1	0	0	0	0
0	0	0	0	0	0	0	0	0
0	1	1	0	1	0	0	1	1
1	0	1	1	0	0	0	0	1
0	0	0	1	1	0	1	0	1
r	r	r	r	r	r	r	r	r
r	r	r	r	r	r	r	r	r
r	r	r	r	r	r	r	r	r
r	r	r	r	r	r	r	r	r
PA10	r	r	PA10	PA10	PA10	PA10	r	r
PA9	r	r	PA9	PA9	PA9	PA9	r	r
PA8	r	r	PA8	PA8	PA8	PA8	r	r
PA7	r	r	PA7	PA7	PA7	PA7	r	r
PA6	r	r	PA6	PA6	PA6	PA6	r	r
PA5	r	r	PA5	PA5	PA5	PA5	r	r
PA4	r	r	PA4	PA4	PA4	PA4	r	r
PA3	r	r	PA3	PA3	PA3	PA3	r	r
PA2	r	r	PA2	PA2	PA2	PA2	r	r
PA1	r	r	PA1	PA1	PA1	PA1	r	r
PA0	r	r	PA0	PA0	PA0	PA0	r	r
BA8	BFA8	BFA8	X	X	X	X	BFA8	BFA8
BA7	BFA7	BFA7	X	X	X	X	BFA7	BFA7
BA6	BFA6	BFA6	X	X	X	X	BFA6	BFA6
BA5	BFA5	BFA5	X	X	X	X	BFA5	BFA5
BA4	BFA4	BFA4	X	X	X	X	BFA4	BFA4
BA3	BFA3	BFA3	X	X	X	X	BFA3	BFA3
BA2	BFA2	BFA2	X	X	X	X	BFA2	BFA2
BA1	BFA1	BFA1	X	X	X	X	BFA1	BFA1
BA0	BFA0	BFA0	X	X	X	X	BFA0	BFA0
X	X	X						
X	X	X						
X	X	X						
X	X	X						
X	X	X						
X	X	X						
X	X	X						
X	X	X						
•								
•								
•								
X (64th bit)								

X (Don't Care)

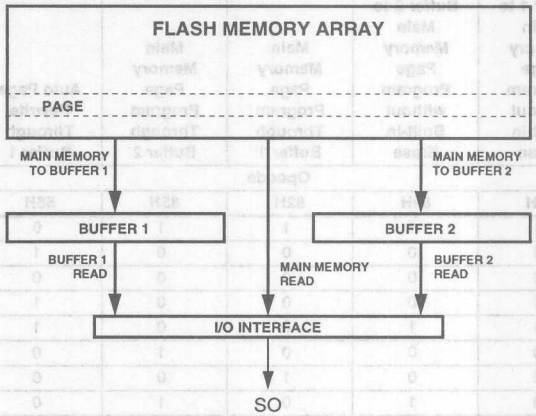
r (reserved bits)

Table 7.

Buffer 1 to Main Memory Page Program with Built-In Erase	Buffer 2 to Main Memory Page Program with Built-In Erase	Buffer 1 to Main Memory Page Program without Built-In Erase	Buffer 2 to Main Memory Page Program without Built-In Erase	Main Memory Page Program Through Buffer 1	Main Memory Page Program Through Buffer 2	Auto Page Rewrite Through Buffer 1	Auto Page Rewrite Through Buffer 2	Status Register
Opcode								
83H	86H	88H	89H	82H	85H	58H	59H	57H
1	1	1	1	1	1	0	0	0
0	0	0	0	0	0	1	1	1
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1	1
0	0	1	1	0	0	1	1	0
0	1	0	0	0	1	0	0	1
1	1	0	0	1	0	0	0	1
1	0	0	1	0	1	0	1	1
r	r	r	r	r	r	r	r	
r	r	r	r	r	r	r	r	
r	r	r	r	r	r	r	r	
r	r	r	r	r	r	r	r	
PA10	PA10	PA10	PA10	PA10	PA10	PA10	PA10	
PA9	PA9	PA9	PA9	PA9	PA9	PA9	PA9	
PA8	PA8	PA8	PA8	PA8	PA8	PA8	PA8	
PA7	PA7	PA7	PA7	PA7	PA7	PA7	PA7	
PA6	PA6	PA6	PA6	PA6	PA6	PA6	PA6	
PA5	PA5	PA5	PA5	PA5	PA5	PA5	PA5	
PA4	PA4	PA4	PA4	PA4	PA4	PA4	PA4	
PA3	PA3	PA3	PA3	PA3	PA3	PA3	PA3	
PA2	PA2	PA2	PA2	PA2	PA2	PA2	PA2	
PA1	PA1	PA1	PA1	PA1	PA1	PA1	PA1	
PA0	PA0	PA0	PA0	PA0	PA0	PA0	PA0	
X	X	X	X	BA8	BA8	X	X	
X	X	X	X	BA7	BA7	X	X	
X	X	X	X	BA6	BA6	X	X	
X	X	X	X	BA5	BA5	X	X	
X	X	X	X	BA4	BA4	X	X	
X	X	X	X	BA3	BA3	X	X	
X	X	X	X	BA2	BA2	X	X	
X	X	X	X	BA1	BA1	X	X	
X	X	X	X	BA0	BA0	X	X	

X (Don't Care)
r (reserved bits)

Figure 5. Data can be read directly from main memory or though the buffers.



Read Operations for the AT45D041

By specifying the appropriate opcode, data can be read from the main memory or from either one of the two buffers (Figure 5).

Main Memory Page Read

A main memory read allows the user to read data directly from any one of the 2048 pages, bypassing both of the data buffers and leaving the buffer contents unchanged. To start a page read, the Main Memory Page Read command (52H) is clocked into the device, followed by four *Reserved* bits, 20 address bits, and 32 don't care bits. The four *Reserved* bits will be address bits used for future expansion and should be zero to ensure upwards compatibility. The 32 don't care bits are sent to give the Serial DataFlash's state machine time to initialize.

When data is read from the main memory, you must specify the page address and the address of the first byte to be read within the page. Specifying the page address requires 11 bits. Specifying the first byte to be read within the page requires nine bits. While reading data from main memory, if the end of the page is reached, the Serial DataFlash will wrap around back to the beginning of the page.

After a high to low transition occurs on the $\overline{CS}$ pin, toggling the SCK pin loads the eight opcode bits, four *Reserved* bits, 20 address bits, and 32 don't care bits from the SI pin; at this point data can be read serially from the SO pin. The $\overline{CS}$ pin must remain low during this entire sequence; a low to high transition of the $\overline{CS}$ pin will terminate the read operation and tri-state the SO pin.

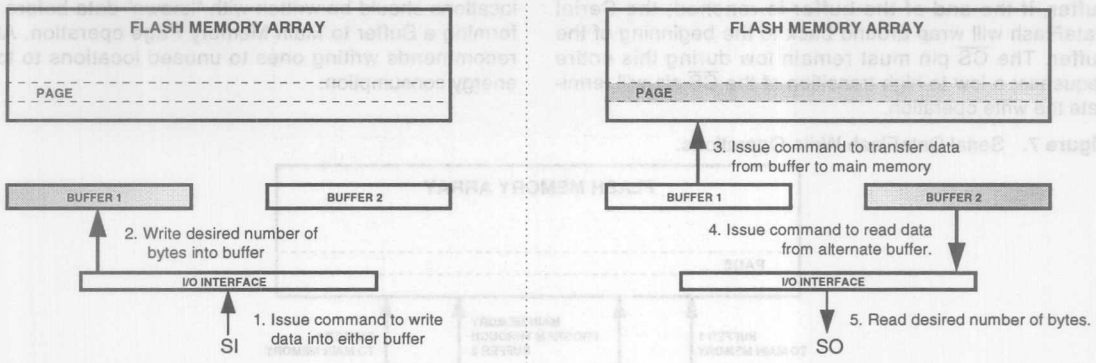
Buffer Read

A buffer read allows the user to read data directly from either of the two buffers. To start a buffer read, a Buffer Read command (54H for buffer 1, 56H for buffer 2) is clocked into the device, followed by 15 *Reserved* bits, nine address bits, and eight don't care bits. The 15 *Reserved* bits may be used for future expansion and should be zero to ensure upwards compatibility. Nine address bits are required to specify the first byte of data to be read from the 264-byte buffer. The eight don't care bits are sent to give the Serial DataFlash's state machine time to initialize. While reading data from a buffer, if the end of the buffer is reached, the Serial DataFlash will wrap around back to the beginning of the buffer.

After a high to low transition occurs on the $\overline{CS}$ pin, toggling the SCK pin loads the eight opcode bits, 15 *Reserved* bits, nine address bits, and eight don't care bits from the SI pin; at this point data can be read serially from the SO pin. The $\overline{CS}$ pin must remain low during this entire sequence; a low to high transition of the $\overline{CS}$ pin will terminate the read operation, and tri-state the SO pin.

NOTE: You can read from one buffer while the Serial DataFlash's state machine is transferring data from the other buffer into main memory (Figure 6).

Figure 6. Serial DataFlash supports virtual read-while-write operations.



4

Main Memory Page to Buffer Transfer

The Serial DataFlash's state machine can automatically transfer data in a main memory page to either buffer 1 or buffer 2. This allows the user to modify one or more bytes of data in a main memory page and then write the modified buffer contents back into main memory.

To start a data transfer, a Main Memory Page to Buffer Transfer command (53H for buffer 1, 55H for buffer 2) is followed by four *Reserved* bits, 11 address bits, and nine don't care bits. The four *Reserved* bits may be used for future expansion and should be zero to ensure upwards compatibility. 11 address bits are required to specify the page in main memory that is to be transferred to the selected buffer.

After a high to low transition occurs on the $\overline{CS}$ pin, toggling the SCK pin loads the eight opcode bits, four *Reserved* bits, 11 address bits, and nine don't care bits from the SI pin. The data transfer begins when there is a low to high transition on the $\overline{CS}$ pin. You can use the RDY/$\overline{BUSY}$ pin or the RDY/$\overline{BUSY}$ bit in the Status Register to determine whether the state machine has completed the transfer. Refer to the section on the Status Register for details on how to access and interpret the Status Register.

Main Memory Page to Buffer Compare

The Serial DataFlash's internal state machine can be used to automatically compare the data in a main memory page to the data in either buffer 1 or buffer 2. This operation is useful after performing a Buffer to Main Memory Page Program or a Main Memory Page Program Command, for verifying that the Serial DataFlash successfully programmed the buffer contents into a main memory page.

To start the compare operation, a Main Memory Page to Buffer Compare command (60H for buffer 1, 61H for buffer 2) is followed by four *Reserved* bits, 11 address bits, and nine don't care bits. The four *Reserved* bits may be used for future expansion and should be zero to ensure upwards compatibility. 11 address bits are required to specify the page in main memory that is to be compared with the selected buffer.

After a high to low transition occurs on the $\overline{CS}$ pin, toggling the SCK pin loads the eight opcode bits, four *Reserved* bits, 11 address bits, and nine don't care bits from the SI pin. The compare operation begins when there is a low to high transition on the $\overline{CS}$ pin. You can use the RDY/$\overline{BUSY}$ pin or the RDY/$\overline{BUSY}$ bit in the Status Register to determine whether the state machine has completed the compare separation. Refer to the section on the Status Register for details on how to access and interpret the Status Register.

NOTE: On completion of the compare operation, the state machine updates the second MSB of the Status Register with the result of the compare.

Program Operations for the AT45D041

By specifying the appropriate opcode, data can be written to main memory or to either one of the two buffers (Figure 7).

Buffer Write

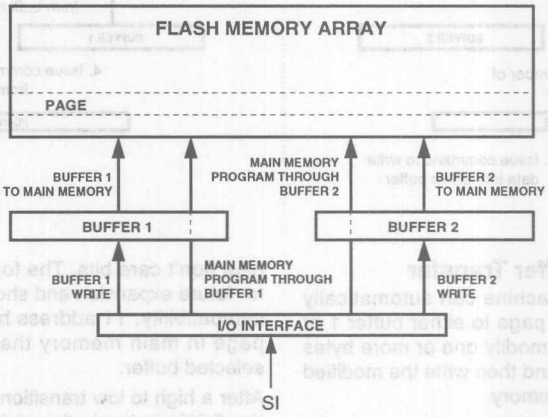
A buffer write allows the user to write data directly into either of the two buffers. To start a buffer write, a Buffer Write command (84H for buffer 1, 87H for buffer 2) is followed by 15 *Reserved* bits and nine address bits. The 15 *Reserved* bits may be used for future expansion and should be zero to ensure upwards compatibility. Nine address bits are required to specify the first byte of data to be written in the 264-byte buffer.

After a high to low transition occurs on the $\overline{CS}$ pin, toggling the SCK pin loads the eight opcode bits, 15 *Reserved* bits,

and nine address bits from the SI pin; at this point data can be written serially from the SI pin. While writing data to a buffer, if the end of the buffer is reached, the Serial DataFlash will wrap around back to the beginning of the buffer. The $\overline{CS}$ pin must remain low during this entire sequence; a low to high transition of the $\overline{CS}$ pin will terminate the write operation.

NOTE: Buffer locations not written to will remain unchanged from their previous values. Any unused buffer locations should be written with "known" data before performing a Buffer to Main Memory Page operation. Atmel recommends writing ones to unused locations to lower energy consumption.

Figure 7. Serial DataFlash Write Operations.



Buffer to Main Memory Page Program with Built-In Erase

The Serial DataFlash's state machine can automatically erase a main memory page and then transfer data from either buffer 1 or buffer 2 into that main memory page. This allows the user to quickly write data to a buffer and not have to issue separate commands to pre-erase a page in the Flash array. You can also use the Buffer to Main Memory Page Program with Built-In Erase command to leave a page in the erased state; to do this, write all 1's to the pages.

Before performing the Buffer to Main Memory Page Program operation, use the Buffer Write operation to write the desired data to either buffer. To start the Buffer to Main Memory Page Program with Built-In Erase command, an 8-bit opcode (83H for buffer 1, 86H for buffer 2) is followed by four *Reserved* bits, 11 address bits, and nine don't care bits. The four *Reserved* bits may be used for future expansion and should be zero to ensure upwards compatibility. 11 address bits are required to specify the page in main memory that is to be erased and then written with the buffer contents.

After a high to low transition occurs on the $\overline{CS}$ pin, toggling the SCK pin loads the eight opcode bits, four *Reserved* bits, 11 address bits, and nine don't care bits from the SI pin. The erase/program operation begins when there is a low to high transition on the $\overline{CS}$ pin. You can use the RDY/$\overline{BUSY}$ pin or the RDY/$\overline{BUSY}$ bit in the Status Register to determine whether the state machine has completed the self-timed operation. Refer to the section on the Status Register for details on how to access and interpret the Status Register.

NOTE: While the state machine is busy transferring data from one buffer to the main memory page, the other buffer may be read from or written to.

Buffer to Main Memory Page Program without Built-In Erase

The Serial DataFlash's state machine can automatically transfer data from either buffer 1 or buffer 2 into a main memory page that has been previously erased. This operation allows the user to quickly write data to a buffer and not have to wait for relatively long with Built-In Erase Flash memory erase time. Note that the Buffer to Main Memory Page Program without Built-In Erase is approximately 30% faster than the Buffer to Main Memory Page Program with Built-In Erase operation.

Before you use the Buffer to Main Memory Page Program without Built-In Erase operation, it is necessary that the main memory page that is being programmed has been previously erased (to erase a page, use the Buffer to Main Memory Page Program with Built-In Erase operation and program in all 1's).

Before performing the Buffer to Main Memory Page Program without Built-In Erase operation, use the Buffer Write operation to write the desired data to either buffer. To start

the Buffer to Main Memory Page Program without Built-In Erase command, an 8-bit opcode (88H for buffer 1, 89H for buffer 2) is followed by four *Reserved* bits, 11 address bits, and nine don't care bits. The four *Reserved* bits may be used for future expansion and should be zero to ensure upwards compatibility. 11 address bits are required to specify the page in main memory that is to be written with the buffer contents.

After a high to low transition occurs on the $\overline{CS}$ pin, toggling the SCK pin loads the eight opcode bits, four *Reserved* bits, 11 address bits, and nine don't care bits from the SI pin. The program operation begins when there is a low to high transition on the $\overline{CS}$ pin. You can use the RDY/$\overline{BUSY}$ pin or the RDY/$\overline{BUSY}$ bit in the Status Register to determine whether the state machine has completed the self-timed operation. Refer to the section on the Status Register for details on how to access and interpret the Status Register.

NOTE: While the state machine is busy transferring data from one buffer to the main memory page, the other buffer may be read from or written to.

Main Memory Page Program

The Main Memory Page Program operation allows you to write to the buffer and transfer the buffer contents to the specified main memory page using a single command. The operation also erases the main memory page before the buffer's data is transferred.

To start the program operation in main memory, a Main Memory Page Program command (82H for buffer 1, 85H for buffer 2) is followed by four *Reserved* bits, and 20 address bits. The four *Reserved* bits may be used for future expansion and should be zero to ensure upwards compatibility. When referencing main memory data, you must specify the page address and the address of the first byte to be written within the buffer. Specifying the page address requires 11 bits. Specifying the first byte to be written within the buffer requires nine bits.

After a high to low transition occurs on the $\overline{CS}$ pin, toggling the SCK pin loads the eight opcode bits, four *Reserved* bits, and 20 address bits from the SI pin. The Serial DataFlash is now ready to take data from the SI pin and store it in the selected data buffer. While writing data to a buffer, if the end of the buffer is reached, the Serial DataFlash will wrap around back to the beginning of the buffer. The $\overline{CS}$ pin must remain low during this entire sequence; a low to high transition of the $\overline{CS}$ pin will initiate the erase of the selected main memory page and then program the data stored in the buffer to that page.

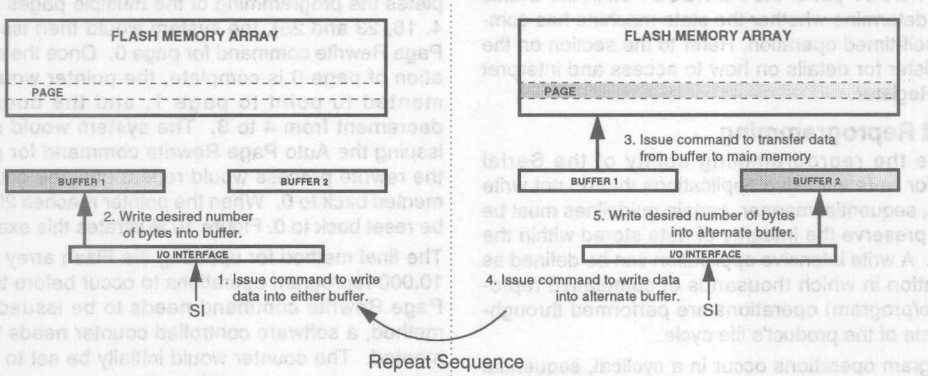
Once the main memory page erase/program has begun, you can use the RDY/$\overline{BUSY}$ pin or the RDY/$\overline{BUSY}$ bit in the Status Register to determine whether the state machine has completed the self-timed operation. Refer to the section on the Status Register for details on how to access and interpret the Status Register.

NOTE: While the state machine is busy transferring data from one buffer to the main memory page, the other buffer may be read from or written to.

Virtual Continuous Write Buffer Operation

The previous sections note that while the state machine is busy transferring data from one buffer to the main memory page, the other buffer may be read from or written to. This feature of the Serial DataFlash allows a virtually continuous write operation provided each of the buffers is not filled faster than the maximum page erase and program time (data cannot be clocked in at a rate in which the time to fill a buffer is less than the maximum t_{EP} time specified in the data sheet). Figure 8 shows the sequence of events that system software can use.

Figure 8. The buffers support a virtually continuous write operation.



- Step 1: Issue a Buffer Write command to write data into either buffer.
- Step 2: Write the desired number of bytes into the buffer.
- Step 3: Issue a Buffer to Main Memory Page Program command.
- Step 4: Issue a Buffer Write command to write data into the alternate buffer.
- Step 5: Write the desired number of bytes into the alternate buffer.
- Step 6: Monitor RDY/$\overline{\text{BUSY}}$ and when the status indicates that the Serial DataFlash is not busy, issue a Buffer to Main Memory Page Program command (for alternate buffer). Return to step 1.

Auto Page Rewrite Command

The Auto Page Rewrite operation allows the Serial DataFlash to automatically rewrite the contents of a main memory page. This operation is a combination of two operations: Main Memory Page to Buffer Transfer and Buffer to Main Memory Page Program with Built-In Erase.

To start the rewrite operation, an Auto Page Rewrite command (58H for buffer 1, 59H for buffer 2) is followed by four *Reserved* bits, 11 address bits, and nine don't care bits. The four *Reserved* bits may be used for future expansion and should be zero to ensure upwards compatibility. 11 address bits are required to specify the page in main memory.

After a high to low transition occurs on the $\overline{\text{CS}}$ pin, toggling the SCK pin loads the eight opcode bits, four *Reserved* bits, 11 address bits, and nine don't care bits from the SI pin. When a low to high transition occurs on the $\overline{\text{CS}}$ pin, the Serial DataFlash transfers data from the page in main memory to the specified buffer, and then programs the data in the buffer back into the same page of main memory. Once the Auto Page Rewrite operation has begun, you can use the RDY/$\overline{\text{BUSY}}$ pin or the RDY/$\overline{\text{BUSY}}$ bit in the Status Register to determine whether the state machine has completed the self-timed operation. Refer to the section on the Status Register for details on how to access and interpret the Status Register.

Extended Reprogramming

To improve the reprogramming ability of the Serial DataFlash for write intensive applications that do not write in a cyclical, sequential manner, certain guidelines must be followed to preserve the integrity of data stored within the Flash array. A write intensive application can be defined as any application in which thousands of cumulative reprogram (erase/program) operations are performed throughout the course of the product's life cycle.

If the reprogram operations occur in a cyclical, sequential manner, then no special guidelines need to be followed. That is, if the Flash pages are updated/rewritten beginning with a specific page (e.g., page 6) and continuing sequentially through the next 2047 pages (e.g., pages 7-2047 and 0-5), and cycled again starting back at the original page (e.g., page 6), then no additional algorithms need to be incorporated into the system's microcontroller or microprocessor software.

However, if the reprogram operations occur in a random fashion in which any number of pages is updated in a random order, then the system must ensure that each page of the Serial DataFlash memory array be updated/rewritten at least once within every 10,000 cumulative page reprogram operations. Depending on the type of application, different methodologies can be used to accomplish the updating of the Flash array.

One method requires that every reprogram operation of a single page be followed by an additional page update. In this scenario, a software controlled pointer would be used to designate which additional page of the Flash array is to be updated. For example, the pointer would initially point to page 0. When the system reprograms a page, say page 12, the system would then issue the Auto Page Rewrite command for page 0 after the completion of the page 12 erase/program operation (t_{EP}). The pointer would then be incremented to point to page 1. When the system reprograms another page, the process would be repeated. When the pointer reaches 2048, it would be reset back to 0. Figure 9 illustrates this example.

Another method for updating the Flash array is somewhat similar to the previous method, but would accommodate reprogram operations of multiple pages. With this method, a software controlled pointer would again be implemented with the addition of a software controlled counter. Like the previous example, the pointer would initially point to page 0 and the counter would be set to 0. When the system reprograms multiple pages, the counter would be incremented for each page reprogram operation. After the system completes the programming of the multiple pages (e.g., pages 4, 18, 23 and 25), the system would then issue the Auto Page Rewrite command for page 0. Once the rewrite operation of page 0 is complete, the pointer would be incremented to point to page 1, and the counter would decrement from 4 to 3. The system would continue by issuing the Auto Page Rewrite command for page 1, and the rewrite process would repeat until the counter decremented back to 0. When the pointer reaches 2048, it would be reset back to 0. Figure 10 illustrates this example.

The final method for updating the Flash array would allow 10,000 reprogram operations to occur before the any Auto Page Rewrite command needs to be issued. With this method, a software controlled counter needs to be implemented. The counter would initially be set to 0, and after every reprogram operation, the counter would be incremented. Once the counter reaches 10,000, the system would begin the Auto Page Rewrite process by issuing the

Auto Page Rewrite command for page 0. Once the rewrite operation of page 0 is complete, the system would continue by rewriting pages 1, 2, 3, and so on until all 2048 pages have been rewritten. After the entire Flash array has been rewritten, the counter would be reset back to 0. Figure 11 illustrates this example.

Figure 9.

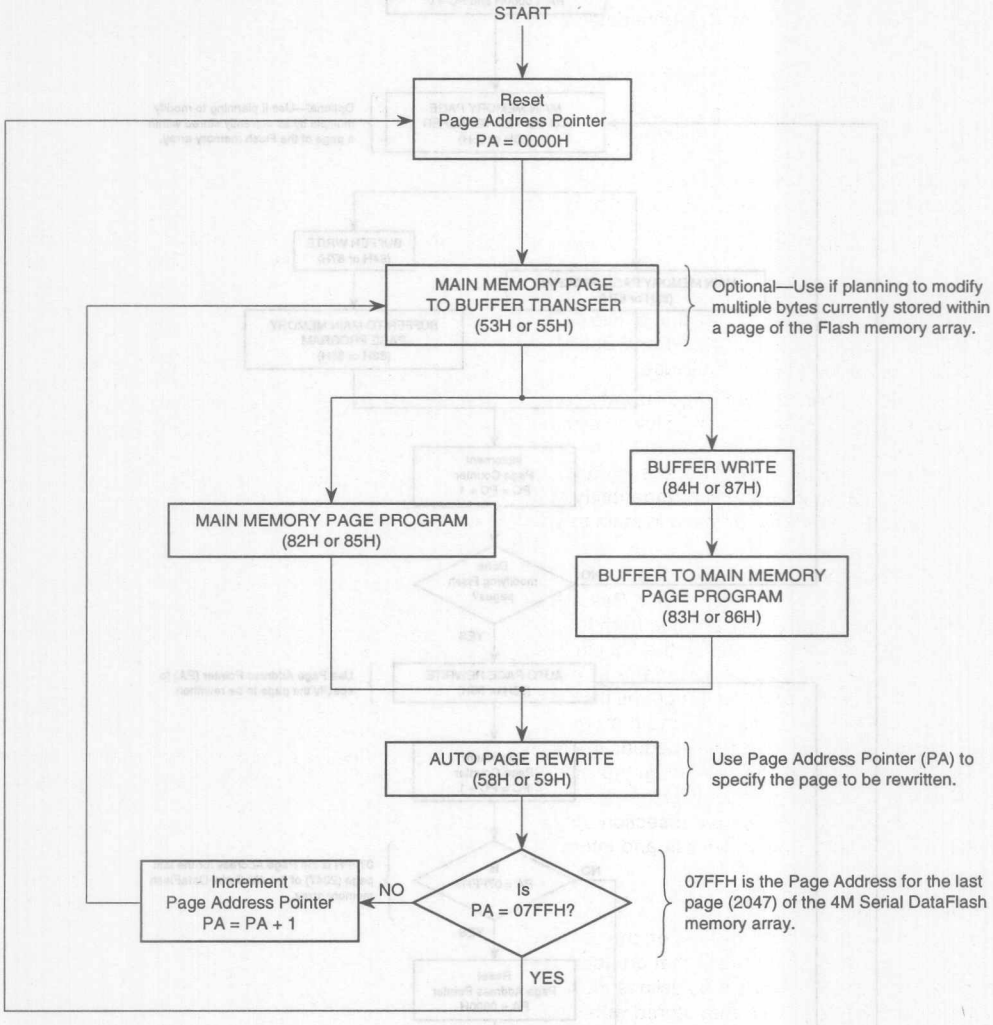


Figure 10.

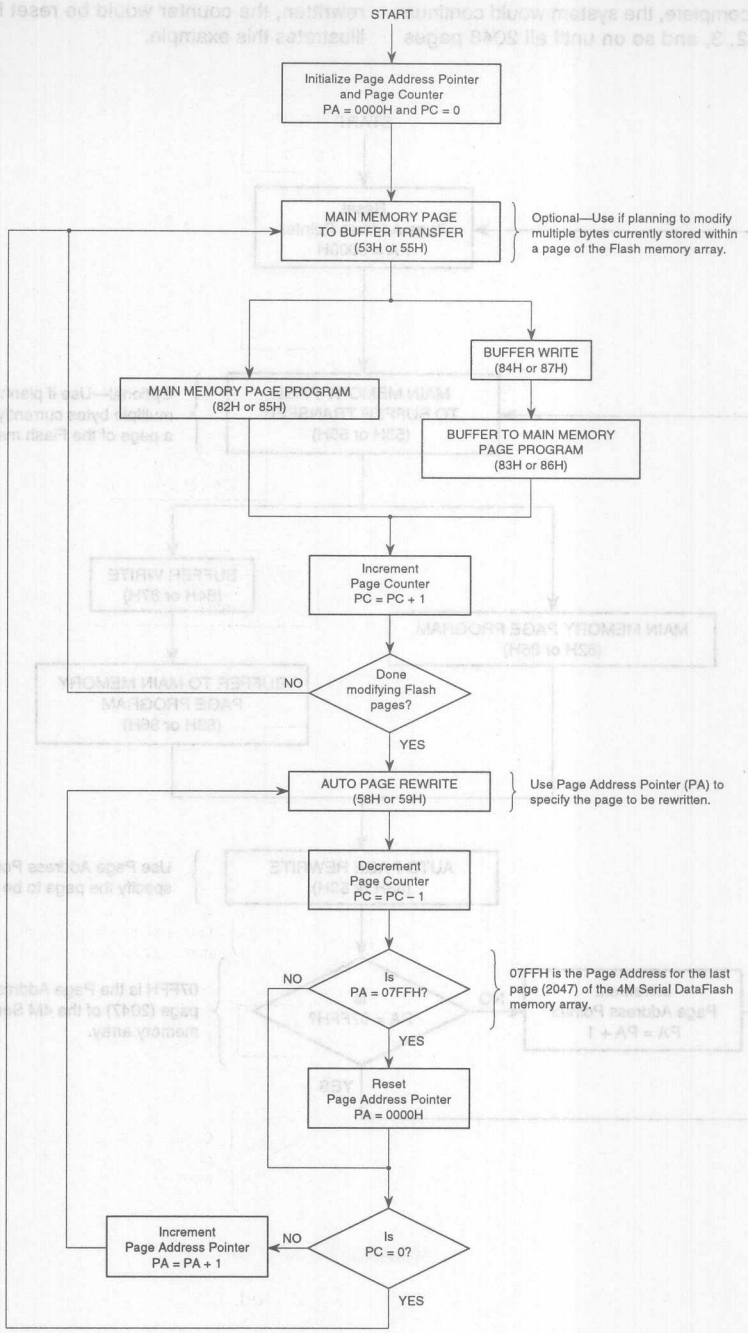
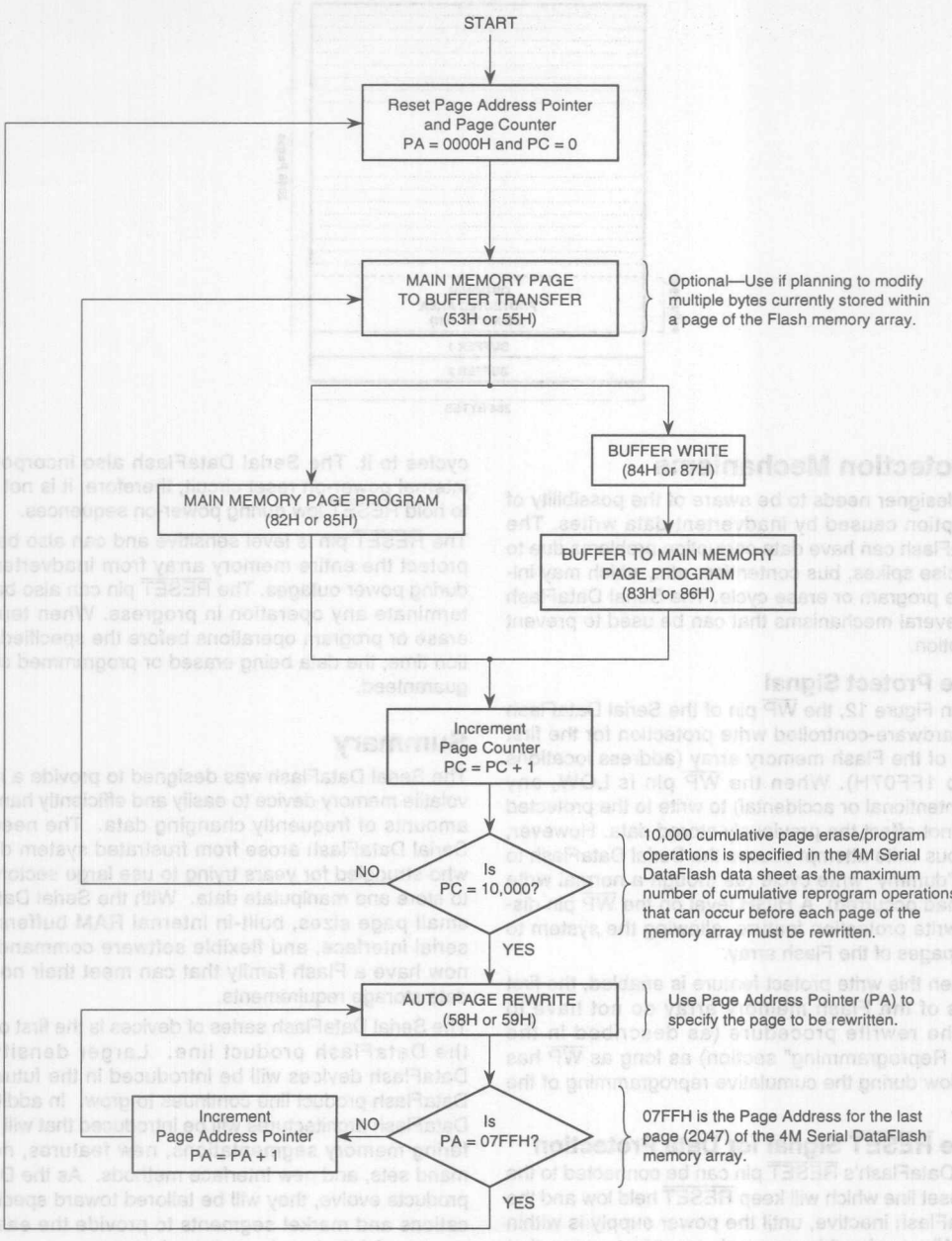
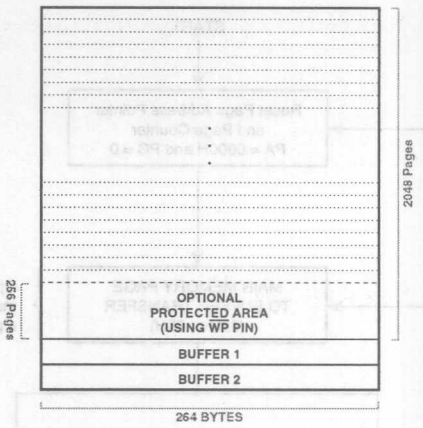

START
Initialize Page Address Pointer and Page Counter PA = 0000H and PC = 0
MAIN MEMORY PAGE TO BUFFER TRANSFER (53H or 55H)
Optional—Use if planning to modify multiple bytes currently stored within a page of the Flash memory array.
BUFFER WRITE (84H or 87H)
MAIN MEMORY PAGE PROGRAM (82H or 85H)
BUFFER TO MAIN MEMORY PAGE PROGRAM (83H or 86H)
Increment Page Counter PC = PC + 1
Done modifying Flash pages?
NO
YES
AUTO PAGE REWRITE (58H or 59H)
Use Page Address Pointer (PA) to specify the page to be rewritten.
Decrement Page Counter PC = PC – 1
Is PA = 07FFH?
NO
YES
07FFH is the Page Address for the last page (2047) of the 4M Serial DataFlash memory array.
Reset Page Address Pointer PA = 0000H
Is PC = 0?
NO
YES
Increment Page Address Pointer PA = PA + 1

Figure 11.



The first 256 pages of the Serial DataFlash can be hardware write protected.

Figure 12.



Data Protection Mechanisms

A system designer needs to be aware of the possibility of data corruption caused by inadvertent data writes. The Serial DataFlash can have data corruption problems due to glitches, noise spikes, bus contention, etc., which may initiate a false program or erase cycle. The Serial DataFlash provides several mechanisms that can be used to prevent data corruption.

The Write Protect Signal

As shown in Figure 12, the $\overline{WP}$ pin of the Serial DataFlash provides hardware-controlled write protection for the first 256 pages of the Flash memory array (address locations 00000H to 1FF07H). When the $\overline{WP}$ pin is LOW, any attempts (intentional or accidental) to write to the protected region will not affect the previously stored data. However, the erroneous write attempt causes the Serial DataFlash to perform a "dummy" write cycle (as though a normal write operation had occurred). A HIGH level on the $\overline{WP}$ pin disables the write protection feature, allowing the system to write to all pages of the Flash array.

NOTE: When this write protect feature is enabled, the first 256 pages of the Flash memory array do not have to undergo the rewrite procedure (as described in the "Extended Reprogramming" section) as long as $\overline{WP}$ has been held low during the cumulative reprogramming of the main array.

Using the $\overline{RESET}$ Signal for Data Protection

The Serial DataFlash's $\overline{RESET}$ pin can be connected to the system's reset line which will keep $\overline{RESET}$ held low and the Serial DataFlash inactive, until the power supply is within tolerance. When using this approach, you must ensure that the memory wakes up before the CPU issues memory read cycles to it. The Serial DataFlash also incorporates an internal power-on reset circuit; therefore, it is not required to hold $\overline{RESET}$ low during power-on sequences.

The $\overline{RESET}$ pin is level sensitive and can also be used to protect the entire memory array from inadvertent writes during power outages. The $\overline{RESET}$ pin can also be used to terminate any operation in progress. When terminating erase or program operations before the specified completion time, the data being erased or programmed cannot be guaranteed.

Summary

The Serial DataFlash was designed to provide a new nonvolatile memory device to easily and efficiently handle large amounts of frequently changing data. The need for the Serial DataFlash arose from frustrated system designers who struggled for years trying to use large sectored Flash to store and manipulate data. With the Serial DataFlash's small page sizes, built-in internal RAM buffers, simple serial interface, and flexible software commands, users now have a Flash family that can meet their nonvolatile data storage requirements.

The Serial DataFlash series of devices is the first offering in the DataFlash product line. Larger density Serial DataFlash devices will be introduced in the future as the DataFlash product line continues to grow. In addition, new DataFlash architectures will be introduced that will have differing memory segmentations, new features, new command sets, and new interface methods. As the DataFlash products evolve, they will be tailored toward specific applications and market segments to provide the easiest and most useful devices for system designers.

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Features

- EE Programmable 65,536 x 1, 131,072 x 1, and 262,144 x 1-bit Serial Memories Designed to Store Configuration Programs for Programmable Gate Arrays
- Simple Interface to SRAM FPGAs Requires only one User I/O Pin
- Compatible With AT6000 FPGAs, ATT3000 FPGA, EPF8000 FPGAs, ORCA FPGAs, XC2000, XC3000, XC4000, XC5000 FPGAs, MPA1000
- Cascadable to Support Additional Configurations or Future Higher-density Arrays (17C128 and 17C256 only)
- Low-power CMOS EEPROM Process
- Programmable Reset Polarity
- Available In the Space-efficient Plastic DIP or Surface-mount PLCC and SOIC Packages
- In-System Programmable Via 2-wire Bus
- Emulation of 24CXX Serial EPROMs
- Available in 3.3V ± 10% LV Version

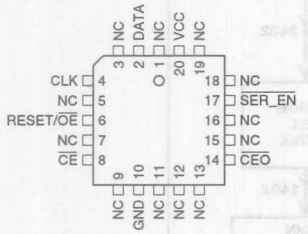
Description

The AT17C65/128/256 and AT17LV65/128/256 (AT17 Series) FPGA Configuration EEPROMS (Configurator) provide an easy-to-use, cost-effective configuration memory for Field Programmable Gate Arrays. The AT17 Series is packaged in the 8-pin DIP and the popular 20-pin PLCC and SOIC. The AT17 Series family uses a simple serial-access procedure to configure one or more FPGA devices. The AT17 Series organization supplies enough memory to configure one or multiple smaller FPGAs. Using a special feature of the AT17 Series, the user can select the polarity of the reset function by programming a special EEPROM bit.

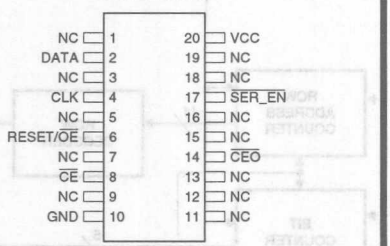
The AT17 Series can be programmed with industry standard programmers.

Pin Configurations

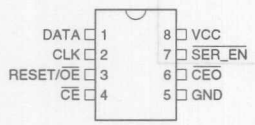
20-pin PLCC



20-Pin SOIC



8-Pin DIP



FPGA Configuration EEPROM

65K, 128K and 256K

AT17C65
AT17C128
AT17C256

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Rev. 0391E–05/97

Controlling The AT17 Series Serial EEPROMs

Most connections between the FPGA device and the Serial EEPROM are simple and self-explanatory.

- The DATA output of the AT17 Series drives DIN of the FPGA devices.
- The master FPGA CCLK output drives the CLK input of the AT17 Series.
- The $\overline{CEO}$ output of any AT17C/LV128/256 drives the $\overline{CE}$ input of the next AT17C/LV128/256 in a cascade chain of PROMs.
- $\overline{SER_EN}$ must be connected to V_{CC}.

There are, however, two different ways to use the inputs $\overline{CE}$ and $\overline{OE}$, as shown in the AC Characteristics waveforms.

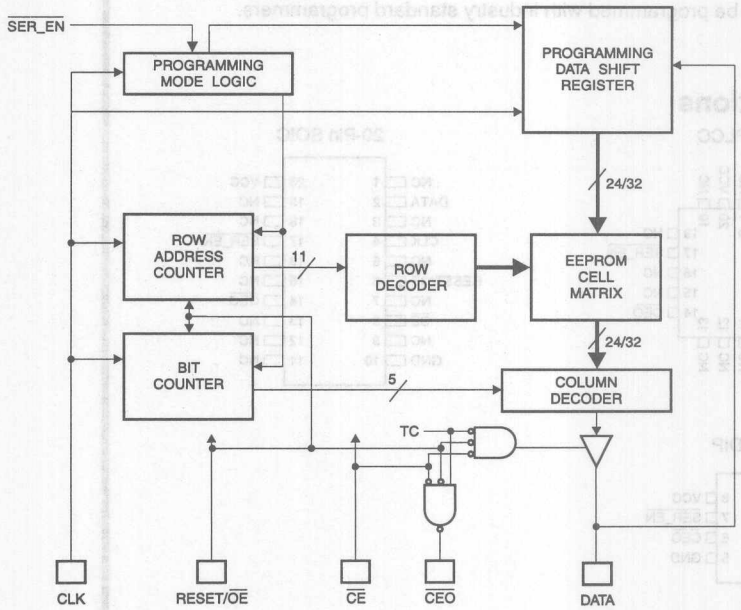
Condition 1

The simplest connection is to have the FPGA D/$\overline{P}$ output drive both $\overline{CE}$ and RESET/$\overline{OE}$ in parallel (Figure 1). Due to its simplicity, however, this method will fail if the FPGA receives an external reset condition during the configuration cycle. If a system reset is applied to the FPGA, it will abort the original configuration and then reset itself for a new configuration, as intended. Of course, the AT17 Series does not see the external reset signal and will not reset its internal address counters and, consequently, will remain out of sync with the FPGA for the remainder of the configuration cycle.

Condition 2

The FPGA D/$\overline{P}$ output drives only the $\overline{CE}$ input of the AT17 Series, while its $\overline{OE}$ input is driven by the inversion of the input to the FPGA $\overline{RESET}$ input pin. This connection works under all normal circumstances, even when the user aborts a configuration before D/$\overline{P}$ has gone High. A High level on the RESET/$\overline{OE}$ input to the AT17C/LVxxx – during FPGA reset – clears the Configurator's internal address pointer, so that the reconfiguration starts at the beginning. The AT17 Series does not require an inverter since the RESET polarity is programmable.

Block Diagram



Pin Configurations

PLCC/ SOIC Pin	DIP Pin	Name	I/O	Description
2	1	DATA	I/O	Three-state DATA output for reading. Input/Output pin for programming.
4	2	CLK	I	Clock input. Used to increment the internal address and bit counter for reading and programming.
6	3	RESET/$\overline{OE}$		RESET/Output Enable input (when $\overline{SER_EN}$ is High). A Low level on both the $\overline{CE}$ and RESET/$\overline{OE}$ inputs enables the data output driver. A High level on RESET/$\overline{OE}$ resets both the addresss and bit counters. A logic polarity of this input is programmable as either RESET/$\overline{OE}$ or $\overline{RESET}$/OE. This document describes the pin as RESET/$\overline{OE}$.
8	4	$\overline{CE}$	I	Chip Enable input. Used for device selection. A Low level on both $\overline{CE}$ and $\overline{OE}$ enables the data output driver. A High level on $\overline{CE}$ disables both the address and bit counters and forces te device into a low power mode. Note this pin will not enable/disable the device in 2-wire Serial mode (ie; when $\overline{SER_EN}$ is Low).
10	5	GND		Ground Pin
14	6	CEO	O	Chip Enable Out output. This signal is asserted Low on the clock cycle following the last bit read from the memory. It will stay Low as long as CE and $\overline{OE}$ are both Low. It will then follow $\overline{CE}$ until $\overline{OE}$ goes High. Thereafter $\overline{CEO}$ will stay High until the entire PROM is read again and senses the status of RESET polarity.
		A2	I	Device selection input, A2. This is used to enable (or select) the device during programming and when $\overline{SER_EN}$ is Low (see Programming Guide for more details).
17	7	$\overline{SER_EN}$	I	Serial enable is normally high during FPGA loading operations. Bringing SER_EN low, enables the 2-wire serial interface for programming.
20	8	VCC		+3.3V/+5V power supply pin.

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-0.1V to V_{CC} + 0.5V
Supply Voltage (V_{CC})	-0.5 V to +7.0V
Maximum Soldering Temp. (10 sec. @ 1/16 in.)	260°C
ESD (R_{ZAP} = 1.5K, C_{ZAP} = 100pF)	2000V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

5

FPGA Master Serial Mode Summary

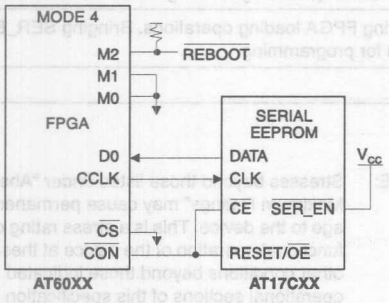
The I/O and logic functions of the FPGA and their associated interconnections are established by a configuration program. The program is loaded either automatically upon power up, or on command, depending on the state of the three FPGA mode pins. In Master Mode, the FPGA automatically loads the configuration program from an external memory. The Serial Configuration EEPROM has been designed for compatibility with the Master Serial Mode.

Cascading Serial Configuration EEPROMs (AT17C/LV128 and AT17C/LV256)

For multiple FPGAs configured as a daisy-chain, or for future FPGAs requiring larger configuration memories, cascaded Configurators provide additional memory (17C/LV128 and 17C/LV256 only).

After the last bit from the first Configurator is read, the next clock signal to the Configurator asserts its $\overline{CEO}$ output Low and disables its DATA line. The second Configurator recognizes the Low level on its $\overline{CE}$ input and enables its DATA output.

Figure 1. Condition 1 Connection



After configuration is complete, the address counters of all cascaded Configurators are reset if the reset signal drives the RESET/$\overline{OE}$ on each Configurator Active.

If the address counters are not to be reset upon completion, then the RESET/$\overline{OE}$ inputs can be tied to ground. For more details, please reference the AT17C Series Programming Guide.

Programming Mode

The programming mode is entered by bringing $\overline{SER_EN}$ Low. In this mode the chip can be programmed by the 2-wire interface. The programming is done at V_{CC} supply only. Programming super voltages are generated inside the chip. See the Programming Specification for Atmel's Configuration Memories Application Note for further information. The AT17C Series parts are read/write at 5V nominal. The AT17LV parts are read/write at 3.0V nominal.

AT17C/LVXXX Reset Polarity

The AT17C/LVXXX lets the user choose the reset polarity as either RESET/$\overline{OE}$ or $\overline{RESET}$/OE.

Standby Mode

The AT17C/LVXXX enters a low-power standby mode whenever $\overline{CE}$ is asserted High. In this mode, the Configurator consumes less than 1.0 mA of current. The output remains in a high impedance state regardless of the state of the $\overline{OE}$ input.

Operating Conditions

Symbol	Description		AT17CXXX		AT17LVXXX		Units
			Min	Max	Min	Max	
V_{CC}	Commercial	Supply voltage relative to GND -0°C to +70°C	4.75	5.25	3.0	3.6	V
	Industrial	Supply voltage relative to GND -40°C to +85C°	4.5	5.5	3.0	3.6	V
	Military	Supply voltage relative to GND -55°C to +125C	4.5	5.5	3.0	3.6	V

DC Characteristics

V_{CC} = 5V ± 5% Commercial / 5V ± 10% Ind./Mil.

Symbol	Description		Min	Max	Units
V_{IH}	High-level input voltage		2.0	V_{CC}	V
V_{IL}	Low-level input voltage		0	0.8	V
V_{OH}	High-level output voltage (I_{OH} = -4 mA)	Commercial	3.7		V
V_{OL}	Low-level output voltage (I_{OL} = +4 mA)			0.32	V
V_{OH}	High-level output voltage (I_{OH} = -4 mA)	Industrial	3.6		V
V_{OL}	Low-level output voltage (I_{OL} = +4 mA)			0.37	V
V_{OH}	High-level output voltage (I_{OH} = -4 mA)	Military	3.5		V
V_{OL}	Low-level output voltage (I_{OL} = +4 mA)			0.4	V
I_{CCA}	Supply current, active mode			10	mA
I_L	Input or output leakage current (V_{IN} = V_{CC} or GND)		-10	10	µA
I_{CCS}	Supply current, standby mode AT17C256	Commercial		75	µA
		Industrial/Military		150	µA
	Supply current, standby mode AT17C128/65	Commercial		1	mA
		Industrial/Military		2	mA

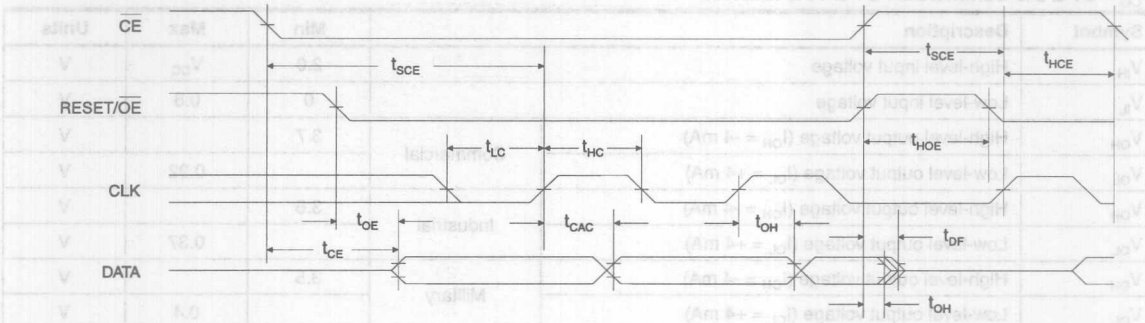
5

DC Characteristics

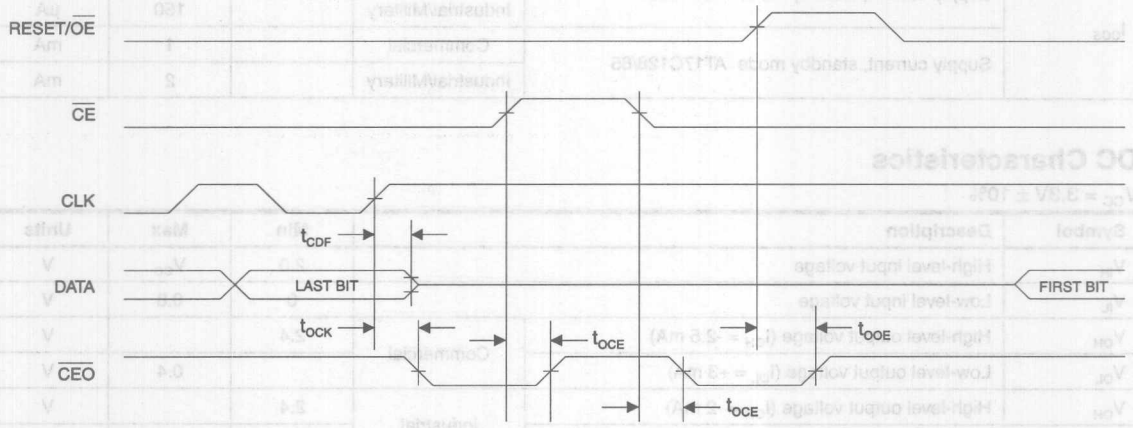
V_{CC} = 3.3V ± 10%

Symbol	Description		Min	Max	Units
V_{IH}	High-level input voltage		2.0	V_{CC}	V
V_{IL}	Low-level input voltage		0	0.8	V
V_{OH}	High-level output voltage (I_{OH} = -2.5 mA)	Commercial	2.4		V
V_{OL}	Low-level output voltage (I_{OL} = +3 mA)			0.4	V
V_{OH}	High-level output voltage (I_{OH} = -2 mA)	Industrial	2.4		V
V_{OL}	Low-level output voltage (I_{OL} = +3 mA)			0.4	V
V_{OH}	High-level output voltage (I_{OH} = -2 mA)	Military	2.4		V
V_{OL}	Low-level output voltage (I_{OL} = +2.5 mA)			0.4	V
I_{CCA}	Supply current, active mode			5	mA
I_L	Input or output leakage current (V_{IN} = V_{CC} or GND)		-10	10	µA
I_{CCS}	Supply current, standby mode	Commercial		50	µA
		Industrial/Military		100	µA

AC Characteristics



AC Characteristics When Cascading



AC Characteristics for AT17C256

V_{CC} = 5V ± 5% Commercial / V_{CC} = 5V ± 10% Ind./Mil.

Symbol	Description	Commercial		Industrial/Military		Units
		Min	Max	Min	Max	
T_{OE}[2]	$\overline{OE}$ to Data Delay		25		25	ns
T_{CE}[2]	$\overline{CE}$ to Data Delay		45		45	ns
T_{CAC}[2]	CLK to Data Delay		50		55	ns
T_{OH}[2]	Data Hold From $\overline{CE}$, $\overline{OE}$, or CLK	0		0		ns
T_{DF}[3]	$\overline{CE}$ or $\overline{OE}$ to Data Float Delay		50		50	ns
T_{LC}	CLK Low Time	20		20		ns
T_{HC}	CLK High Time	20		20		ns
T_{SCE}	$\overline{CE}$ Setup Time to CLK (to guarantee proper counting)	35		40		ns
T_{HCE}	$\overline{CE}$ Hold Time to CLk (to guarantee proper counting)	0		0		ns
T_{HOE}	$\overline{OE}$ High Time (guarantees counter is reset)	20		20		ns
F_{MAX}	MAX Input Clock Frequency		12.5		12.5	MHz

AC Characteristics for AT17C256 When Cascading

V_{CC} = 5V± 5% Commercial / V_{CC} = 5V ± 10% Ind./Mil.

Symbol	Description	Commercial		Industrial/Military		Units
		Min	Max	Min	Max	
T_{CDF}[3]	CLK to Data Float Delay		50		50	ns
T_{OCK}[2]	CLK to $\overline{CEO}$ Delay		35		40	ns
T_{OCE}[2]	CE to $\overline{CEO}$ Delay		35		35	ns
T_{OOE}[2]	RESET/$\overline{OE}$ to $\overline{CEO}$ Delay		30		35	ns

Notes:
1. Preliminary specifications for military operating range only.
2. AC test load = 50 pf.
3. Float delays are measured with 5 pF AC loads. Transition is measured ±200 mV from steady state active levels.

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AC Characteristics for AT17C65/128

V_{CC} = 5V ± 5% Commercial / V_{CC} = 5V ± 10% Ind./Mil.

Symbol	Description	Commercial		Industrial/Military		Units
		Min	Max	Min	Max	
T_{OE}[2]	$\overline{OE}$ to Data Delay		110		150	ns
T_{CE}[2]	$\overline{CE}$ to Data Delay		50		50	ns
T_{CAC}[2]	CLK to Data Delay		50		55	ns
T_{OH}[2]	Data Hold From $\overline{CE}$, $\overline{OE}$, or CLK	0		0		ns
T_{DF}[3]	$\overline{CE}$ or $\overline{OE}$ to Data Float Delay		50		50	ns
T_{LC}	CLK Low Time	30		35		ns
T_{HC}	CLK High Time	30		35		ns
T_{SCE}	$\overline{CE}$ Setup Time to CLK (to guarantee proper counting)	45		50		ns
T_{HCE}	$\overline{CE}$ Hold Time to CLk (to guarantee proper counting)	0		5		ns
T_{HOE}	$\overline{OE}$ High Time (guarantees counter is reset)	50		60		ns
F_{MAX}[4]	MAX Input Clock Frequency		10		10	MHz

AC Characteristics for AT17C65/128 When Cascading

V_{CC} = 5V± 5% Commercial / V_{CC} = 5V ± 10% Ind./Mil.

Symbol	Description	Commercial		Industrial/Military		Units
		Min	Max	Min	Max	
T_{CDF}[3]	CLK to Data Float Delay		50		50	ns
T_{OCK}[2]	CLK to $\overline{CEO}$ Delay		65		75	ns
T_{OCE}[2]	CE to $\overline{CEO}$ Delay		55		60	ns
T_{OE}[2]	RESET/$\overline{OE}$ to $\overline{CEO}$ Delay		55		55	ns

Notes:
1. Preliminary specifications for military operating range only.
2. AC test load = 50 pf.
3. Float delays are measured with 5 pF AC loads. Transition is measured ±200 mV from steady state active levels.
4. During cascade F_{MAX} = 8 MHz.

AC Characteristics

V_{CC} = 3.3V ± 10%

Symbol	Description	Commercial		Industrial/Military		Units
		Min	Max	Min	Max	
T_{OE}[2]	$\overline{OE}$ to Data Delay		40		45	ns
T_{CE}[2]	$\overline{CE}$ to Data Delay		60		60	ns
T_{CAC}[2]	CLK to Data Delay		75		80	ns
T_{OH}[2]	Data Hold From $\overline{CE}$, $\overline{OE}$, or CLK	0		0		ns
T_{DF}[3]	$\overline{CE}$ or $\overline{OE}$ to Data Float Delay		55		55	ns
T_{LC}	CLK Low Time	25		25		ns
T_{HC}	CLK High Time	25		25		ns
T_{SCE}	$\overline{CE}$ Setup Time to CLK (to guarantee proper counting)	35		60		ns
T_{HCE}	$\overline{CE}$ Hold Time to CLk (to guarantee proper counting)	0		0		ns
T_{HOE}	$\overline{OE}$ High Time (guarantees counter is reset)	25		25		ns
F_{MAX}[4]	MAX Input Clock Frequency	10		8	10	MHz

Notes: 1. Preliminary specifications for military operating range only.
2. AC test lead = 50 pf.
3. Float delays are measured with 5 pF AC loads. Transition is measured ±200 mV afrom steady state active levels.
4. During cascade F_{MAX} = 8 MHz.

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AC Characteristics When Cascading

V_{CC} = 3.3V ± 10%

Symbol	Description	Commercial		Industrial/Military		Units
		Min	Max	Min	Max	
T_{CDF}[3]	CLK to Data Float Delay		60		60	ns
T_{OCK}[2]	CLK to $\overline{CEO}$ Delay		55		60	ns
T_{OCE}[2]	CE to $\overline{CEO}$ Delay		55		60	ns
T_{OOE}[2]	RESET/$\overline{OE}$ to $\overline{CEO}$ Delay		40		45	ns

Ordering Information - 5V Devices

Memory Size (K)	Ordering Code	Package	Operation Range
64K	AT17C65-10PC	8P3	Commercial (0°C to 70°C)
	AT17C65-10JC	20J	
	AT17C65-10SC	20S	
	AT17C65-10PI	8P3	Industrial (-40°C to 85°C)
	AT17C65-10JI	20J	
	AT17C65-10SI	20S	
128K	AT17C128-10PC	8P3	Commercial (0°C to 70°C)
	AT17C128-10JC	20J	
	AT17C128-10SC	20S	
	AT17C128-10PI	8P3	Industrial (-40°C to 85°C)
	AT17C128-10JI	20J	
	AT17C128-10SI	20S	
256K	AT17C256-10PC	8P3	Commercial (0°C to 70°C)
	AT17C256-10JC	20J	
	AT17C256-10SC	20S	
	AT17C256-10PI	8P3	Industrial (-40°C to 85°C)
	AT17C256-10JI	20J	
	AT17C256-10SI	20S	

Package Type	
8P3	8-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
20J	20-Lead, Plastic J-Leaded Chip Carrier (PLCC)
20S	20-Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)

Ordering Information - 3.3V Devices

Memory Size (K)	Ordering Code	Package	Operation Range
64K	AT17LV65-10PC AT17LV65-10JC AT17LV65-10SC	8P3 20J 20S	Commercial (0°C to 70°C)
	AT17LV65-10PI AT17LV65-10JI AT17LV65-10SI	8P3 20J 20S	Industrial (-40°C to 85°C)
128K	AT17LV128-10PC AT17LV128-10JC AT17LV128-10SC	8P3 20J 20S	Commercial (0°C to 70°C)
	AT17LV128-10PI AT17LV128-10JI AT17LV128-10SI	8P3 20J 20S	Industrial (-40°C to 85°C)
256K	AT17LV256-10PC AT17LV256-10JC AT17LV256-10SC	8P3 20J 20S	Commercial (0°C to 70°C)
	AT17LV256-10PI AT17LV256-10JI AT17LV256-10SI	8P3 20J 20S	Industrial (-40°C to 85°C)

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Package Type	
8P3	8-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
20J	20-Lead, Plastic J-Leaded Chip Carrier (PLCC)
20S	20-Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)

Programming Specification for Atmel's FPGA Configuration EEPROMs AT17C65/128/256/512/010 AT17C65A/128A/256A/512A/010A

FPGA Configuration EEPROM Programming Specification

Application Note

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The FPGA Configurator

The Configurator is a serial EEPROM memory which also can be used to load programmable devices. This document describes the features needed to program the Configurator, and also covers programming for 3.3V LV devices and Altera Pinout varients.

Serial Bus Overview

The serial bus is a two wire bus; one wire (CLOCK) functions as a clock and is provided by the programmer, the second wire (DATA) is a bi-directional signal and is used to provide data and control information.

Information is transmitted on the serial bus in messages. Each MESSAGE is preceded by a START BIT and is ended with a STOP BIT. The message consists of an integer number of bytes, each byte consists of 8 bits of data and is followed by a ninth ACKNOWLEDGE BIT. This ACKNOWLEDGE BIT is provided by the recipient of the data. This is possible because devices only drive DATA low, the system (in the programming case the Programmer) provides a small pull-up current (1k Ohm equivalent) for the Data Pin.

The MESSAGE FORMAT consists of the bytes shown in the Message Bytes table below. The MESSAGE FORMAT is preceded by a start bit and ended by a stop bit.

The programmer provides all the bytes except for the data bytes when the device is being read. Note that each byte is individually acknowledged. This acknowledgment is provided by the Configurator in all cases except for the data bytes in the read mode, in which case the acknowledge is provided by the programmer.

Bit Format

Data on the DATA pin may change only during CLOCK low times.

Message Bytes

DEVICE ADDRESS	1ST ADDDRESS BYTE	2ND ADDRESS BYTE	3RD ADDRESS BYTE (010/512 Only)	DATA BYTE(S)

Message Format

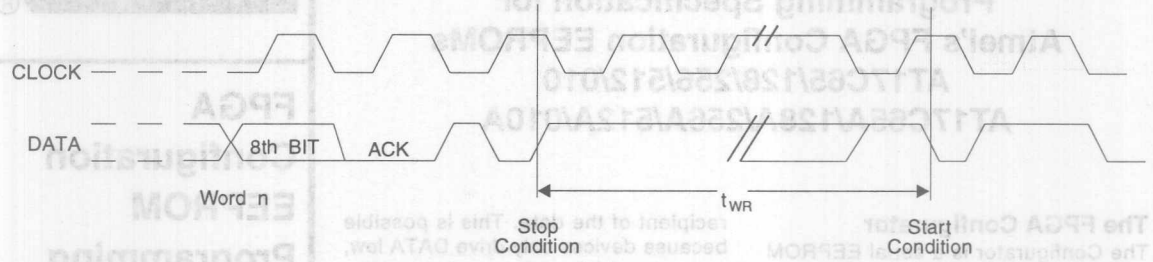
START BIT	DEVICE ADDRESS	1ST ADDRESS BYTE	2ND ADDRESS BYTE	3RD ADDRESS BYTE (010/512 Only)	DATA BYTE(S)	STOP BIT

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Start and Stop Bits

The START BIT is indicated by a high-to-low transition of DATA when CLOCK is high. Similarly, the STOP BIT is generated by a low-to-high transition of DATA when CLOCK is high, as shown below.

Start and Stop Bits



Acknowledge Bit

The ACKNOWLEDGE BIT ("ACK") is shown in the above figure. Note that the ACKNOWLEDGE BIT is provided by the device receiving the byte. The receiving device can accept the byte by asserting a low value on DATA, or it can refuse the byte by asserting (not driving the signal) a 1 on DATA. All bytes must be terminated by either the ACKNOWLEDGE BIT or a STOP BIT.

Bit Ordering Protocol

The most significant bit is the first bit of a byte transmitted on DATA for the DEVICE ADDRESS BYTE and the EEPROM ADDRESS BYTES. It is followed by the lesser significant bits until the eighth bit, the least significant bit is transmitted. This is followed by the acknowledge bit. However, for DATA BYTES (both writing and reading) the first bit transmitted is the least significant bit. This protocol is shown in the tables below.

Device Address Byte

The contents of the Device Address Byte are shown below, along with the order in which the bits are clocked into the device. The A2 bit is provided to allow 2 devices to share a common bus; when programming a single device, the A2 pin must be forced to a logic '0' or '1' level. It is recommended that this pin be connected to 0V (GND) using a 4.7K ohm resistor pulldown.

Note: For the 010/512 only this pin will be pulled to ground if left floating.

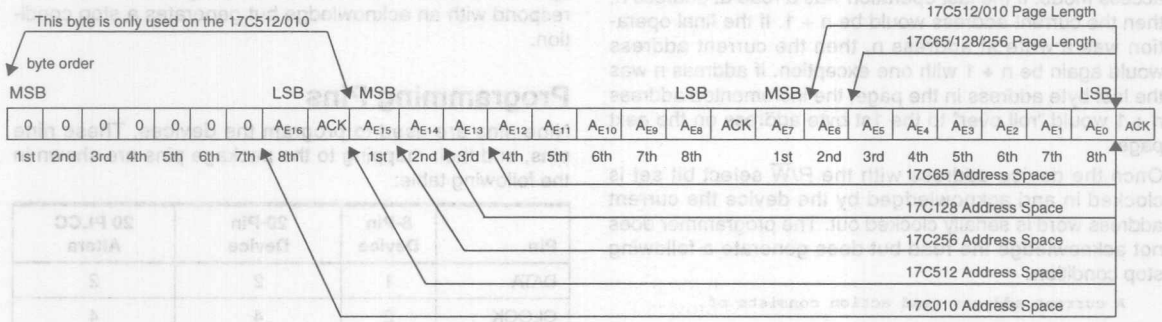
Device Address Byte

MSB							LSB
1	0	1	0	A_2	1	1	R/$\overline{W}$
1st	2nd	3rd	4th	5th	6th	7th	8th

Where: R/$\overline{W}$ = 1 Read
= 0 Write
A2 = 1 if A2 pin is at V_{CC}
= 0 if A2 pin is at GROUND

EEPROM Address

The EEPROM address consists of two bytes on the 17C65/128/256, and three bytes on the 17C512/010. Each address byte is followed by an acknowledge bit (provided by the device which is receiving data). These bytes define the address space of the device, as described below. The order in which each byte is clocked into the device is also indicated. Unused bits in an address byte (e.g. the high order bits above A_{E16} on the 17C010) must be set to "0".



Data Byte

The organization of the Data Byte is shown below. Note that in this case, the data byte is clocked into the device LSB first and MSB last.

Writing

All writing takes place in pages. A page is 64 bytes long on the 17C65/128/256 and 128 bytes long on the 17C512/010, and the page boundaries are addresses where A5 - 0 on the 17C65/128/256 and A6 - 0 on the 17C512/010 are all zero. Writing can start at any address within a page and the number of bytes written must be 64 for the 17C65/128/256 and 128 for the 17C512/010. The first byte is written at the transmitted address. The address is incremented in the device following the receipt of each data word received. Only the lower six bits of the address are incremented and if the address is incremented after the last byte in the page is sent, then the next byte to be written is the first byte of the same page.

Data Byte

LSB							MSB
D0	D1	D2	D3	D4	D5	D6	D7
1st	2nd	3rd	4th	5th	6th	7th	8th

A write action consists of

- a Start Bit
- a Device Address with R/$\overline{W}$ = 0
  - An Acknowledge Bit From the device
- First Word of the Address
  - An Acknowledge Bit From the device
- Second Word of the Address
  - An Acknowledge Bit From the device
- Third Word of Address (AT17C010/AT17512 Only)
  - An ACK from Device
- One or more data bytes (sent to the device)
  - Each followed by an Acknowledge Bit From the device
- a Stop bit

WRITE POLLING: On receipt of the stop bit, the device enters an internally timed write cycle. While the device is busy with this write cycle it will not acknowledge any transfers. Thus the programmer can start the next page write by sending the Start Bit followed by the Device Address. If this is not acknowledged, then the programmer should abandon the transfer without asserting a stop bit. The programmer can then repeat this until an acknowledge is received. When this is received the write action can proceed, i.e., the next byte to be sent is the device address.

Reading

Read operations are initiated the same way as write operations with the exception that the R/$\overline{W}$ bit in the device

address is set to one. There are three read operations: current address read, random read and sequential read.

CURRENT ADDRESS READ: The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained and the device remains in 2-wire access mode. If the last operation was a read at address n, then the current address would be n + 1. If the final operation was a write at address n, then the current address would again be n + 1 with one exception. If address n was the last byte address in the page, the incremented address n + 1 would "roll over" to the 1st byte address on the next page.

Once the device address with the R/$\overline{W}$ select bit set is clocked in and acknowledged by the device the current address word is serially clocked out. The programmer does not acknowledge the read but does generate a following stop condition.

```
A current address read action consists of
    a Start Bit
    a Device Address with R/W = 1
      An Acknowledge Bit From the device
    a data byte from the device
    a stop bit from the programmer.
```

RANDOM READ: A random read requires a "dummy" byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the device, the programmer must generate another start condition. The programmer now initiates a current address read by sending a device address with the R/$\overline{W}$ bit high. The device acknowledges the device address and serially clocks out the data word. The programmer does not acknowledge the read but does generate a following stop condition.

```
A random address read action consists of
  a Start Bit
  a Device Address with R/W = 0
    An Acknowledge Bit From the device
  First Word of the Address
    An Acknowledge Bit From the device
  Second Word of the Address
    An Acknowledge Bit From the device
  Third Word of Address (AT17C010/AT17C512 Only)
    An ACK bit from the device
  a Start Bit
  a Device Address with R/W = 1
    An Acknowledge Bit From the device
  a data byte from the device
  a stop bit from the programmer.
```

SEQUENTIAL READ: Sequential reads are initiated by either a current address read or a random address read. After the programmer receives a data word, it responds with an acknowledge. As long as the device receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words until the memory address limit is reached. The sequential read operation is terminated when the programmer does not respond with an acknowledge but generates a stop condition.

Programming Pins

Nine pins are used to program the devices. These nine pins, and their mapping to the package pins are shown in the following table:

Pin	8-Pin Device	20-Pin Device	20 PLCC Altera
DATA	1	2	2
CLOCK	2	4	4
WP1	N/A	5 (512/010 Only)	5 (512/010 only)
RESET/$\overline{OE}$	3	6	8
WP2	N/A	7 (512/010 Only)	N/A
$\overline{CE}$	4	8	9
GROUND	5	10	10
A2 ($\overline{CEO}$)	6	14	12
READY	N/A	15 (512/010 Only)	15 (512/010 Only)
$\overline{SER_EN}$	7	17	18
V_{CC}	8	20	20

Programmer Functions

The programmer needs to perform the following functions:

1. Check the Manufacturers Code and the Device Code (Not necessary for In-System Programming)
2. Program the device
3. Verify the device
4. Set the Reset Polarity option.

In the order given above. They are performed in the following manner. (The same protocol and operations are used for both 5V and 3.3V devices, and the Altera pinout variants except where stated.)

Reading Manufacturers and Device Code

The 17C512/010 use a different algorithm than the 17C65/128/256 devices for reading the manufacturers and device ID code. On 17C512/010 devices the reading of these bytes are accomplished by performing a read operation with the upper address byte set to binary pattern 0000 0100 and the two lower address bytes set to all zeros during sequence to load in the data word address. On 17C65/128/256 devices the read is done on the manufactures device ID code from address 0 and 1, respectively, by performing a "read" as specified in this spec, with the following DC voltages set:

```
RESET/OE      = 0V
CE            = 11.5 ± 0.5V
A2 (CEO)      = (Same as A2 bit in Device Address,
                usually 0V)
SER_EN        = 0V
```

The correct codes are [1]

```
Manufacturers Code   - Byte 0      1E
Device Code          - Byte 1      FF    17C128
                                   7F    17C65
                                   77    17C256
                                   37    17C512
                                   F7    17C010
```

Note: 1. The Manufacturer's Code and Device Code are read using the same byte ordering specified in the beginning of this document; i.e., LSB first, MSB last.

Programming the Device

All the bytes in the device's page must be written. The order is not important but it is suggested that the device be written sequentially from Byte 0. Writing is accomplished by using the DATA and CLOCK pins and setting the other programming pins as follows:

```
RESET/OE      = 0V
CE            = 0V
A2 (CEO)      = (Same as A2 bit in Device Address,
                usually 0V)
SER_EN        = 0V
```

Write Protect Operation

The 17C family of devices have a "Write Protect" feature which allows portions of the memory to be blocked during write. When the blocking is in effect, data will not be written in the blocked portion and the existing data in the blocked portion will be preserved.

For the 17C65/128/256, the RESET/$\overline{OE}$ pin is used for WRITE PROTECT when in serial mode ($\overline{SER_EN}$ is LOW). When the RESET/$\overline{OE}$ pin is HIGH, memory is protected as follows: (Note $\overline{CE}$ must be low.)

17C65: The lower 1/2 of memory is protected (address 0000 - 0FFF)

17C128: The lower 1/4 of memory is protected (address 0000 - 0FFF)

17C256: The lower 1/4 of memory is protected (address 0000 - 1FFF)

For the 17C512/010, there are two dedicated Write Protect pins; WP1 (pin 5) and WP2 (pin 7). They are decoded to provide protection described below. (WP1/WP2 have weak pull-downs by default. The AT17C/LV512/010A parts do not support WP2):

WP2	WP1	Protection
0	0	No protection
0	1	Addresses 00000 - 07FFF (1/4 of 17C010, 1/2 of 17C512)
1	0	Addresses 00000 - 0FFFF (1/2 of 17C010, All of 17C512)
1	1	Addresses 00000 - 17FFF (3/4 of 17C010, All of 17C512)

Verifying the Device

All bytes in the device must be read and compared to their intended values. Reading is done using the CLOCK and DATA pins with the other programming pins set to the same value as in programming:

```
RESET/OE  = 0V
CE        = 0V
A2 (CEO)  = (Same as A2 bit in Device Address,
            usually 0V)
SER_EN    = 0V
```

Programming the RESET POLARITY Option

All devices in the 17CXXX family have the ability to change the polarity of the RESET/$\overline{OE}$ pin. This is required for the devices to load data correctly for many FPGA families. The 17C65/128/256 use a different algorithm from the 17C512/010; both algorithms are described on the next page.

1. AT17C65/128/256 RESET/$\overline{OE}$ Polarity Programming
   A. Setting the polarity option ACTIVE HIGH OE (ACTIVE LOW RESET): Write a byte "FF" of data to address 3FFF, using the previously defined 2-wire write algorithm, with the other programming pins set to the following:

```
RESET/OE  = Vcc +/- 0.25V
CE        = Vcc +/- 0.25V
A2 (CEO)  = (Same as A2 bit in
            Device Address; usually 0V)
SER_EN    = 0V
```

   This will change the RESET/$\overline{OE}$ pin functionality to $\overline{RESET}$/OE, i.e. active high OE and active low RESET.

   B. Setting the polarity option ACTIVE LOW OE (ACTIVE HIGH RESET): Write a byte "FF" of data to address 3FFF, using the previously defined 2-wire write algorithm, with the other programming pins set to the following:

```
RESET/OE  = 0V
CE        = Vcc +/- 0.25V
A2 (CEO)  = (Same as A2 bit in
            Device Address; usually 0V)
SER_EN    = 0V
```

   This will change the $\overline{RESET}$/OE pin functionality to RESET/$\overline{OE}$, i.e. active low OE and active high RESET (the default condition).

   Important Notes on AT17C65/128/256 Polarity Programming:

   i. The pin conditions above must be maintained during the entire program cycle, i.e. for 10 ms or until the next Device Address is 'ACK'ED' (if using Write Polling).

   ii. After the RESET/$\overline{OE}$ polarity has been modified the AT17C65/128/256 MUST be powered down and back up again before attempting to verify functionality or use the newly programmed polarity function.

   C. Verifying the RESET/OE Polarity on the AT17 C65/128/256

   The following algorithm can be used to read the programmed polarity of the RESET/$\overline{OE}$ pin:

   Power up the device with

```
RESET/OE  = 0V
CE        = 0V
A2 (CEO)  = Input to programmer (High Z)
SER_EN    = Vcc +/- 0.25V
CLOCK     = 0V
DATA      = Input to programmer
```

   In this condition, if the DATA pin is tri-stated, then the RESET/$\overline{OE}$ fuse is programmed for active high OE (active low RESET); if the DATA pin reads a "0" or a "1", the RESET/$\overline{OE}$ fuse is active low OE (active high RESET).

2. AT17C512/010 RESET/$\overline{OE}$ Polarity Programming
   A. Setting the polarity option ACTIVE HIGH OE (ACTIVE LOW RESET): Write 4 bytes "00 00 00 00" to addresses 20000 - 20003, using the previously defined 2-wire write algorithm.

   B. Setting the polarity option ACTIVE LOW OE (ACTIVE HIGH RESET): Write 4 bytes "FF FF FF FF" to addresses 20000 - 20003, using the previously defined 2-wire write algorithm.

   C. Verifying the RESET/$\overline{OE}$ Polarity on the 17C512/010: Read 4 bytes of data from addresses 20000 - 20003, using the previously defined 2-wire Random Read algorithm. If the data is "FF FF FF FF" then the fuse is programmed for ACTIVE LOW OE (ACTIVE HIGH RESET, which is the default condition); if the data is "00 00 00 00" then the fuse is programmed for ACTIVE HIGH OE (ACTIVE LOW RESET).

DC Characteristics

V_{CC} = 5.0V ± 5%, T_A = 15°C - 85°C[1]

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V_{CC}	Supply Voltage		4.75	5.0	5.25	V
I_{CC}	Supply Current	V_{CC} = 5V		2.0	5.0	mA
I_{LL}	Input Leakage Current	$V_{IN} = V_{CC}$ or V_{SS}		0.10	10	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or V_{SS}		0.05	10	µA
V_{IH}	High-Level Input Voltage		V_{CC} x 0.7		V_{CC} + 0.5	V
V_{IL}	Low-Level Input Voltage		-0.5		0.4	V
V_{OL}	Output Low Level Voltage	I_{OL} = 3 mA			0.4	V

Note: 1. This parameter is characterized and is not 100% tested.

AC Characteristics

V_{CC} = 5.0V ± 5%, T_A = 15°C - 85°C[1]

Symbol	Parameter	Min	Max	Units
f_{CLOCK}	Clock Frequency, Clock		400	KHz
t_{LOW}	Clock Pulse Width Low	1.2		µs
t_{HIGH}	Clock Pulse Width High	0.8		µs
t_{AA}	Clock Low to Data Out Valid	0.1	0.9	µs
t_{BUF}	Time the bus must be free before a new transmission can start	1.2		µs
$t_{HD;STA}$	Start Hold Time	0.6		µs
$t_{SU;STA}$	Start Set-Up Time	0.6		µs
$t_{HD\ DAT}$	Data In Hold Time	0		µs
$t_{SU\ DAT}$	Data In Set-up Time	0.1		µs
t_R	Inputs Rise Time		0.3	µs
t_F	Inputs Fall Time		0.3	µs
$t_{SU\ STO}$	Stop Set-up Time	0.6		µs
t_{DH}	Data Out Hold Time	0.05		µs
t_{WR}	Write Cycle Time		10	ms

Note: 1. This parameter is characterized and is not 100% tested.

DC Characteristics

V_{CC} = 3.3V ± 5%, T_A = 15°C - 85°C[1]

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V_{CC}	Supply Voltage		3.0	3.3	3.6	V
I_{CC}	Supply Current	V_{CC} = 3.6		2.0	3.0	mA
I_{LL}	Input Leakage Current	$V_{IN} = V_{CC}$ or V_{SS}		0.10	10	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or V_{SS}		0.05	10	µA
V_{IH}	High-Level Input Voltage		V_{CC} x 0.7		V_{CC} + 0.5	V
V_{IL}	Low-Level Input Voltage		-0.5		0.2	V
V_{OL}	Output Low Level Voltage	I_{OL} = 2.1 mA			0.4	V

Note: 1. This parameter is characterized and is not 100% tested.

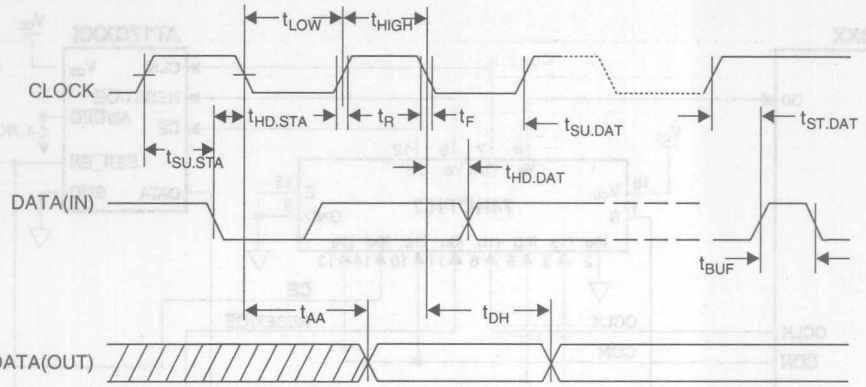
AC Characteristics

V_{CC} = 3.3V ± 5%, T_A = 15°C - 85°C[1]

Symbol	Parameter	Min	Max	Units
f_{CLOCK}	Clock Frequency, Clock		100	KHz
t_{LOW}	Clock Pulse Width Low	4.0		µs
t_{HIGH}	Clock Pulse Width High	4.0		µs
t_{AA}	Clock Low to Data Out Valid	0.1	1.0	µs
t_{BUF}	Time the bus must be free before a new transmission can start	4.5		µs
$t_{HD;STA}$	Start Hold Time	2.0		µs
$t_{SU;STA}$	Start Set-Up Time	2.0		µs
$t_{HD\ DAT}$	Data In Hold Time	0		µs
$t_{SU\ DAT}$	Data In Set-up Time	0.2		µs
t_R	Inputs Rise Time		0.3	µs
t_F	Inputs Fall Time		0.3	µs
$t_{SU\ STO}$	Stop Set-up Time	2.0		µs
t_{DH}	Data Out Hold Time	0.1		µs
t_{WR}	Write Cycle Time		20	ms

Note: 1. This parameter is characterized and is not 100% tested.

Serial Data Timing Diagram



AT17CXXX Configurator In-System Programming Applications

For standard in-system programming, where the RESET/OE polarity does not need to be changed, Figure 1 shows a typical circuit arrangement. A 74HCT157 multiplexer is used to steer the appropriate signals of the configurator, the device(s) programmed by the configurator (typically a FPGA or EPLD), and the ISP (In-System Programmable) port connector. The ISP port may be a connection to a microcontroller on-board or an off-board programmer. The signals need to be muxed to avoid contention and to avoid possible disruption to the EPLD/FPGA operation. Bringing SER_EN low puts the configurator into ISP mode and also switches the multiplexer.

For applications where the RESET/OE polarity may also need to be programmed, Figure 2 shows the expanded ISP port and the associated connections to the multiplexer. Refer to the device programming section in this document for specific details.

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Figure 1. In-System Programming Example (65K/128K/256K)

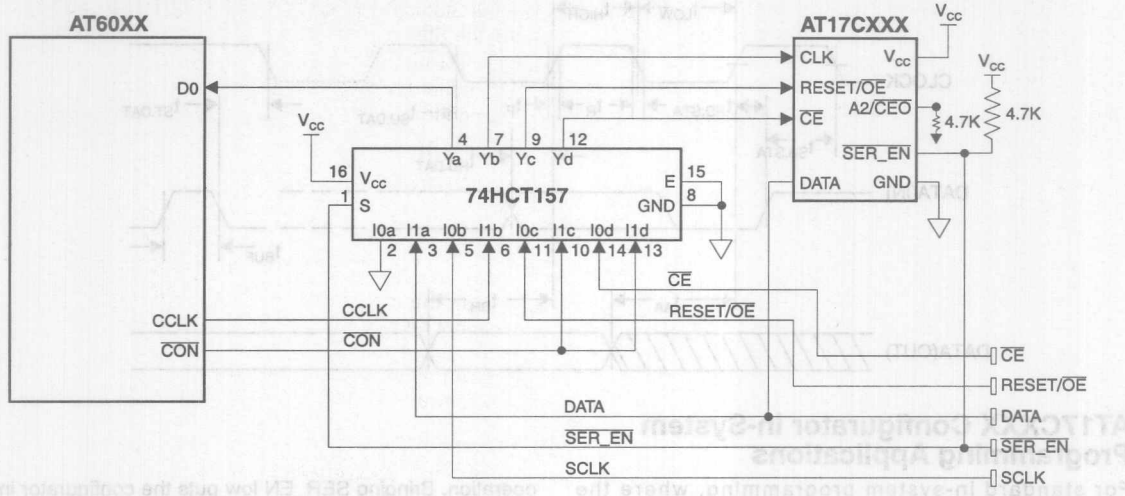


Figure 2. RESET/OE Programming Configuration 65K/128K/256K, (Recommended for use with XC4000/XC5000 devices.)

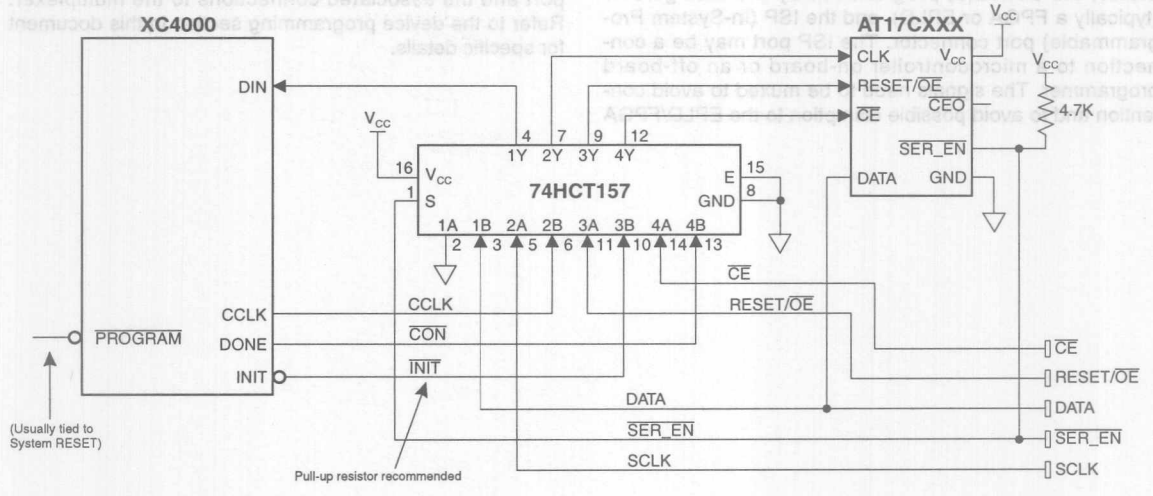
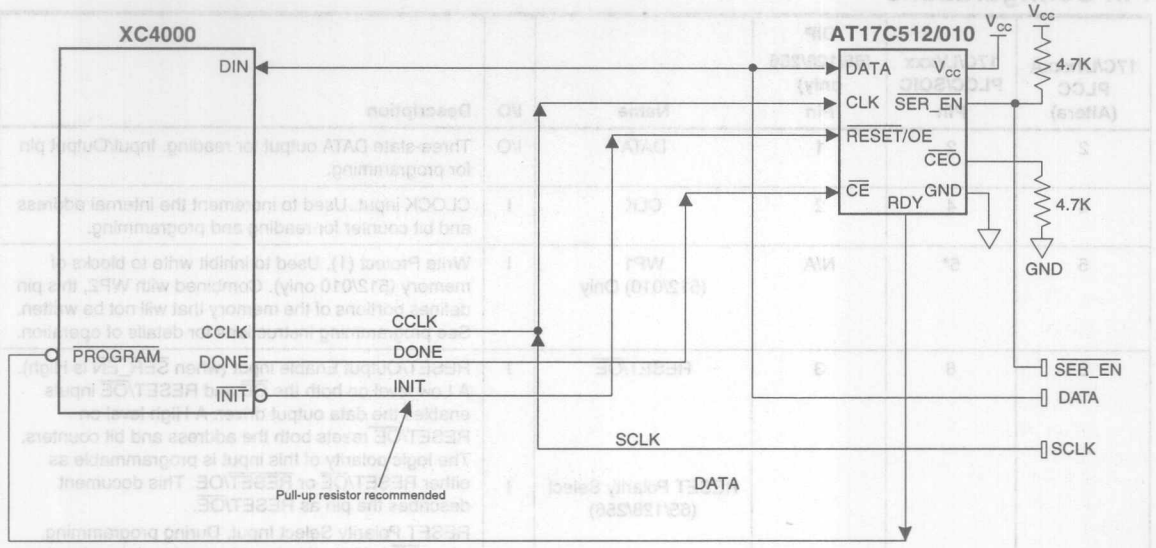


Figure 3. In-System Programming of the AT17C512/010



5

Pin Configurations

17C/LVxxxA PLCC (Altera) Pin	17C/LVxxx PLCC/SOIC Pin	DIP (65/128/256 only) Pin	Name	I/O	Description
2	2	1	DATA	I/O	Three-state DATA output for reading. Input/Output pin for programming.
4	4	2	CLK	I	CLOCK input. Used to increment the internal address and bit counter for reading and programming.
5	5*	N/A	WP1 (512/010) Only	I	Write Protect (1). Used to inhibit write to blocks of memory (512/010 only). Combined with WP2, this pin defines portions of the memory that will not be written. See programming instructions for details of operation.
8	6	3	RESET/$\overline{OE}$	I	RESET/Output Enable input (when $\overline{SER_EN}$ is High). A Low level on both the $\overline{CE}$ and RESET/$\overline{OE}$ inputs enables the data output driver. A High level on RESET/$\overline{OE}$ resets both the address and bit counters. The logic polarity of this input is programmable as either RESET/$\overline{OE}$ or $\overline{RESET}$/OE. This document describes the pin as RESET/$\overline{OE}$.
			RESET Polarity Select (65/128/256)	I	RESET Polarity Select Input. During programming, when $\overline{CE}$ is High, this input is used to determine the polarity of the RESET pin when $\overline{SER_EN}$ is High.
			WP (65/128/256)	I	Write Protect (WP) input (when $\overline{CE}$ is low). When WP is Low or floating, the entire memory can be written. When WP is enabled (High), the lowest 1/4 of the memory cannot be written; i.e., 16K in 17C65, 32K in 17C128, and 64K in 17C256. Note that when WP is High, the chip will still acknowledge the receipt of data, but it will not write it into memory.
N/A	7*	N/A	WP2 (512/010)	I	Write Protect (2). Used to inhibit write to blocks of memory (512/010 only). Combined with WP1, this pin defines portions of the memory that will not be written. See programming instructions for details of operation.
9	8	4	$\overline{CE}$	I	Chip Enable input. Used for device selection only when $\overline{SER_EN}$ is High. A Low level on both $\overline{CE}$ and $\overline{OE}$ enables the data output driver. A High level on $\overline{CE}$ disables both the address and bit counters and forces the device into a low power mode. Note this pin will NOT enable/disable the device in 2-wire Serial mode (i.e., when $\overline{SER_EN}$ is Low). During programming, and when $\overline{CE}$ is Low, the main array is read and written. When $\overline{CE}$ is High, the main array is deselected and a Serial WRITE operation will change the polarity of the RESET pin.
10	10	5	GND		Ground Pin.

Note: * These input pins (512/010 Only) contain a weak internal pull down device and when forced high will draw ~5 µA/pin current when $\overline{SER_EN}$ is low. They will draw no current when $\overline{SER_EN}$ is high.

Pin Configurations (Continued)

17C/LVxxxA PLCC (Altera) Pin	17C/LVxxx PLCC/SOIC Pin	DIP (65/128/256 only) Pin	Name	I/O	Description
12	14*	6	$\overline{CEO}$	I	Chip Enable Output. This signal is asserted Low on the clock cycle following the last bit read from the memory. It will stay Low as long as $\overline{CE}$ and $\overline{OE}$ are both low. It will then follow $\overline{CE}$ until $\overline{OE}$ goes High. Thereafter, $\overline{CEO}$ will stay High until the entire PROM is read again and senses the status of RESET polarity.
			A2	O	Device selection input, A2. Used to enable (select) the device during programming. When $\overline{SER_EN}$ is Low, this pin MUST be at either a logic level '1' or '0' (i.e., not tristate) and the A2 contents of the Device Address must match the condition of the pin for the device to be selected. Atmel recommends addition of a 4.7 KΩ external pull-down resistor for ISP applications.
15	15	N/A	READY (512/010)	O	Ready output (512/010 only). This pin is an open-collector indicator of the device's internal Power-up RESET condition. It is driven Low until the Power-up RESET is cleared, at which time it is released to a tri-state condition. This can be used with an external pullup resistor for a Ready indication.
18	17	7	$\overline{SER_EN}$	I	Serial enable is normally high during FPGA loading operations. Bringing $\overline{SER_EN}$ Low enables the 2-wire serial interface mode for programming.
20	20	8	V_{CC}		Power Supply Pin.

Note: * These input pins (512/010 Only) contain a weak internal pull down device and when forced high will draw ~5 µA/pin current when $\overline{SER_EN}$ is low. They will draw no current when $\overline{SER_EN}$ is high.

Features

- EE Programmable 524,288 x 1 and 1,048,576 x 1-bit Serial Memories Designed to Store Configuration Programs for Field Programmable Gate Arrays (FPGA)
- Simple Interface to SRAM FPGAs
- Compatible with Atmel AT6000, AT40K FPGAs, Altera EPF8K, EPF10K, EPF6K FPGAs, ORCA FPGAs, Xilinx XC3000, XC4000, XC5200 FPGAs, Motorola MPA1000 FPGAs
- Cascadable to Support Additional Configurations or Future Higher-density Arrays
- Low-power CMOS EEPROM Process
- Programmable Reset Polarity
- Available In PLCC Package (Pin Compatable across Product Family)
- In-System Programmable Via 2-wire Bus
- Emulation of 24CXX Serial EPROMs
- Available in 3.3V ± 10% LV and 5V Versions
- System Friendly READY Pin

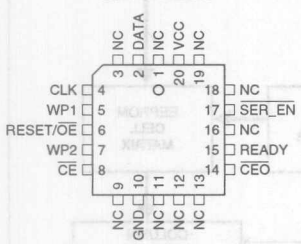
Description

The AT17C512/010 and AT17LV512/010 (high-density AT17 Series) FPGA Configuration EEPROMs (Configurators) provide an easy-to-use, cost-effective configuration memory for Field Programmable Gate Arrays. The high-density AT17 Series is packaged in the popular 20-pin PLCC. The high-density AT17 Series family uses a simple serial-access procedure to configure one or more FPGA devices. The high-density AT17 Series organization supplies enough memory to configure one or multiple smaller FPGAs. The user can select the polarity of the reset function by programming one EEPROM byte. The devices also support a write protection mode and a system friendly READY pin, which signifies a "good" power level to the device and can be used to ensure reliable system power-up.

The high-density AT17 Series can be programmed with industry-standard programmers, and the Atmel ATDH2200 Programming board.

Pin Configurations

20-Pin PLCC



FPGA Configuration EEPROM Memory

512K and 1M

AT17C512
AT17LV512
AT17C010
AT17LV010

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Rev. 0944A–12/97

Controlling The High-Density AT17 Series Serial EEPROMs

Most connections between the FPGA device and the Serial EEPROM are simple and self-explanatory:

- The DATA output of the high-density AT17 Series drives DIN of the FPGA devices.
- The master FPGA CCLK output drives the CLK input of the high-density AT17 Series.
- The $\overline{CEO}$ output of any AT17C/LV512/010 drives the $\overline{CE}$ input of the next AT17C/LV512/010 in a cascade chain of PROMs.
- $\overline{SER_EN}$ must be connected to V_{CC}, (except during ISP).

READY is available as an open-collector indicator of the device's RESET status; it is driven Low while the device is in its POWER-ON RESET cycle and released (tri-stated) when the cycle is complete.

There are two different ways to use the inputs $\overline{CE}$ and $\overline{OE}$, as shown in the AC Characteristics waveforms.

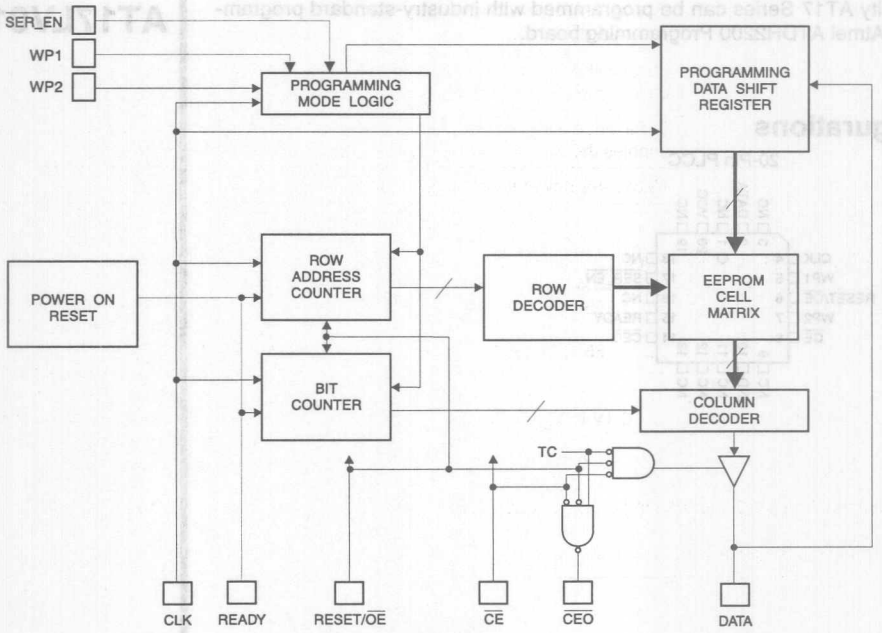
Condition 1

The simplest connection is to have the FPGA D/$\overline{P}$ output drive both $\overline{CE}$ and RESET/$\overline{OE}$ in parallel (Figure 1). Due to its simplicity, however, this method will fail if the FPGA receives an external reset condition during the configuration cycle. If a system reset is applied to the FPGA, it will abort the original configuration and then reset itself for a new configuration, as intended. Of course, the high-density AT17 Series does not see the external reset signal and will not reset its internal address counters and, consequently, will remain out of sync with the FPGA for the remainder of the configuration cycle.

Condition 2

The FPGA D/$\overline{P}$ output drives only the $\overline{CE}$ input of the high-density AT17 Series, while its $\overline{OE}$ input is driven by the inversion of the input to the FPGA $\overline{RESET}$ input pin. This connection works under all normal circumstances, even when the user aborts a configuration before D/$\overline{P}$ has gone High. A High level on the RESET/$\overline{OE}$ input to the AT17C/LVxxx – during FPGA reset – clears the Configurator's internal address pointer, so that the reconfiguration starts at the beginning. The high-density AT17 Series does not require an inverter since the RESET polarity is programmable.

Block Diagram



Pin Configurations

20 PLCC	Name	I/O	Description
2	DATA	I/O	Three-state DATA output for reading. Input/Output pin for programming.
4	CLK	I	Clock input. Used to increment the internal address and bit counter for reading and programming.
5	WP1	I	WRITE PROTECT (1). Used to protect portions of memory during programming. See programming guide for details.
6	RESET/$\overline{OE}$	I	RESET/Output Enable input (when $\overline{SER_EN}$ is High). A Low level on both the $\overline{CE}$ and RESET/$\overline{OE}$ inputs enables the data output driver. A High level on RESET/$\overline{OE}$ resets both the address and bit counters. The logic polarity of this input is programmable as either RESET/$\overline{OE}$ or $\overline{RESET}$/OE. This document describes the pin as RESET/$\overline{OE}$.
7	WP2	I	WRITE PROTECT (2). Used to protect portions of memory during programming. See programming guide for details.
8	$\overline{CE}$	I	Chip Enable input. Used for device selection. A Low level on both $\overline{CE}$ and $\overline{OE}$ enables the data output driver. A High level on $\overline{CE}$ disables both the address and bit counters and forces the device into a low power mode. Note this pin will not enable/disable the device in 2-wire Serial Programming mode (i.e., when $\overline{SER_EN}$ is Low).
10	GND		Ground pin.
14	$\overline{CEO}$	O	Chip Enable Out output. This signal is asserted Low on the clock cycle following the last bit read from the memory. It will stay Low as long as CE and $\overline{OE}$ are both Low. It will then follow $\overline{CE}$ until $\overline{OE}$ goes High. Thereafter, $\overline{CEO}$ will stay High until the entire PROM is read again and senses the status of RESET polarity.
	A2	I	Device selection input, A2. This is used to enable (or select) the device during programming, when $\overline{SER_EN}$ is Low (see Programming Guide for more details)
15	READY	O	Open collector reset state indicator. Driven Low during power-up reset, released when power-up is complete. (Recommend a 4.7KΩ Pull-up on this pin if used).
17	$\overline{SER_EN}$	I	Serial enable is normally high during FPGA loading operations. Bringing SER_EN Low, enables the two wire serial interface mode for programming.
20	VCC		+3.3V/+5V power supply pin.

5

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-0.1V to V_{CC} + 0.5V
Supply Voltage (V_{CC})	-0.5V to +7.0V
Maximum Soldering Temp. (10 s @ 1/16 in.)	260°C
ESD (R_{ZAP} = 1.5K, C_{ZAP} = 100 pF)	2000V

*NOTICE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

FPGA Master Serial Mode Summary

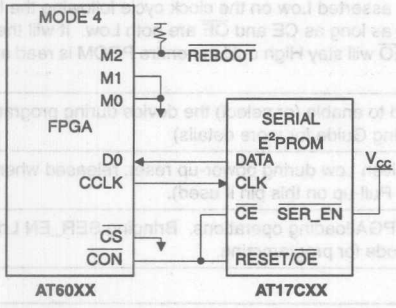
The I/O and logic functions of the FPGA and their associated interconnections are established by a configuration program. The program is loaded either automatically upon power up, or on command, depending on the state of the three FPGA mode pins. In Master Mode, the FPGA automatically loads the configuration program from an external memory. The Serial Configuration EEPROM has been designed for compatibility with the Master Serial Mode.

Cascading Serial Configuration EEPROMs

For multiple FPGAs configured as a daisy-chain, or for future FPGAs requiring larger configuration memories, cascaded Configurators provide additional memory.

As the last bit from the first Configurator is read, the clock signal to the Configurator asserts its $\overline{CEO}$ output Low and disables its DATA line. The second Configurator recognizes the Low level on its $\overline{CE}$ input and enables its DATA output.

Figure 1. Condition 1 Connection



After configuration is complete, the address counters of all cascaded Configurators are reset if the reset signal drives the RESET/$\overline{OE}$ on each Configurator to its active (High) level.

If the address counters are not to be reset upon completion, then the RESET/$\overline{OE}$ inputs can be tied to ground. For more details, please reference the AT17C Series Programming Guide.

Programming Mode

The programming mode is entered by bringing $\overline{SER_EN}$ Low. In this mode the chip can be programmed by the 2-wire interface. The programming is done at V_{CC} supply only. Programming super voltages are generated inside the chip. See the Programming Specification for Atmel's Configuration Memories Application Note for further information. The AT17C Series parts are read/write at 5V nominal. The AT17LV parts are read/write at 3.3V nominal.

AT17C/LVXXX Reset Polarity

The AT17C/LVXXX lets the user choose the reset polarity as either RESET/$\overline{OE}$ or $\overline{RESET}$/OE.

Standby Mode

The AT17C/LVXXX enters a low-power standby mode whenever $\overline{CE}$ is asserted High. In this mode, the Configurator consumes less than 0.5mA at 5.0 volts. The output remains in a high impedance state regardless of the state of the $\overline{OE}$ input.

Operating Conditions

Symbol	Description		AT17CXXX Min	AT17CXXX Max	AT17LVXXX Min	AT17LVXXX Max	Units
V_{CC}	Commercial	Supply voltage relative to GND -0°C to +70°C	4.75	5.25	3.0	3.6	V
	Industrial	Supply voltage relative to GND -40°C to +85°C	4.5	5.5	3.0	3.6	V
	Military	Supply voltage relative to GND -55°C to +125°C	4.5	5.5	3.0	3.6	V

DC Characteristics

V_{CC} = 5V ± 5% Commercial / 5V ± 10% Ind./Mil.

Symbol	Description		Min	Max	Units
V_{IH}	High-level input voltage		2.0	V_{CC}	V
V_{IL}	Low-level input voltage		0	0.8	V
V_{OH}	High-level output voltage (I_{OH} = -4 mA)	Commercial	3.86		V
V_{OL}	Low-level output voltage (I_{OL} = +4 mA)			0.32	V
V_{OH}	High-level output voltage (I_{OH} = -4 mA)	Industrial	3.76		V
V_{OL}	Low-level output voltage (I_{OL} = +4 mA)			0.37	V
V_{OH}	High-level output voltage (I_{OH} = -4 mA)	Military	3.7		V
V_{OL}	Low-level output voltage (I_{OL} = +4 mA)			0.4	V
I_{CCA}	Supply current, active mode (at FMAX)			10	mA
I_L	Input or output leakage current (V_{IN} = V_{CC} or GND)		-10	10	µA
I_{CCS}	Supply current, standby mode	Commercial		0.5	mA
		Industrial/Military		0.5	mA

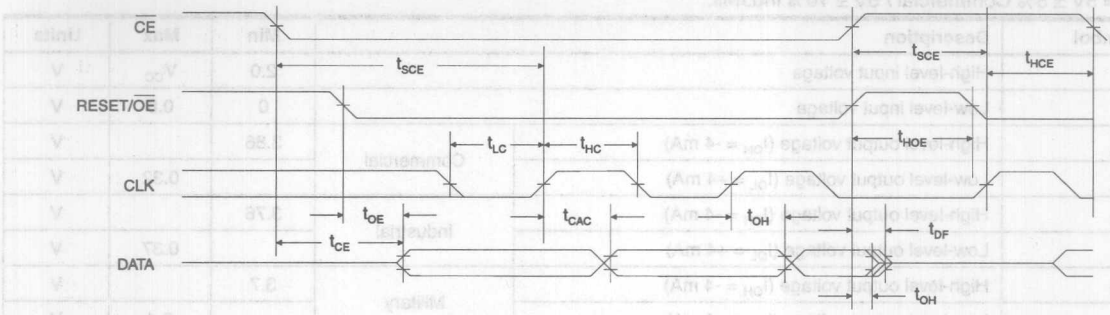
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DC Characteristics

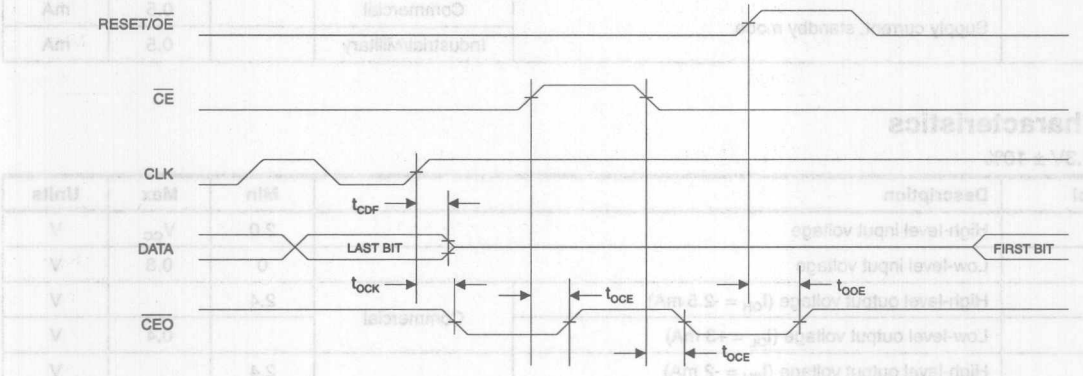
V_{CC} = 3.3V ± 10%

Symbol	Description		Min	Max	Units
V_{IH}	High-level input voltage		2.0	V_{CC}	V
V_{IL}	Low-level input voltage		0	0.8	V
V_{OH}	High-level output voltage (I_{OH} = -2.5 mA)	Commercial	2.4		V
V_{OL}	Low-level output voltage (I_{OL} = +3 mA)			0.4	V
V_{OH}	High-level output voltage (I_{OH} = -2 mA)	Industrial	2.4		V
V_{OL}	Low-level output voltage (I_{OL} = +3 mA)			0.4	V
V_{OH}	High-level output voltage (I_{OH} = -2 mA)	Military	2.4		V
V_{OL}	Low-level output voltage (I_{OL} = +2.5 mA)			0.4	V
I_{CCA}	Supply current, active mode			5	mA
I_L	Input or output leakage current (V_{IN} = V_{CC} or GND)		-10	10	µA
I_{CCS}	Supply current, standby mode	Commercial		100	µA
		Industrial/Military		100	µA

AC Characteristics



AC Characteristics When Cascading



AC Characteristics for AT17C512/010

V_{CC} = 5V ± 5% Commercial / V_{CC} = 5V ± 10% Ind./Mil

Symbol	Description	Commercial/Industrial		Military		Units
		Min	Max	Min	Max	
T_{OE} (2)	$\overline{OE}$ to Data Delay		30		35	ns
T_{CE} (2)	$\overline{CE}$ to Data Delay		45		45	ns
T_{CAC} (2)	CLK to Data Delay		50		50	ns
T_{OH} (2)	Data Hold From $\overline{CE}$, $\overline{OE}$, or CLK	0		0		ns
T_{DF} (3)	$\overline{CE}$ or $\overline{OE}$ to Data Float Delay		50		50	ns
T_{LC}	CLK Low Time	20		20		ns
T_{HC}	CLK High Time	20		20		ns
T_{SCE}	$\overline{CE}$ Setup Time to CLK (to guarantee proper counting)	20		25		ns
T_{HCE}	$\overline{CE}$ Hold Time to CLK (to guarantee proper counting)	0		0		ns
T_{HOE}	$\overline{OE}$ High Time (Guarantees Counter Is Reset)	20		20		ns
F_{MAX}	MAX Input Clock Frequency	15		15		MHz
V_{RDY}	Ready Pin Open Collector Voltage	1.2	2.2	1.2	2.2	V

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AC Characteristics for AT17C512/010 When Cascading

V_{CC} = 5V± 5% Commercial / V_{CC} = 5V ± 10% Ind./Mil.

Symbol	Description	Commercial/Industrial		Military		Units
		Min	Max	Min	Max	
T_{CDF} (3)	CLK to Data Float Delay		50		50	ns
T_{OCK} (2)	CLK to $\overline{CEO}$ Delay		35		40	ns
T_{OCE} (2)	CE to $\overline{CEO}$ Delay		35		35	ns
T_{OOE} (2)	RESET/$\overline{OE}$ to $\overline{CEO}$ Delay		30		30	ns

Notes: 1. Preliminary specifications for military operating range only.
2. AC test load = 50 pF.
3. Float delays are measured with 5 pF AC loads. Transition is measured ± 200 mV from steady state active levels.

AC Characteristics for AT17LV512/010

V_{CC} = 3.3V ± 10%

Symbol	Description	Commercial/Industrial		Military		Units
		Min	Max	Min	Max	
T_{OE}[2]	$\overline{OE}$ to Data Delay		50		55	ns
T_{CE}[2]	$\overline{CE}$ to Data Delay		55		60	ns
T_{CAC}[2]	CLK to Data Delay		55		60	ns
T_{OH}	Data Hold From $\overline{CE}$, $\overline{OE}$, or CLK	0		0		ns
T_{DF}[3]	$\overline{CE}$ or $\overline{OE}$ to Data Float Delay		50		50	ns
T_{LC}	CLK Low Time	25		25		ns
T_{HC}	CLK High Time	25		25		ns
T_{SCE}	$\overline{CE}$ Setup Time to CLK (to guarantee proper counting)	30		35		ns
T_{HCE}	$\overline{CE}$ Hold Time to CLK (to guarantee proper counting)	0		0		ns
T_{HOE}	$\overline{OE}$ High Time (Guarantees Counter Is Reset)	25		25		ns
F_{MAX}[4]	MAX Input Clock Frequency	15		10		MHz
V_{RDY}	Ready Pin Open Collector Voltage	1.2	2.2	1.2	2.2	V

Notes: 1. Preliminary specifications for military operating range only.
2. AC test load = 50 pF.
3. Float delays are measured with 5 pF AC loads. Transition is measured ± 200 mV from steady state active levels.
4. During cascade F_{MAX} = 12.5 MHz.

AC Characteristics for AT17LV512/010 When Cascading

V_{CC} = 3.3V ± 10%

Symbol	Description	Commercial/Industrial		Military		Units
		Min	Max	Min	Max	
T_{CDF}[3]	CLK to Data Float Delay		50		50	ns
T_{OCK}[2]	CLK to $\overline{CEO}$ Delay		50		55	ns
T_{OCE}[2]	CE to $\overline{CEO}$ Delay		35		40	ns
T_{OOE}[2]	RESET/$\overline{OE}$ to $\overline{CEO}$ Delay		35		35	ns

Ordering Information - 5V Devices

Memory Size	Ordering Code	Package	Operation Range
512K	AT17C512-10JC	20J	Commercial (0°C to 70°C)
	AT17C512-10JI	20J	Industrial (-40°C to 85°C)
1M	AT17C010-10JC	20J	Commercial (0°C to 70°C)
	AT17C010-10JI	20J	Industrial (-40°C to 85°C)

Ordering Information - 3.3V Devices

Memory Size	Ordering Code	Package	Operation Range
512K	AT17LV512-10JC	20J	Commercial (0°C to 70°C)
	AT17LV512-10JI	20J	Industrial (-40°C to 85°C)
1M	AT17LV010-10JC	20J	Commercial (0°C to 70°C)
	AT17LV010-10JI	20J	Industrial (-40°C to 85°C)

Package Type	
20J	20 Lead, Plastic J-Leaded Chip Carrier (PLCC)

Ordering Information - 5V Devices

Memory Size	Ordering Code	Package	Operation Range
512K	AT17C512-10JC	20J	Commercial (0°C to 70°C)
	AT17C512-10JI	20J	Industrial (-40°C to 85°C)
1M	AT17C010-10JC	20J	Commercial (0°C to 70°C)
	AT17C010-10JI	20J	Industrial (-40°C to 85°C)

Ordering Information - 3.3V Devices

Memory Size	Ordering Code	Package	Operation Range
512K	AT17LV512-10JC	20J	Commercial (0°C to 70°C)
	AT17LV512-10JI	20J	Industrial (-40°C to 85°C)
1M	AT17LV010-10JC	20J	Commercial (0°C to 70°C)
	AT17LV010-10JI	20J	Industrial (-40°C to 85°C)

Package Type	
20J	20 Lead, Plastic J-Leaded Chip Carrier (PLCC)

Features

- Serial EEPROM Family for Configuring Altera FLEX® 10K Devices
- Simple, Easy-to-use 4-pin Interface
- EE Programmable 1M Bit Serial Memories Designed To Store Configuration Programs For Programmable Gate Arrays
- Cascadable To Support Additional Configurations or Future Higher-density Arrays
- Low-power CMOS EEPROM Process
- Programmable Reset Polarity
- Available in the Space-efficient Surface-mount PLCC Package
- In-System Programmable Via 2-Wire Bus
- Emulation of 24CXX Serial EPROMs
- Available in 3.3V ± 10% LV and 5V ± 5% C Versions

Description

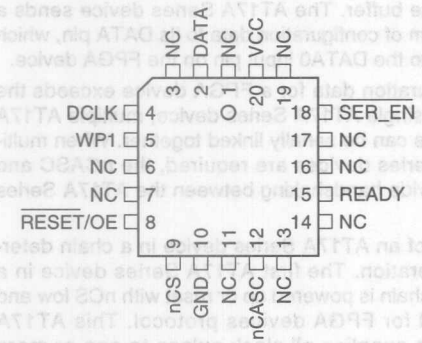
The AT17C512/010A and AT17LV512/010A (AT17A Series) FPGA Configuration EEPROMs (Configurators) provide and easy-to-use, cost-effective configuration memory for programming Altera FLEX Field Programmable Gate Arrays, FPGA, (the "devices"). The AT17A Series is packaged in the popular 20-pin PLCC package. The AT17A Series family uses a simple serial-access procedure to configure one or more FPGA devices. The AT17A Series organization supplies enough memory to configure one or multiple smaller FPGAs. Using a special feature of the AT17A Series, the user can select the polarity of the reset function by programming an EEPROM byte. The AT17C/LV512/010A parts generate their own internal clock and can be used as a system "master" for loading the FPGA devices.

The Atmel devices also supports a system friendly READY pin and a write protect mechanism. The READY pin is used to simplify system power-up considerations. The WP1 pin is used to protect part of the device memory during in-system programming.

The AT17A Series can be programmed with industry standard programmers.

Pin Configurations

20-Pin PLCC



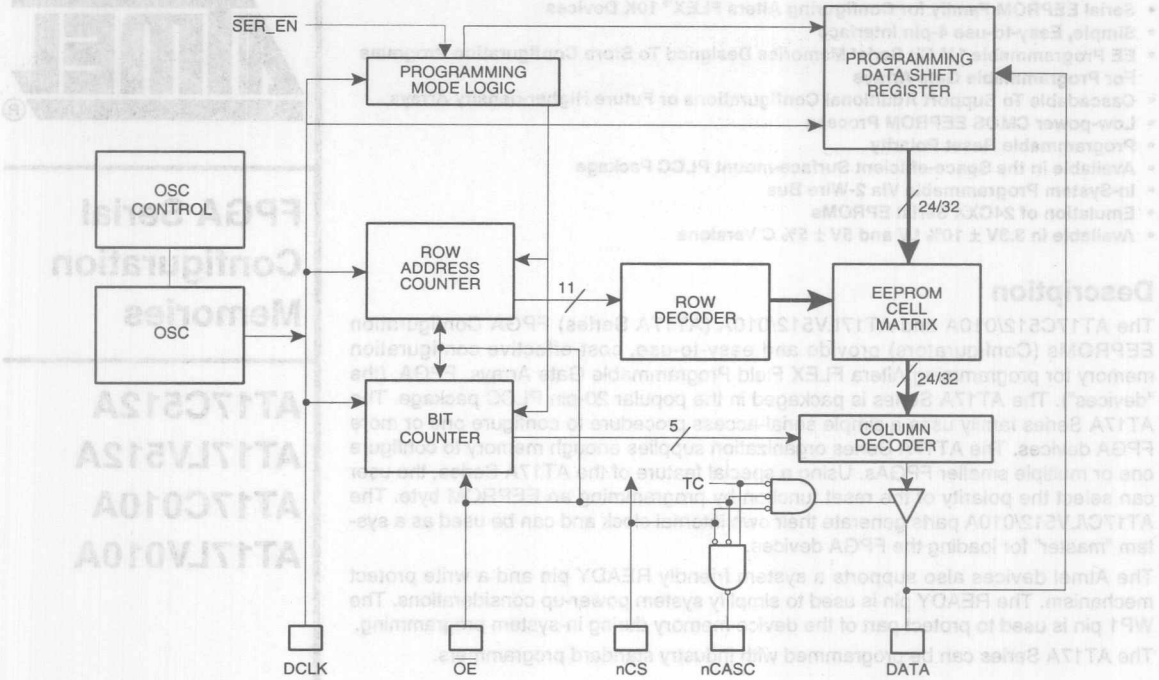
FPGA Serial Configuration Memories

AT17C512A
AT17LV512A
AT17C010A
AT17LV010A

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Block Diagram



Device Configuration

The control signals for configuration EEPROMs–nCS, OE, and DCLK–interface directly with the FPGA device control signals. All FPGA devices can control the entire configuration process and retrieve data from the configuration EEPROM without requiring an external intelligent controller.

The configuration EEPROM device's OE and nCS pins control the tri-state buffer on the DATA output pin and enable the address counter and the oscillator. When OE is driven low, the configuration EEPROM device resets the address counter and tri-states its DATA pin. The nCS pin controls the output of the AT17A Series. If nCS is held high after the OE reset pulse, the counter is disabled and the DATA output pin is tri-stated. When nCS is driven low, the counter and the DATA output pin are enabled. When OE is driven low again, the address counter is reset and the DATA output pin is tri-stated, regardless of the state of the nCS.

When the configurator has driven out all of its data and nCASC is driven low, the device tri-states the DATA pin to avoid contention with other configurators. Upon power-up, the address counter is automatically reset.

FPGA Device Configuration

FPGA devices can be configured with an AT17A Series EEPROM. The AT17A Series device stores configuration data in its EEPROM array and clocks the data out serially with its internal oscillator. The OE, nCS, and DCLK pins supply the control signals for the address counter and the output tri-state buffer. The AT17A Series device sends a serial bitstream of configuration data to its DATA pin, which is connected to the DATA0 input pin on the FPGA device.

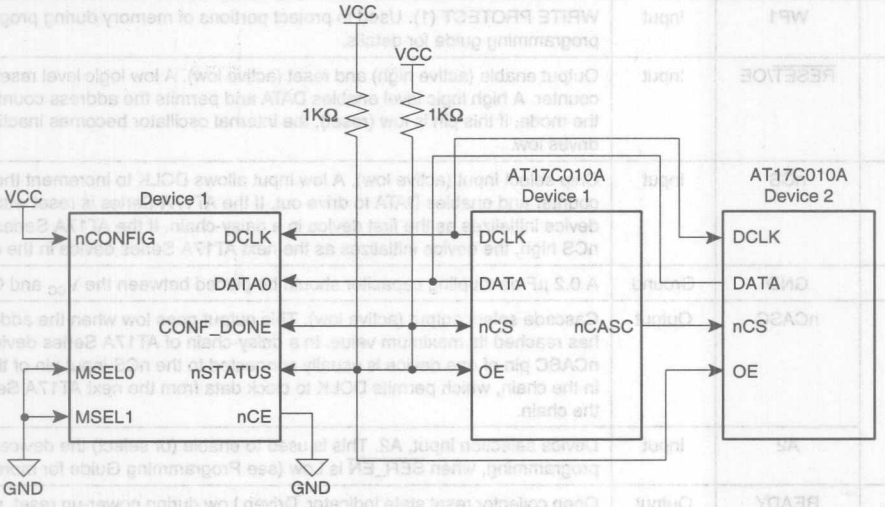
When configuration data for a FPGA device exceeds the capacity of a single AT17A Series device, multiple AT17A Series devices can be serially linked together. When multiple AT17A Series devices are required, the nCASC and nCS pins provide handshaking between the AT17A Series devices.

The position of an AT17A Series device in a chain determines its operation. The first AT17A Series device in a Configurator chain is powered up or reset with nCS low and is configured for FPGA devices protocol. This AT17A Series device supplies all clock pulses to one or more FPGA devices and to any downstream AT17A Series during configuration. The first AT17A Series device also provides the first stream of data to the FPGA devices during

multi-device configuration. Once the first AT17A Series device finishes sending configuration data, it drives its nCASC pin low, which drives the nCS pin of the second AT17A Series device low. This activates the second AT17A Series device to send configuration data to the FPGA device.

The first AT17A Series device clocks all subsequent AT17A Series devices until configuration is complete. Once all configuration data is transferred and nCS on the first AT17A Series device is driven high by CONF_DONE on the FPGA devices, the first AT17A Series device clocks 16 additional cycles to initialize the FPGA device. Then the first AT17A Series device goes into zero-power (idle) state. If nCS on the first AT17A Series device is driven high before all configuration data is transferred–or if the nCS is not driven high after all configuration data is transferred–the nSTATUS is driven low, indicating a configuration error.

Figure 1. FPGA Device Configured with Two AT17A Series Devices



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Pin Configurations

Pin Number (20-Pin PLCC)	Pin Name	Pin Type	Description
2	DATA	Output	Serial data output.
4	DCLK	I/O	Clock output or clock input. Rising edges on DCLK increment the internal address counter and present the next bit of data to the DATA pin. The counter is incremented only if the OE input is held high, the nCS input is held low, and all configuration data has not been transferred to the target device (otherwise, in FPGA 10K master mode, the DCLK pin drives low).
5	WP1	Input	WRITE PROTECT (1). Used to protect portions of memory during programming. See programming guide for details.
8	$\overline{\text{RESET}}$/OE	Input	Output enable (active high) and reset (active low). A low logic level resets the address counter. A high logic level enables DATA and permits the address counter to count. In the mode, if this pin is low (reset), the internal oscillator becomes inactive and DCLK drives low.
9	nCS	Input	Chip select input (active low). A low input allows DCLK to increment the address counter and enables DATA to drive out. If the AT17A Series is reset with nCS low, the device initializes as the first device in a daisy-chain. If the AT17A Series is reset with nCS high, the device initializes as the next AT17A Series device in the chain
10	GND	Ground	A 0.2 µF decoupling capacitor should be placed between the V_{CC} and GND pins.
12	nCASC	Output	Cascade select output (active low). This output goes low when the address counter has reached its maximum value. In a daisy-chain of AT17A Series devices, the nCASC pin of one device is usually connected to the nCS input pin of the next device in the chain, which permits DCLK to clock data from the next AT17A Series device in the chain.
	A2	Input	Device selection input, A2. This is used to enable (or select) the device during programming, when $\overline{\text{SER_EN}}$ is Low (see Programming Guide for more details)
15	READY	Output	Open collector reset state indicator. Driven Low during power-up reset, released when power-up is complete. (Recommend a 4.7KΩ Pull-up on this pin if used).
18	$\overline{\text{SER_EN}}$	Input	Serial enable is normally high during FPGA loading operations. Bringing SER_EN Low, enables the two wire serial interface mode for programming.
20	V_{CC}	Power	Power pin.

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-0.1V to V_{CC} + 0.5V
Supply Voltage (V_{CC})	-0.5V to +7.0V
Maximum Soldering Temp. (10 s @ 1/16 in.)	260°C
ESD (R_{ZAP} = 1.5K, C_{ZAP} = 100 pF)	2000V

*NOTICE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Operating Conditions

Symbol	Description		AT17CXXXA Min	AT17CXXXA Max	AT17LVXXXA Min	AT17LVXXXA Max	Units
V_{CC}	Commercial	Supply voltage relative to GND -0°C to +70°C	4.75	5.25	3.0	3.6	V
	Industrial	Supply voltage relative to GND -40°C to +85°C	4.5	5.5	3.0	3.6	V
	Military	Supply voltage relative to GND -55°C to +125°C	4.5	5.5	3.0	3.6	V

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DC Characteristics

V_{CC} = 5V ± 5% Commercial / 5V ± 10% Ind./Mil.

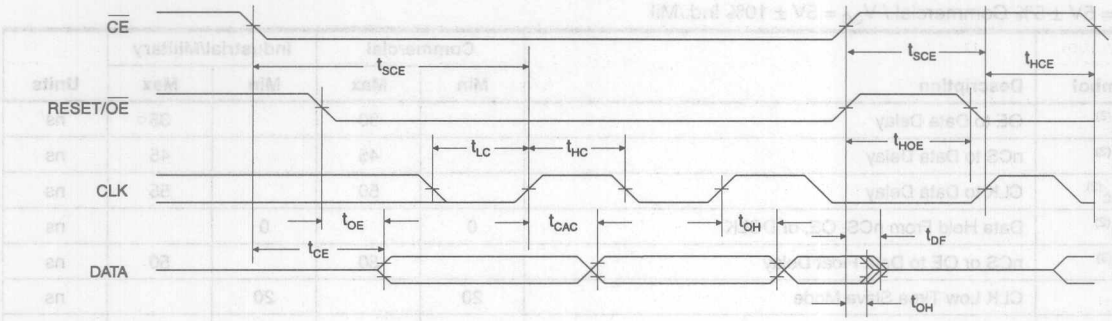
Symbol	Description		Min	Max	Units
V_{IH}	High-level input voltage		2.0	V_{CC}	V
V_{IL}	Low-level input voltage		0	0.8	V
V_{OH}	High-level output voltage (I_{OH} = -4 mA)	Commercial	3.7		V
V_{OL}	Low-level output voltage (I_{OL} = +4 mA)			0.32	V
V_{OH}	High-level output voltage (I_{OH} = -4 mA)	Industrial	3.6		V
V_{OL}	Low-level output voltage (I_{OL} = +4 mA)			0.37	V
V_{OH}	High-level output voltage (I_{OH} = -4 mA)	Military	3.5		V
V_{OL}	Low-level output voltage (I_{OL} = +4 mA)			0.4	V
I_{CCA}	Supply current, active mode			10	mA
I_L	Input or output leakage current (V_{IN} = V_{CC} or GND)		-10	10	µA
I_{CCS}	Supply current, standby mode AT17010A/512A	Commercial		150	µA
		Industrial/Military		150	µA

DC Characteristics

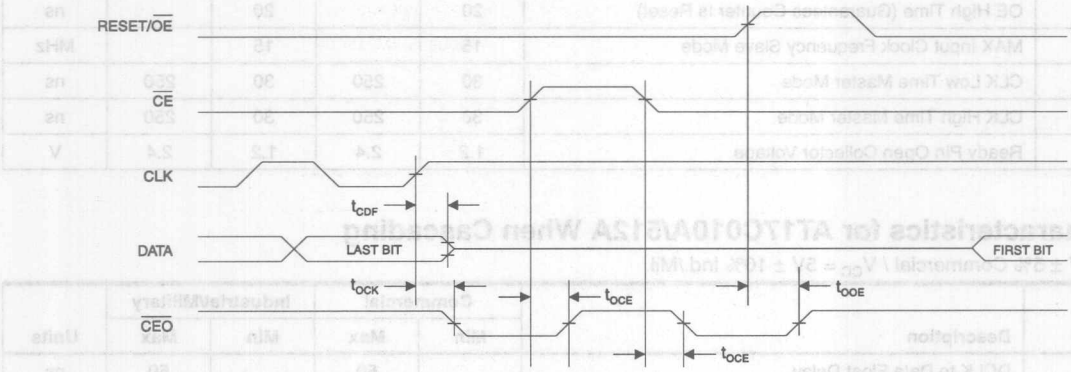
V_{CC} = 3.3V ± 10%

Symbol	Description		Min	Max	Units
V_{IH}	High-level input voltage		2.0	V_{CC}	V
V_{IL}	Low-level input voltage		0	0.8	V
V_{OH}	High-level output voltage (I_{OH} = -2.5 mA)	Commercial	2.4		V
V_{OL}	Low-level output voltage (I_{OL} = +3 mA)			0.4	V
V_{OH}	High-level output voltage (I_{OH} = -2 mA)	Industrial	2.4		V
V_{OL}	Low-level output voltage (I_{OL} = +3 mA)			0.4	V
V_{OH}	High-level output voltage (I_{OH} = -2 mA)	Military	2.4		V
V_{OL}	Low-level output voltage (I_{OL} = +2.5 mA)			0.4	V
I_{CCA}	Supply current, active mode			5	mA
I_L	Input or output leakage current (V_{IN} = V_{CC} or GND)		-10	10	µA
I_{CCS}	Supply current, standby mode	Commercial		50	µA
		Industrial/Military		50	µA

AC Characteristics



AC Characteristics When Cascading



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AC Characteristics for AT17C010A/512A

V_{CC} = 5V ± 5% Commercial / V_{CC} = 5V ± 10% Ind./Mil

Symbol	Description	Commercial		Industrial/Military		Units
		Min	Max	Min	Max	
T_{OE}[2]	OE to Data Delay		30		35	ns
T_{CE}[2]	nCS to Data Delay		45		45	ns
T_{CAC}[2]	CLK to Data Delay		50		55	ns
T_{OH}[2]	Data Hold From nCS, OE, or DCLK	0		0		ns
T_{DF}[3]	nCS or OE to Data Float Delay		50		50	ns
T_{LC}	CLK Low Time Slave Mode	20		20		ns
T_{HC}	CLK High Time Slave Mode	20		20		ns
T_{SCE}	nCS Setup Time to DCLK (to guarantee proper counting)	20		25		ns
T_{HCE}	nCS Hold Time to DCLK (to guarantee proper counting)	0		0		ns
T_{HOE}	OE High Time (Guarantees Counter Is Reset)	20		20		ns
F_{MAX}	MAX Input Clock Frequency Slave Mode	15		15		MHz
T_{LC}	CLK Low Time Master Mode	30	250	30	250	ns
T_{HC}	CLK High Time Master Mode	30	250	30	250	ns
V_{RDY}	Ready Pin Open Collector Voltage	1.2	2.4	1.2	2.4	V

AC Characteristics for AT17C010A/512A When Cascading

V_{CC} = 5V ± 5% Commercial / V_{CC} = 5V ± 10% Ind./Mil.

Symbol	Description	Commercial		Industrial/Military		Units
		Min	Max	Min	Max	
T_{CDF}[3]	DCLK to Data Float Delay		50		50	ns
T_{OCK}[2]	DCLK to nCASC Delay		35		40	ns
T_{OCE}[2]	CE to nCASC Delay		35		35	ns
T_{OOE}[2]	OE to nCASC Delay		30		30	ns

Notes: 1. Preliminary specifications for military operating range only.

2. AC test load = 50 pF.

3. Float delays are measured with 5 pF AC loads. Transition is measured ± 200 mV from steady state active levels.

AC Characteristics for AT17C010A/512A

V_{CC} = 3.3V ± 10% Commercial / V_{CC} = 3.3V ± 10% Ind./Mil

Symbol	Description	Commercial		Industrial/Military		Units
		Min	Max	Min	Max	
T_{OE}[2]	OE to Data Delay		50		55	ns
T_{CE}[2]	nCS to Data Delay		55		60	ns
T_{CAC}[2]	CLK to Data Delay		60		65	ns
T_{OH}[2]	Data Hold From nCS, OE, or DCLK	0		0		ns
T_{DF}[3]	nCS or OE to Data Float Delay		50		50	ns
T_{LC}	CLK Low Time Slave Mode	25		25		ns
T_{HC}	CLK High Time Slave Mode	25		25		ns
T_{SCE}	nCS Setup Time to DCLK (to guarantee proper counting)	35		40		ns
T_{HCE}	nCS Hold Time to DCLK (to guarantee proper counting)	0		0		ns
T_{HOE}	OE High Time (Guarantees Counter Is Reset)	20		20		ns
F_{MAX}[4]	MAX Input Clock Frequency Slave Mode	15		10		MHz
T_{LC}	CLK Low Time Master Mode	30	300	30	300	ns
T_{HC}	CLK High Time Master Mode	30	300	30	300	ns
V_{RDY}	Ready Pin Open Collector Voltage	1.2	2.4	1.2	2.4	V

AC Characteristics for AT17C010A/512A When Cascading

V_{CC} = 3.3V ± 10% Commercial / V_{CC} =3.3V ± 10% Ind./Mil.

Symbol	Description	Commercial		Industrial/Military		Units
		Min	Max	Min	Max	
T_{CDF}[3]	DCLK to Data Float Delay		50		50	ns
T_{OCK}[2]	DCLK to nCASC Delay		50		55	ns
T_{OCE}[2]	CE to nCASC Delay		35		40	ns
T_{OOE}[2]	OE to nCASC Delay		35		35	ns

Notes:
1. Preliminary specifications for military operating range only.
2. AC test load = 50 pF.
3. Float delays are measured with 5 pF AC loads. Transition is measured ± 200 mV from steady state active levels.
4. During cascade F_{MAX} = 12.5 MHz

Ordering Information - 5V Devices

Memory Size (K)	Ordering Code	Package	Operation Range
512K[1]	AT17C512A-10JC	20J	Commercial (0°C to 70°C)
	AT17C512A-10JI	20J	Industrial (-40°C to 85°C)
1M Bit[2]	AT17C010A-10JC	20J	Commercial (0°C to 70°C)
	AT17C010A-10JI	20J	Industrial (-40°C to 85°C)

Ordering Information - 3.3V Devices

Memory Size (K)	Ordering Code	Package	Operation Range
512K[1]	AT17LV512A-10JC	20J	Commercial (0°C to 70°C)
	AT17LV512A-10JI	20J	Industrial (-40°C to 85°C)
1M Bit[2]	AT17LV010A-10JC	20J	Commercial (0°C to 70°C)
	AT17LV010A-10JI	20J	Industrial (-40°C to 85°C)

Notes: 1. Use 512K density parts to replace Altera EPC1441.
2. Use 1M density parts to replace Altera EPC1

Package Type	
20J	20-Lead, Plastic J-Leaded Chip Carrier (PLCC)

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Parallel EEPROMs 3

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Atmel's Policy on Quality

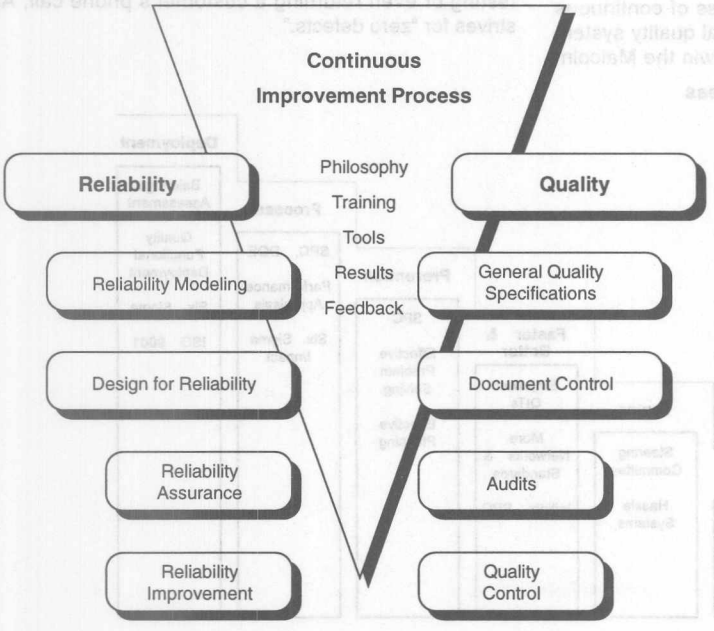
Application Note

Dedicated to Customer Satisfaction

It seems like such a simple request - *to get what you want, when you want it, and for a reasonable price.* However, in the complex world of integrated circuits, thousands of factors influence the design and manufacture of a part and can affect how the device will perform. At Atmel, every employee is committed to making sure the customer gets what he wants. From the executive level and throughout the organization, the Company's goal is one hundred percent customer satisfaction.

To achieve this goal, Atmel's employees have developed the philosophy, structure, training and tools necessary to sustain product quality and reliability. The result is two interrelated functions, one dedicated to quality and one dedicated to reliability. The "thread" that ties these functions to each other and to the rest of the Company is the Continuous Improvement Process.

Atmel's corporate philosophy of continuous improvement insures that you get not only high quality, reliable devices, but that every group within the Company is operating with your requirements in mind. Atmel's hall-mark is excellence: quality and reliability from its circuits and service from its employees.



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Rev. 0551C–10/98

ISO 9000 Certification

Certification to ISO 9001 and ISO 9002 for product design and Manufacturing Processes is just one example of how Atmel strives to meet the needs of its customers around the world.

Certification is not easy and it is the result of an ever-present commitment to quality, reliability, and continuous improvement.

Atmel's commitment to ISO 9000 extends to our major contractors and distributors as well. Most are ISO 9000 certified. Atmel is continuing to work with others to become certified.

Continuous Improvement

Accepting the Malcolm Baldrige National Quality Award, one recipient said that "we are in a race without a finish line." That is a good synopsis of Atmel's philosophy of continuous improvement. The key responsibility of the executives, managers and employees of Atmel is to constantly and forever improve the quality of products and services delivered.

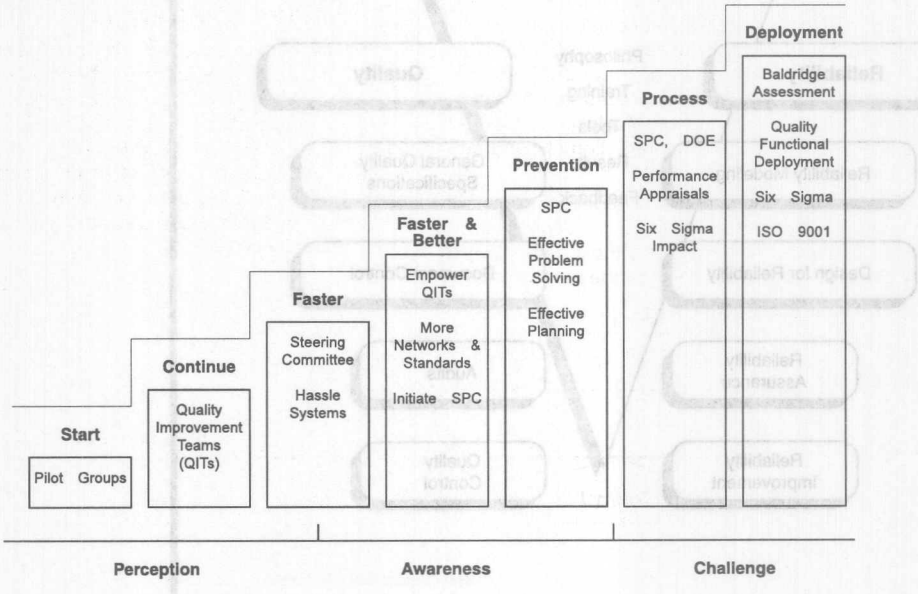
The Company's objectives include providing the leadership and training required to sustain a process of continuous quality improvement; implementing a total quality system that will allow Atmel to compete for and win the Malcolm Baldrige National Quality Award; implementing and utilizing SPC throughout the organization; and understanding and integrating the concepts of "six sigma" into the culture and processes.

In the past, the organization has gone through formal training in the Crosby 14-Step Quality Program; the Alamo Problem Solving, Planning and Decision Making Program; General Quality Specifications; Statistical Process Control (SPC); Statistical Design of Experiments (DOE); and in-house training for managerial and supervision skills.

Today, training continues with an emphasis on SPC, DOE, six sigma concepts and team building. The figure below represents the steps Atmel has already taken along the journey of continuous improvement. Each year, new organizational goals and functional strategies elevate the Company's level of quality even higher.

In addition to training, the journey of continuous improvement involves integrating SPC, DOE, just-in-time (JIT) and other techniques into everyday operations. Use of these techniques throughout the corporation, not just in manufacturing, is proof of Atmel's commitment to continuous improvement. Whether it is order entry, wafer fabrication, review of customer specifications, government compliance testing or even returning a customer's phone call, Atmel strives for "zero defects."

Atmel's Continuous Improvement Process



Statistical Process Control

Control of process parameters is the heart of Atmel's continuous improvement system. SPC involves the portrayal of process parametric values in a graphical form to display whether an operation is in control or out of control. Through experimentation and evaluation, upper and lower control limits are established for each parametric value of a given process step. The parametric values are charted on a continual basis and the result is an easy-to-interpret graph which allows for immediate corrections or adjustments by the person closest to the operation. This type of quality measurement can be applied to almost any operation within the Company.

Currently over 500 SPC charts are monitored throughout wafer fabrication, test and packaging operations. Used at crucial points in the fabrication process, SPC insures compliance with pre-set control limits. Measurements taken at critical steps in the process are used in the development of engineering models and applied to current design. Process SPC data is monitored to insure the integrity of each wafer and the resulting statistics are used to constantly improve the process.

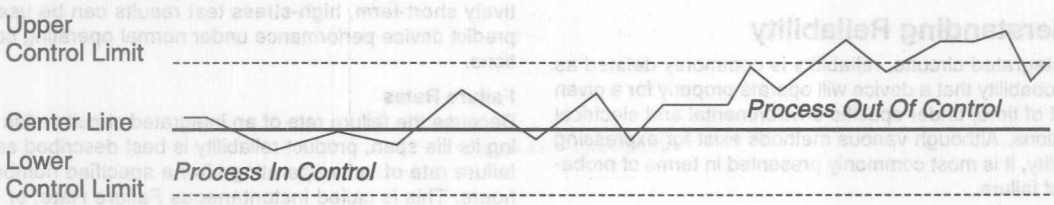
Statistical Design of Experiments (DOE)

The DOE technique has been successfully used for many years by the agriculture and chemical industries. Only recently has the technique been used in high-technology industries.

Using DOE, various problems can be solved simultaneously by determining variables that are statistically significant, interaction between variables and the amount of variation possible in the process or product. DOE can greatly reduce the time required for process qualification and optimization. This is especially useful in wafer fabrication where quality depends on the interaction of hundreds of different process steps and materials.

When DOE is coupled with computer-aided design and process models, it can be used to predict relationships and outcomes by running experiments. Actual experiments are run on only those processes which show the most promise. This, in turn, reduces the time and cost of designing new products and processes or improving existing ones.

Example of a Process Control Chart



Just-in-time

The concept of receiving products exactly when they are needed for the system is what JIT is all about. In order for this technique to succeed, however, a significant commitment is made by both the supplier and the customer. JIT implies a partnership that gives the customer quality devices, reliable deliveries and lower costs compared with carrying inventory. Atmel performs design and fabrication tasks with such predictability that circuits may go directly to the customer's work floor, eliminating incoming inspection.

The Payoff

Quality and reliability at Atmel cannot be separated from the life cycle of the product. The Company recognizes that quality and reliability must be maintained at all levels of the organization and must be constantly improved. Through continuous improvement and a focus on customer requirements, Atmel has established dock-to-stock programs with several high-performance computer and military system companies.

The bottom line for Atmel customers is lower system life-cycle cost and faster time-to-market. Atmel's culture puts customer requirements and continuous improvement above all else, insuring that indeed you get what you want, when you want it, and at a reasonable price.

Atmel's Quality System

The foundation of Atmel's quality system is ISO-9001 and MIL-STD-883. These specifications are translated into company policies covering all areas of design, qualification, manufacturing and customer service. Atmel has chosen to operate to the high standards of the military in order to meet or exceed the needs of commercial and industrial customers. The Company's employees are trained, certified and audited on these policies, which are outlined in Atmel's Quality Manual.

Quality Control

Atmel's quality efforts focus on the customer and their system. For example, through strict attention to customers' component and system requirements Atmel has achieved preferred supplier status. To attain this level of customer confidence the Company demonstrates a commitment to quality control in all areas of the operation. This includes purchase control, in-process quality control, and statistical quality control.

Purchase Control

Every manufacturing process relies on its raw materials, and incoming inspection plays a vital role in the quality of those raw materials. At Atmel, incoming inspection is supplemented by supplier audits, historical review of supplier quality and insistence that suppliers use SPC.

In-process Quality Control

Once raw materials are controlled, the processes that transform them into a final product must also be controlled. This is done through inspection of product at critical, interim stages of manufacturing. Also included is the auditing of personnel and operations to insure that the proper procedures are being followed.

Statistical Quality Control

Immediate action is taken by the manufacturing organization when discrepancies are found during an inspection. At Atmel, a typical discrepancy results in permanent corrective action.

However, another vital function of quality control is the reporting of longer-term trends and statistics based upon individual control functions. Statistical quality control can be used to highlight increases in defects or errors in a department, for example. Atmel uses this information to take preventative action when a negative trend is detected.

Audits

Atmel maintains a self-audit group that continually monitors compliance to internal procedures and to customer specifications. The findings of this group are routinely reported to management to insure that adequate corrective actions are taken for any deficiencies.

Understanding Reliability

For integrated circuits, reliability is commonly defined as the probability that a device will operate properly for a given period of time, under specific environmental and electrical conditions. Although various methods exist for expressing reliability, it is most commonly presented in terms of probability of failure.

Reliability Modeling

Applying test data to general failure distribution curves, such as Weibull or lognormal curves, requires that the data fit the distribution and that the model is physically and mathematically reasonable with respect to the failure mechanism. Developing an accurate reliability model requires consideration of non-test-related failures as well as unidentified failure mechanisms. Atmel's reliability program is built on an understanding of the assumptions and restrictions inherent in practical reliability testing.

Design for Reliability

Many reliability concerns can be minimized with proper design techniques. For example ESD, which contributes to production yield loss and is a potential reliability problem, can be reduced or eliminated through the establishment of adequate design rules. Atmel's reliability assurance systems insure that data taken from actual product testing is fed back to design groups for verification of models and design rule updates.

Reliability Assurance Concepts

Accelerated Testing

During its life cycle, an integrated circuit passes through three distinct phases which are best defined by the failure rate of the device. In order to determine the actual interval associated with each phase, a significant number of cumulative failures (usually 50 percent) must be observed. Due to the dramatically small failure rates of integrated circuits, testing under normal operating conditions provides little or no useful data for forecasting reliability. An alternative is to increase stress levels above normal, thereby accelerating the development of failure mechanisms over time. Determining proper stress conditions that lead to realistic failures (those that could occur under normal conditions) without introducing unwanted mechanisms is a primary concern of the Reliability Engineer.

Atmel's Reliability group uses a variety of tests designed to accelerate specific failures and reduce the probability of spurious results. Variables such as temperature, voltage, currents, humidity and radiation can be controlled during testing to influence operational parameters of the device. Stress also can be selectively increased to affect specific circuit elements. To quantify the degree of failure acceleration due to increased stress, the industry has developed a number of physical models. By utilizing these models, relatively short-term, high-stress test results can be used to predict device performance under normal operating conditions.

Failure Rates

Because the failure rate of an integrated circuit varies during its life span, product reliability is best described as the failure rate of units operating after a specified number of hours. This is called Instantaneous Failure Rate, or IFR. Other measures include Average Failure Rate, the average of the IFR over a period of time, and Cumulative Failure Rate, the total number of failures occurring during operation. Because the integrated circuit failure rates are remark-

ably low, they are normally measured with respect to billions of device hours. This value, referred to as a FIT, is defined as failures per one billion hours of device operation.

Failure Mechanisms

Integrated circuit failure mechanisms can be classified as either process anomalies or wear-out mechanisms. Process anomalies result from less than ideal process conditions and include product defects such as contamination, step coverage deficiencies and electrostatic discharge (ESD) damage. Often termed "quality" problems, these mechanisms are normally detected through process screens such as visual inspection, thermal cycling and burn-in. Process anomalies that escape manufacturing screens often accelerate or encourage wear-out mechanisms. For example, ESD can weaken insulating oxides or thin metallization allowing dielectric breakdown or electromigration failures to occur earlier in the life cycle.

Wear-out mechanisms are directly related to the useful life of device materials, their physical properties, and interactions occurring at material interfaces. Because wear-out mechanisms result from intrinsic physical properties of the materials, reducing these failures requires attention at the design level, strict control of process variation, and use of high quality materials and composites.

Of the failure mechanisms studied by Reliability, electromigration, time-dependent dielectric breakdown and latch-up are the primary concerns.

ELECTROMIGRATION: One of the more studied problems in integrated circuit design and production is electromigration. Devices utilizing aluminum conductors are most susceptible to the phenomena. Electrons flowing in the conductor effectively collide with aluminum atoms, pushing them away and eventually forming an open circuit. Design, wafer process control, metal composition, temperature and current density determine how long a device will operate before electromigration results in a failure. Atmel's experimental electromigration models and associated research have resulted in design and production techniques which decrease this risk. One such technique adds a small quantity of copper to the aluminum. This greatly enhances the current carrying capability of the metal, reducing the occurrence of electromigration.

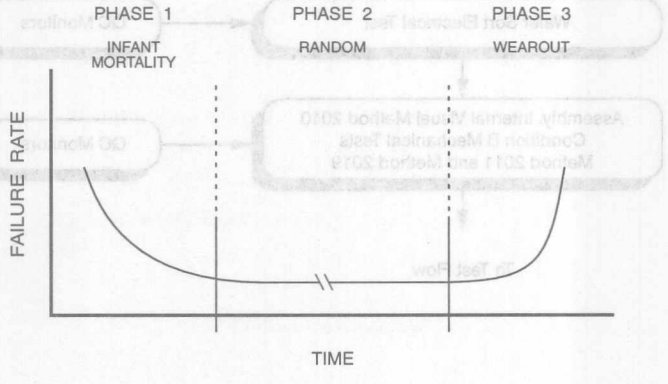
TIME-DEPENDENT DIELECTRIC BREAKDOWN: Reduced dielectric strength in MOS capacitors is caused by the accumulation of electric charge in a gate oxide, which limits the operational life of the device. Experiments performed on CMOS and Bipolar Enhanced MOS (BEMOS) devices indicate that Atmel's dielectrics and related processes provide excellent resistance to long-term degradation and failure, even at the high voltage levels typical in non-digital circuit applications.

LATCH-UP: Latch-up in a CMOS device allows extremely high current to flow, often resulting in open circuit traces or bond wires. The condition can occur in any PNPN structure. Proper design and Atmel's proprietary process have eliminated this problem before it occurs.

The Bathtub Curve

The traditional "bathtub" curve used to describe the failure rate of a product is actually a combination of two exponential failure rate models. The first model begins with a high failure rate and rapidly declines to a low, nearly constant level. This model describes the early-life reliability of an integrated circuit. Atmel's incoming material inspection, production test and process controls identify and remove potential phase one failures before they are shipped to a customer. Test and screening limits have been established through characterization and qualification of the processes used in fabrication. DOE and SPC are used to maintain process stability and repeatability throughout design, product development and production.

Reliability Life (Bathtub) Curve



The second model that makes up the "bathtub curve" starts with a low, relatively constant failure rate and climbs exponentially after some period of time. This is the phase three wear-out stage where mechanisms such as electromigration and oxide breakdown predominate. Through rigorous analysis of phase three failures, Atmel has developed techniques to optimize material life. The result is a forestalled phase three period and consequently, an increased phase two period.

By combining these two models, a bathtub-shaped curve representing the lifetime of the product is formed. The nearly flat portion of the curve is the result of a mathematical summation of the "tails" of the two models and represents phase two. A low, stable failure rate is characteristic of this stage as failures observed during this period are random in nature. These random failures are usually the result of sudden exposure to over-stress conditions or rare occurrences of wear-out type mechanisms. Devices shipped to the customer are in this stable portion of their lifetime.

Manufacturing for Quality and Reliability

All ceramic Atmel products are manufactured to the standards of Military Standard 883D, Class B through wafer fabrication and assembly as shown in Figure 1. The products then follow different test flows that correspond to the different classes of products that Atmel offers.

1. Commercial Grade. This product follows Test Flow (1), Figure 2 and is guaranteed over the temperature range of 0°C to +70°C.
2. Industrial Grade. This product follows Test Flow (2), Figure 3 and is guaranteed over the temperature range of -40°C to +85°C.
3. Quality Enhancement Flow. This product follows Test Flow (3), Figure 4 which specifies burn-in of industrial product in a standard flow.
4. Military Grade. Three classes of military products are offered by Atmel (MIL-STD-883D, Class B standard product, Standard Military Drawing (SMD) product, and Source Control Drawing (SCD) product). The Military Section discusses test procedures for these products in detail.

The Payoff

The focus of Atmel's quality and reliability efforts is the customer and his system. The common goals of highest field reliability and lowest system life cycle cost are achieved through close working relationships using programs such as "ship to stock", "just in time", and "failure trend analysis". Under these programs incoming Atmel circuits go straight to the customers' workfloors—they do not go through an incoming inspection cycle. This, of course, lowers manufacturing costs and is a testimony of the trust that has been established. In addition, long term field failures are analyzed so that corrective action plans can be implemented. Atmel has developed programs such as these with many major customers.

Figure 1. MIL-STD-883D, Class B, Product Flow.
All ceramic Atmel products are manufactured to these standards.

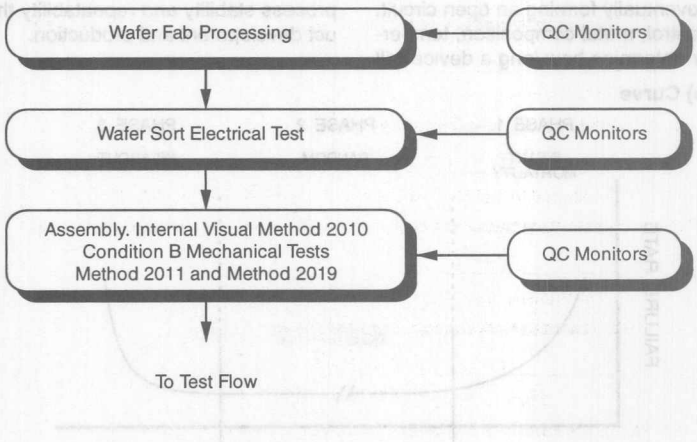


Figure 2. Test Flow (1), Commercial Grade Test Flow.

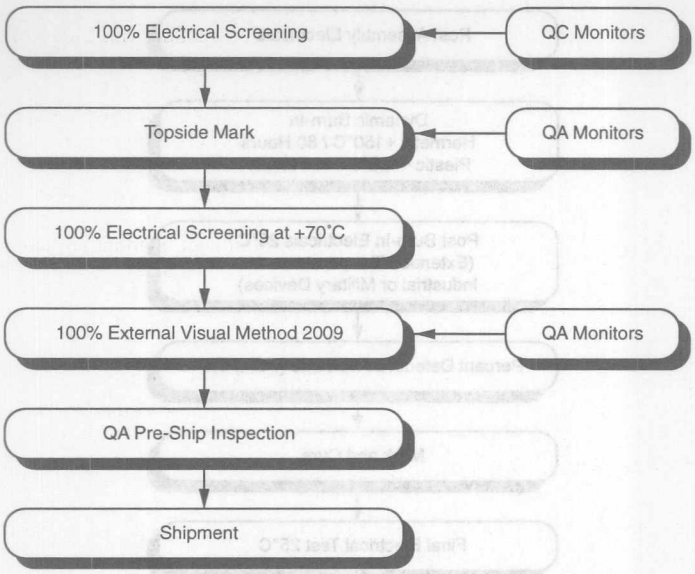


Figure 3. Test Flow (2), Industrial Grade Test Flow.

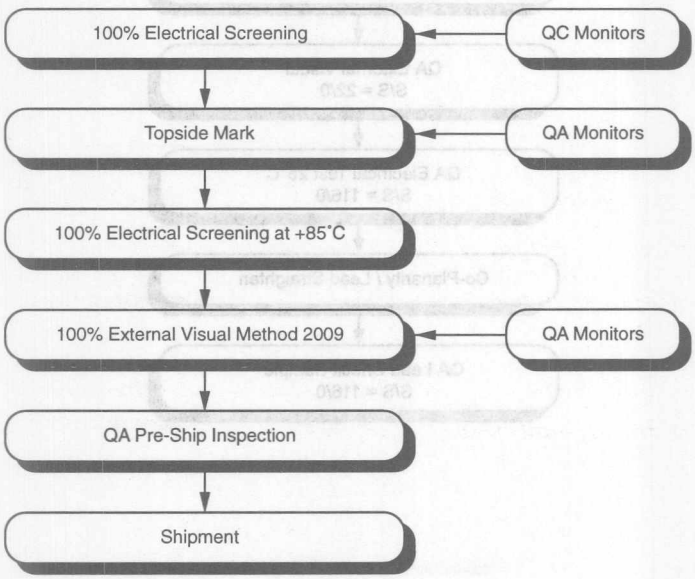
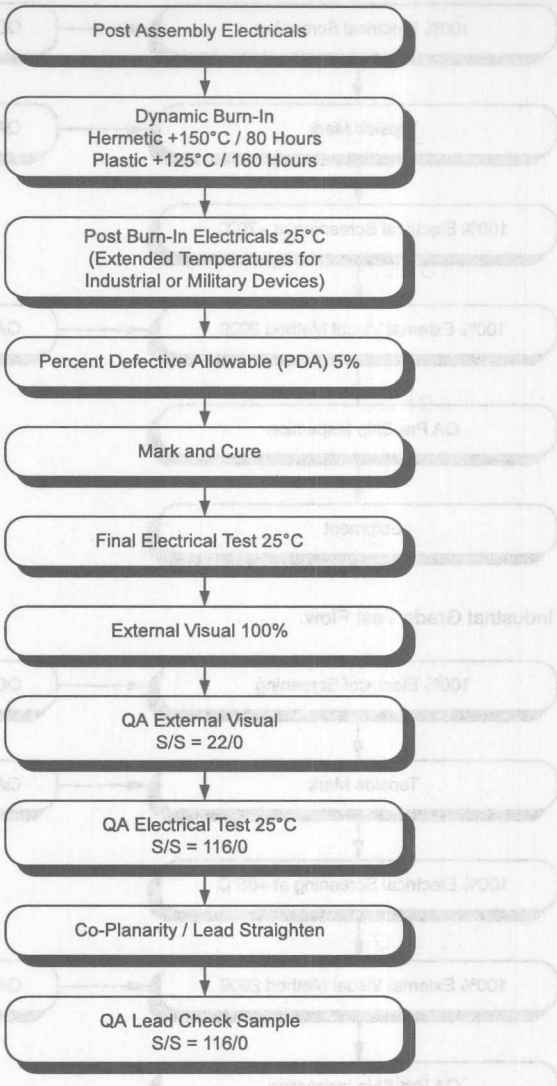


Figure 4. Test Flow (3), Quality Enhancement Flow (-9).



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Atmel is committed to producing products to the highest quality standards achievable through the constant use of Statistical Process Control techniques and a very active Continuous Improvement System. These systems influence the entire product life cycle from the initial product definition, through the subsequent product design and fabrication process, to the final test procedures.

Assembly and Screening

Without regard for the products' final end use all wafers produced by Atmel are fabricated with the assumption that they are destined for high reliability applications in the military marketplace. After fabrication, products directed towards use by the military will enter into special flows, beginning with the assembly operation, that will insure full compliance for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices."

Figure 1 and 2 illustrate the standard flow for military products. It conforms to the requirements set forth in MIL-STD-883 method 5504.

Quality Conformance Inspection

As shown in Table 1, Atmel performs all the quality conformance inspections specified by MIL-STD-883 method 5005 for class B products. This testing includes Groups A and B on each individual inspection lot and Groups C and D on a periodic basis as defined in MIL-I-38535, Appendix A.

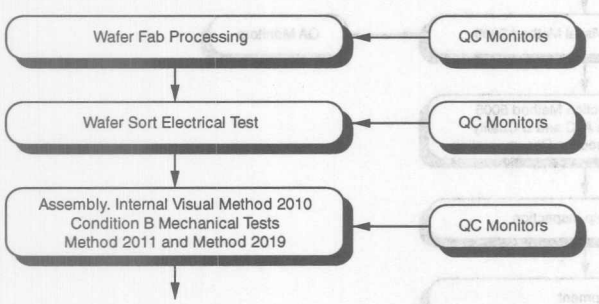
Lot specific Group A, Group B and preconditioning data and generic Group C and Group D data are available for customer procurement.

Military Product Programs

Atmel offers three programs for the procurement of military products:

(1) MIL-STD-883, Class B Program
Products procured to Atmel's MIL-STD-883 program are fully compliant with MIL-STD-883 paragraph 1.2.1, with no exceptions. These products are categorized as Atmel standard "883" products and may be procured by specifying the Atmel part number appended with the suffix /883. A Certificate of Compliance (C of C) is enclosed with each shipment. Refer to the product's data sheet for specific ordering information.

Figure 1. MIL-STD-883, Class B, Product Flow.
All Atmel products are manufactured to these standards.



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(2) Standard Microcircuit Drawing (SMD) Program
Products procured to the Standard Microcircuit Drawing are class B products fully compliant with MIL-STD-883 paragraph 1.2.1. In addition, these products are in full compliance with the applicable Standard Microcircuit Drawing. Atmel's test philosophy is to screen and test both Atmel Standard /883 products and products ordered by the SMD number identically.

Section 2, Table 1 lists currently approved Atmel SMD parts, organized by their Atmel part number. Section 2, Table 2 lists currently approved Atmel SMD parts, organized by their SMD number.

(3) Source Control Drawing (SCD) Program
Program procured to a source control drawing are class B products fully compliant with MIL-STD-883 paragraph 1.2.1 with optional additional tests as specified by the customer drawing. Atmel must review and accept a customer's SCD prior to order acceptance to assure compliance.

Figure 2. Test Flow (3), MIL-STD-883, Class B, SMD and SCD Test Flow.

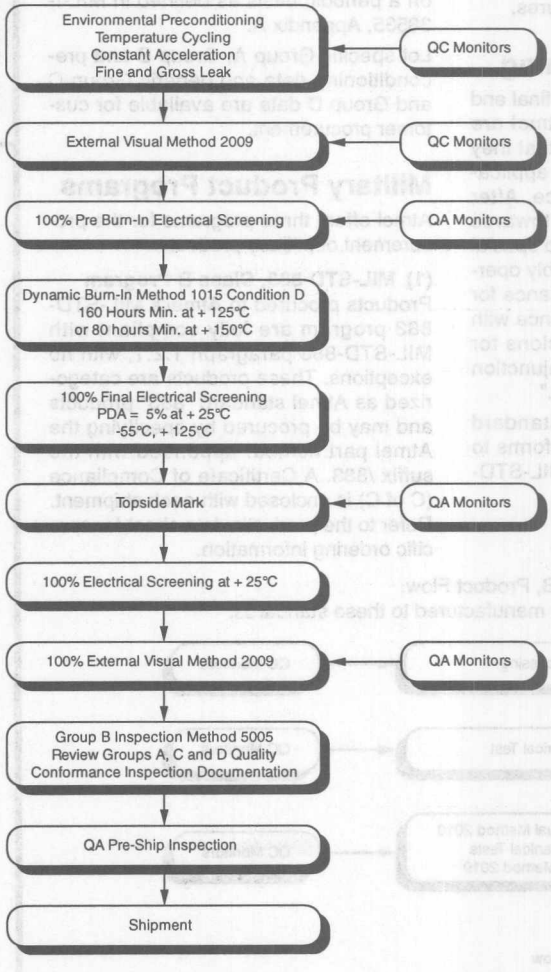


Table 1. Quality Conformance Inspections, Method 5005

Group A: Electrical Tests

Performed On Each Lot

Screen	MIL-STD-883 Table 1 Subgroups	LTPD
Static Tests at +25°C	1	2
Static Tests at +125°C	2	2
Static Tests at -55°C	3	2
Dynamic Tests at +25°C	4	2
Function Tests at +25°C	7	2
Function Tests at +125°C	8A	2
Function Tests at -55°C	8B	2
Switching Tests at +25°C	9	2
Switching Tests at +125°C	10	2
Switching Tests at -55°C	11	2

Group B: Assembly Integrity Tests

Performed On Each Lot

Screen	MIL-STD-883 Test Method	Conditions	Quantity (Accept No. or LTPD)
SUBGROUP 2			
Resistance to Solvents	2015	Top and Bottom Marks	4(0)
SUBGROUP 3			
Solderability	2003	+245°C +/-5°C	10
SUBGROUP 5			
Bond Strength	2011	Condition D	15

Group C: Die Related Tests

Screen	MIL-STD-883 Test Method	Conditions	LTPD
SUBGROUP 1			
Steady State Life Test	1005	Condition D	5
End Point Electricals	5005	As specified in the applicable device specification	
Physical Dimensions	2016	MIL-M-38510, Appendix C	15

Group D: Package Related Tests

By Package Type, Assembly Location, and Exterior Lead Finish

Screen	MIL-STD-883 Test Method	Conditions	Quantity (Accept No. or LTPD)
SUBGROUP 1			15
Physical Dimensions	2016	MIL-M-38510, Appendix C	
SUBGROUP 2			5
Lead Integrity	2004	Condition B2 (Condition D for LCC)	
Seal: Fine	1014	Condition A or B	
Seal: Gross	1014	Condition C	
SUBGROUP 3			15
Thermal Shock	1011	Condition B, 15 Cycles	
Temperature Cycling	1010	Condition C, 100 Cycles	
Moisture Resistance	1004	10 Cycles	
End Point Electricals	5005	As specified in the applicable device specification (within 42 hrs)	
Seal: Fine	1014	Condition A or B	
Seal: Gross	1014	Condition C	
Visual Examination		Per Visual of Method 1004 and 1010	
SUBGROUP 4			15
Mechanical Shock	2002	Condition B	
Vibration Variable Freq.	2007	Condition A	
Constant Acceleration	2001	Condition E, 30 KG., Y1	
Seal: Fine	1014	Condition A or B	
Seal: Gross	1014	Condition C	
Visual Examination	1010		
End Point Electricals	5005	As specified in the applicable device specification	
SUBGROUP 5			15
Salt Atmosphere	1009	Condition A	
Seal: Fine	1014	Condition A or B	
Seal: Gross	1014	Condition C	
Visual Examination		Per Visual of Method 1009	
SUBGROUP 6			3 (0) or 5 (1)
Internal Water Vapor Content	1018	5,000 PPM Maximum Water Content at 100°C	
SUBGROUP 7			15
Adhesion of Lead Finish	2025	Glass Frit Seal Only (LTPD for Number of Leads)	
SUBGROUP 8			5 (0)
Lid Torque	2024	Glass Frit Seal Only	

Standard Microcircuit Drawing Product Offering

SMD Products

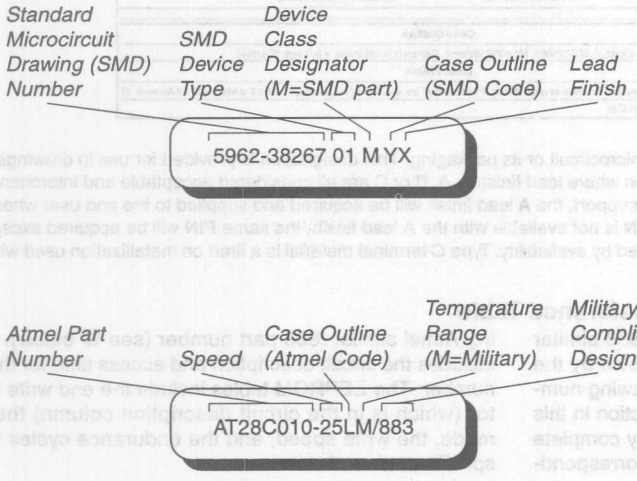
Introduction to the SMD Product Listing

Each Standard Microcircuit Drawing (SMD) part number that Atmel supplies corresponds to an Atmel /883 part number. SMD products are compliant to MIL-STD-883, paragraph 1.2.1 and to the requirements of the applicable standard microcircuit drawing. The tables in this section list the currently approved Atmel SMD parts by Atmel part number (Table 1) and by SMD part number (Table 2). They define and cross reference the Atmel /883 part number with the SMD part number for your ordering convenience.

Figure 1 shows how an Atmel SMD order number defines a part, compared to the components of the Atmel similar part number.

Please note that some SMD part numbers contain the letter "M" between the device type and the case outline designator. The "M" is part of the one part-one number system, set up by DESC. It is a device class designator which indicates the part is an SMD part number as opposed to being a JAN part number.

Figure 1. Components of an SMD number (top) compared to the Atmel similar part number (bottom).



How to Use the Atmel Part Type Reference Table

The organization of Table 1 enables the purchaser to order a standardized military part by using the Atmel generic part type to locate the correct SMD drawing number. The SMD part number is the order number for SMD devices. The Atmel generic part type, which begins with the prefix "AT," heads Table 1. There are four sections in this table (see sample table below):

SMD Options

The first section lists the SMD options available at Atmel. It includes the industry generic part type, the SMD drawing number, and the SMD device type. The SMD case outline options, the lead finish options, the circuit description, and the access time that correspond to that device type are also included. The tables for the EEPROM in this section include the end write indicator in the circuit description column and the write mode for the specific device type.

Order Code Cross-Reference

The next section of the table cross-references each optionally complete SMD part number (see ❶ below) with the Atmel similar /883 part number (see ❷ below).

Case Outline Legend

The third section gives the SMD case outline options available for the device.

Lead Finish Legend

The last section lists the SMD lead finish options available for the device.

SMD Options with Part Description and Specifications

AT28C64B

Generic Number	Standard Microcircuit Drawing Number				Description				
28C64B	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description End Write Indicator	Write Mode	Access Time (ns)	Write Speed (ms)	Endurance (Cycles)
	5962-87514	08	X	X, A	8K x 8 E^{2}PROM Data Polling	Byte/Page	250	10	10K
	5962-87514	09	X	X, A	8K x 8 E^{2}PROM Data Polling	Byte/Page	200	10	10K

Order Code Cross-Reference

Atmel Cage No. 1 FN41	Example: Atmel Order Number	Atmel Similar Part Number
	❶ 5962-87514 08 XX	❷ AT28C64B-25DM/883
	5962-87514 09 XX	AT28C64B-20DM/883

Case Outline Legend

Case Outline	
X	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)

Lead Finish Legend

Lead Finish	
X	Denotes no preference in lead finish; Finish A will be supplied (per paragraph 30.6.2.7 of MIL-I-38535B Appendix A)
A	Hot Solder Dip

Note: Finish letter "X" shall not be marked on the microcircuit or its packaging. This designation is provided for use in drawings, part lists, purchase orders, or other documentation where lead finishes A, B or C are all considered acceptable and interchangeable without preference. For Government logistic support, the A lead finish will be acquired and supplied to the end user when the X is included in the PIN for lead finish. If the PIN is not available with the A lead finish, the same PIN will be acquired except with the B or C lead finish designator as determined by availability. Type C terminal material is a fired on metallization used with leadless chip carriers.

How to Use the Atmel SMD Number Reference Table

Table 2 allows quick reference to the Atmel /883 similar part number when the SMD part number is known by the purchaser. The head for Table 2 is the SMD drawing number (see the example table below). The only section in this table is a cross-reference between the optionally complete SMD drawing number (see ❶ below) and the corresponding Atmel similar /883 part number (see ❷ below). It also includes the circuit description and access time for that part number. The EEPROM tables include the end write indicator (which is in the circuit description column) the write mode, the write speed, and the endurance cycles for the specific part number.

Order Codes | Part Description and Specifications

5962-87514

Order Code Cross-Reference

❶ Atmel Order Number	❷ Atmel Similar Part Number	Circuit Description End Write Indicator	Write Mode	Access Time (ns)	Write Spd. (ms)	Endur. (Cycles)
5962-87514 08 XX	AT28C64B-25DM/883	8K x 8 E^{2}PROM Data Polling	Byte/Page	250	10	10K
5962-87514 09 XX	AT28C64B-20DM/883	8K x 8 E^{2}PROM Data Polling	Byte/Page	200	10	10K
5962-87514 10 XX	AT28HC64B-12DM/883	8K x 8 E^{2}PROM Data Polling	Byte/Page	120	2	10K

Table 1. Atmel SMD Part Types, Listed by Atmel Part Number

AT28C64									
Generic Number	**Standard Microcircuit Drawing Number**				**Description**				
28C64	**Drawing Number**	**Device Type**	**Case Outline**	**Lead Finish**	**Circuit Description End Write Indicator**	**Write Mode**	**Access Time (ns)**	**Write Speed (ms)**	**Endurance (Cycles)**
	5962-87514	13	X, Y, Z	X, A	8K x 8 EEPROM Rdy/$\overline{\text{Busy}}$	Byte	350	1	10K
	5962-87514	14	X, Y	X, A	8K x 8 EEPROM Rdy/$\overline{\text{Busy}}$	Byte	300	1	10K
	5962-87514	15	X, Y, Z	X, A	8K x 8 EEPROM Rdy/$\overline{\text{Busy}}$	Byte	250	1	10K
	5962-87514	16	X, Y	X, A	8K x 8 EEPROM Rdy/$\overline{\text{Busy}}$	Byte	200	1	10K
	5962-87514	17	X, Y	X, A	8K x 8 EEPROM Rdy/$\overline{\text{Busy}}$	Byte	150	1	10K
	Example:Atmel Order Number				**Atmel Similar Part Number**				
	5962-87514 **13 XX**				AT28C64-35DM/883				
	5962-87514 **13 YX**				AT28C64-35LM/883				
	5962-87514 **13 ZX**				AT28C64-35FM/883				
	5962-87514 **14 XX**				AT28C64-30DM/883				
	5962-87514 **14 YX**				AT28C64-30LM/883				
	5962-87514 **15 XX**				AT28C64-25DM/883				
	5962-87514 **15 YX**				AT28C64-25LM/883				
	5962-87514 **15 ZX**				AT28C64-25FM/883				
	5962-87514 **16 XX**				AT28C64-20DM/883				
	5962-87514 **16 YX**				AT28C64-20LM/883				
	5962-87514 **17 XX**				AT28C64-15DM/883				
Atmel Cage No. 1FN41	5962-87514 **17 YX**				AT28C64-15LM/883				

Case Outline	
X	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
Y	32L, 32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
Z	28F, 28 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)
Lead Finish	
X	Denotes no preference in lead finish; Finish A will be supplied (per paragraph 30.6.2.7 of MIL-I-38535B Appendix A)
A	Hot Solder Dip

Note: New designs to use AT28C256 product SMD 5962-88525.

Table 1. Atmel SMD Part Types, Listed by Atmel Part Number

AT28C64F									
Generic Number	**Standard Microcircuit Drawing Number**				**Description**				
28C64F	**Drawing Number**	**Device Type**	**Case Outline**	**Lead Finish**	**Circuit Description End Write Indicator**	**Write Mode**	**Access Time (ns)**	**Write Speed (ms)**	**Endurance (Cycles)**
	5962-87514	28	X, Y, Z	X, A	8K x 8 EEPROM Rdy/Busy	Byte	200	0.2	10K
Atmel Cage No. 1FN41	**Example: Atmel Order Number**				**Atmel Similar Part Number**				
	5962-87514 **28 XX**				AT28C64F-20DM/883				
	5962-87514 **28 YX**				AT28C64F-20LM/883				
	5962-87514 **28 ZX**				AT28C64F-20FM/883				
Case Outline									
X	28D6 28 Lead 0.600" Wide Non-Windowed Ceramic Dual Inline Package (Cerdip)								
Y	32L 32 Pad Non-Windowed Ceramic Leadless Chip Carrier (LCC)								
Z	28F 28 Lead Non-Windowed Ceramic Bottom-Brazed Flat Package (Flatpack)								
Lead Finish									
X	Denotes no preference in lead finish; Finish A will be supplied (per paragraph 30.6.2.7 of MIL-I-38535B Appendix A)								
A	Hot Solder Dip								

Note: New designs to use AT28C256 product SMD 5962-88525.

Table 1. Atmel SMD Part Types, Listed by Atmel Part Number

AT28C64X									
Generic Number	**Standard Microcircuit Drawing Number**				**Description**				
28C64X	**Drawing Number**	**Device Type**	**Case Outline**	**Lead Finish**	**Circuit Description End Write Indicator**	**Write Mode**	**Access Time (ns)**	**Write Speed (ms)**	**Endurance (Cycles)**
	5962-87514	18	X, Y	X, A	8K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte	350	1	10K
	5962-87514	19	X, Y	X, A	8K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte	300	1	10K
	5962-87514	20	X, Y, Z	X, A	8K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte	250	1	10K
	5962-87514	21	X, Y	X, A	8K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte	200	1	10K
	5962-87514	22	X, Y	X, A	8K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte	150	1	10K

	Example: Atmel Order Number	**Atmel Similar Part Number**
	5962-87514 **18 XX**	AT28C64X-35DM/883
	5962-87514 **18 YX**	AT28C64X-35LM/883
	5962-87514 **19 XX**	AT28C64X-30DM/883
	5962-87514 **19 YX**	AT28C64X-30LM/883
	5962-87514 **20 XX**	AT28C64X-25DM/883
	5962-87514 **20 YX**	AT28C64X-25LM/883
	5962-87514 **20 ZX**	AT28C64X-25FM/883
	5962-87514 **21 XX**	AT28C64X-20DM/883
	5962-87514 **21 YX**	AT28C64X-20LM/883
	5962-87514 **22 XX**	AT28C64X-15DM/883
Atmel Cage No. 1FN41	5962-87514 **22 YX**	AT28C64X-15LM/883

Case Outline	
X	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
Y	32L, 32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
Z	28F, 28 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)
Lead Finish	
X	Denotes no preference in lead finish; Finish A will be supplied (per paragraph 30.6.2.7 of MIL-I-38535B Appendix A)
A	Hot Solder Dip

Note: New designs to use AT28C256 product SMD 5962-88525.

Table 1. Atmel SMD Part Types, Listed by Atmel Part Number

AT28C64B									
Generic Number	Standard Microcircuit Drawing Number				Description				
28C64B	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description End Write Indicator	Write Mode	Access Time (ns)	Write Speed (ms)	Endurance (Cycles)
	5962-87514	08	X	X, A	8K x 8 EEPROM Data Polling	Byte/ Page	250	2	10K
	5962-87514	09	X	X, A	8K x 8 EEPROM Data Polling	Byte/ Page	200	2	10K
Atmel Cage No. 1FN41	Example: Atmel Order Number				Atmel Similar Part Number				
	5962-87514 **08 XX**				AT28C64B-25DM/883				
	5962-87514 **09 XX**				AT28C64B-20DM/883				
Case Outline									
X	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)								
Lead Finish									
X	Denotes no preference in lead finish; Finish A will be supplied (per paragraph 30.6.2.7 of MIL-I-38535B Appendix A)								
A	Hot Solder Dip								

Note: New designs to use AT28C256 product SMD 5962-88525.

AT28HC64B									
Generic Number	Standard Microcircuit Drawing Number				Description				
28HC64B	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description End Write Indicator	Write Mode	Access Time (ns)	Write Speed (ms)	Endurance (Cycles)
	5962-87514	10	X	X, A	8K x 8 EEPROM Data Polling	Byte/ Page	120	2	10K
	5962-87514	11	X	X, A	8K x 8 EEPROM Data Polling	Byte/ Page	90	2	10K
	5962-87514	12	X	X, A	8K x 8 EEPROM Data Polling	Byte/ Page	70	2	10K
Atmel Cage No. 1FN41	Example: Atmel Order Number				Atmel Similar Part Number				
	5962-87514 **10 XX**				AT28HC64B-12DM/883				
	5962-87514 **11 XX**				AT28HC64B-90DM/883				
	5962-87514 **12 XX**				AT28HC64B-70DM/883				
Case Outline									
X	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)								
Lead Finish									
X	Denotes no preference in lead finish; Finish A will be supplied (per paragraph 30.6.2.7 of MIL-I-38535B Appendix A)								
A	Hot Solder Dip								

Note: New designs to use AT28C256 product SMD 5962-88634.

Table 1. Atmel SMD Part Types, Listed by Atmel Part Number

AT28C256									
Generic Number	**Standard Microcircuit Drawing Number**				**Description**				
28C256	**Drawing Number**	**Device Type**	**Case Outline**	**Lead Finish**	**Circuit Description End Write Indicator**	**Write Mode**	**Access Time (ns)**	**Write Speed (ms)**	**Endurance (Cycles)**
	5962-88525	01	U, X, Y, Z	X, A	32K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	350	10	10K
	5962-88525	02	U, X, Y, Z	X, A	32K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	300	10	10K
	5962-88525	03	U, X, Y, Z	X, A	32K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	250	10	10K
	5962-88525	04	U, X, Y, Z	X, A	32K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	200	10	10K
	5962-88525	06	U, X, Y, Z	X, A	32K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	150	10	10K
	5962-88525	09(1)	U, X, Y, Z	X, A	32K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	350	10	10K
	5962-88525	10(1)	U, X, Y, Z	X, A	32K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	300	10	10K
	5962-88525	11(1)	U, X, Y, Z	X, A	32K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	250	10	10K
	5962-88525	12(1)	U, X, Y, Z	X, A	32K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	200	10	10K
	5962-88525	14(1)	U, X, Y, Z	X, A	32K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	150	10	10K

	Example: Atmel Order Number	**Atmel Similar Part Number**
	5962-88525 **01 UX**	AT28C256-35UM/883
	5962-88525 **01 XX**	AT28C256-35DM/883
	5962-88525 **01 YX**	AT28C256-35LM/883
	5962-88525 **01 ZX**	AT28C256-35FM/883
	5962-88525 **02 UX**	AT28C256-30UM/883
	5962-88525 **02 XX**	AT28C256-30DM/883
	5962-88525 **02 YX**	AT28C256-30LM/883
	5962-88525 **02 ZX**	AT28C256-30FM/883
	5962-88525 **03 UX**	AT28C256-25UM/883
	5962-88525 **03 XX**	AT28C256-25DM/883
	5962-88525 **03 YX**	AT28C256-25LM/883
	5962-88525 **03 ZX**	AT28C256-25FM/883
	5962-88525 **04 UX**	AT28C256-20UM/883
	5962-88525 **04 XX**	AT28C256-20DM/883
	5962-88525 **04 YX**	AT28C256-20LM/883
Atmel Cage No. 1FN41	5962-88525 **04 ZX**	AT28C256-20FM/883

Table 1. Atmel SMD Part Types, Listed by Atmel Part Number

AT28C256 (Continued)		
	Example: Atmel Order Number	**Atmel Similar Part Number**
	5962-88525 **06 UX**	AT28C256-15UM/883
	5962-88525 **06 XX**	AT28C256-15DM/883
	5962-88525 **06 YX**	AT28C256-15LM/883
	5962-88525 **06 ZX**	AT28C256-15FM/883
	5962-88525 **09 UX**	AT28C256-35UM/883
	5962-88525 **09 XX**	AT28C256-35DM/883
	5962-88525 **09 YX**	AT28C256-35LM/883
	5962-88525 **09 ZX**	AT28C256-35FM/883
	5962-88525 **10 UX**	AT28C256-30UM/883
	5962-88525 **10 XX**	AT28C256-30DM/883
	5962-88525 **10 YX**	AT28C256-30LM/883
	5962-88525 **10 ZX**	AT28C256-30FM/883
	5962-88525 **11 UX**	AT28C256-25UM/883
	5962-88525 **11 XX**	AT28C256-25DM/883
	5962-88525 **11 YX**	AT28C256-25LM/883
	5962-88525 **11 ZX**	AT28C256-25FM/883
	5962-88525 **12 UX**	AT28C256-20UM/883
	5962-88525 **12 XX**	AT28C256-20DM/883
	5962-88525 **12 YX**	AT28C256-20LM/883
	5962-88525 **12 ZX**	AT28C256-20FM/883
	5962-88525 **14 UX**	AT28C256-15UM/883
	5962-88525 **14 XX**	AT28C256-15DM/883
	5962-88525 **14 YX**	AT28C256-15LM/883
Atmel Cage No. 1FN41	5962-88525 **14 ZX**	AT28C256-15FM/883

Case Outline	
U	28U, 28 Pin, Ceramic Pin Grid Array (PGA)
X	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
Y	32L, 32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
Z	28F, 28 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)
Lead Finish	
X	Denotes no preference in lead finish; Finish A will be supplied (per paragraph 30.6.2.7 of MIL-I-38535B Appendix A)
A	Hot Solder Dip

Note: 1. SMD specifies Software Data Protection feature for device type, although Atmel product supplied to *every* device type on the SMD is 100% tested for this feature.

Table 1. Atmel SMD Part Types, Listed by Atmel Part Number

AT28C256E									
Generic Number	**Standard Microcircuit Drawing Number**				**Description**				
28C256E	**Drawing Number**	**Device Type**	**Case Outline**	**Lead Finish**	**Circuit Description End Write Indicator**	**Write Mode**	**Access Time (ns)**	**Write Speed (ms)**	**Endurance (Cycles)**
	5962-88525	05	U, X, Y, Z	X, A	32K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte Page	250	10	100K
	5962-88525	08	U, X, Y, Z	X, A	32K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	150	10	100K
	5962-88525	13(1)	U, X, Y, Z	X, A	32K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	250	10	100K
	5962-88525	16(1)	U, X, Y, Z	X, A	32K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	150	10	100K
	Example: Atmel Order Number				**Similar Part Number**				
	5962-88525 **05 UX**				AT28C256E-25UM/883				
	5962-88525 **05 XX**				AT28C256E-25DM/883				
	5962-88525 **05 YX**				AT28C256E-25LM/883				
	5962-88525 **05 ZX**				AT28C256E-25FM/883				
	5962-88525 **08 UX**				AT28C256E-15UM/883				
	5962-88525 **08 XX**				AT28C256E-15DM/883				
	5962-88525 **08 YX**				AT28C256E-15LM/883				
	5962-88525 **08 ZX**				AT28C256E-15FM/883				
	5962-88525 **13 UX**				AT28C256E-25UM/883				
	5962-88525 **13 XX**				AT28C256E-25DM/883				
	5962-88525 **13 YX**				AT28C256E-25LM/883				
	5962-88525 **13 ZX**				AT28C256E-25FM/883				
	5962-88525 **16 UX**				AT28C256E-15UM/883				
	5962-88525 **16 XX**				AT28C256E-15DM/883				
	5962-88525 **16 YX**				AT28C256E-15LM/883				
Atmel Cage No. 1FN41	5962-88525 **16 ZX**				AT28C256E-15FM/883				

Case Outline	
U	28U, 28 Pin, Ceramic Pin Grid Array (PGA)
X	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
Y	32L, 32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
Z	28F, 28 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)
Lead Finish	
X	Denotes no preference in lead finish; Finish A will be supplied (per paragraph 30.6.2.7 of MIL-I-38535B Appendix A)
A	Hot Solder Dip

Note: 1. SMD specifies Software Data Protection feature for device type, although Atmel product supplied to *every* device type on the SMD is 100% tested for this feature.

Table 1. Atmel SMD Part Types, Listed by Atmel Part Number

AT28C256F									
Generic Number	**Standard Microcircuit Drawing Number**				**Description**				
28C256F	**Drawing Number**	**Device Type**	**Case Outline**	**Lead Finish**	**Circuit Description End Write Indicator**	**Write Mode**	**Access Time (ns)**	**Write Speed (ms)**	**Endurance (Cycles)**
	5962-88525	07	U, X, Y, Z	X, A	32K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	150	3	10K
	5962-88525	15[1]	U, X, Y, Z	X, A	32K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	150	3	10K
	Example: Atmel Order Number				**Atmel Similar Part Number**				
	5962-88525 **07 UX**				AT28C256F-15UM/883				
	5962-88525 **07 XX**				AT28C256F-15DM/883				
	5962-88525 **07 YX**				AT28C256F-15LM/883				
	5962-88525 **07 ZX**				AT28C256F-15FM/883				
	5962-88525 **15 UX**				AT28C256F-15UM/883				
	5962-88525 **15 XX**				AT28C256F-15DM/883				
	5962-88525 **15 YX**				AT28C256F-15LM/883				
Atmel Cage No. 1FN41	5962-88525 **15 ZX**				AT28C256F-15FM/883				

Case Outline	
U	28U, 28 Pin, Ceramic Pin Grid Array (PGA)
X	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
Y	32L, 32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
Z	28F, 28 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)

Lead Finish	
X	Denotes no preference in lead finish; Finish A will be supplied (per paragraph 30.6.2.7 of MIL-I-38535B Appendix A)
A	Hot Solder Dip

Note: 1. SMD specifies Software Data Protection feature for device type, although Atmel product supplied to *every* device type on the SMD is 100% tested for this feature.

Table 1. Atmel SMD Part Types, Listed by Atmel Part Number

AT28HC256									
Generic Number	**Standard Microcircuit Drawing Number**				**Description**				
28HC256	**Drawing Number**	**Device Type**	**Case Outline**	**Lead Finish**	**Circuit Description End Write Indicator**	**Write Mode**	**Access Time (ns)**	**Write Speed (ms)**	**Endurance (Cycles)**
	5962-88634	01	U, X, Y, Z	X, A	32K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	120	10	10K
	5962-88634	03	U, X, Y, Z	X, A	32K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	90	10	10K
	Example: Atmel Order Number				**Similar Part Number**				
	5962-88634 **01 UX**				AT28HC256-12UM/883				
	5962-88634 **01 XX**				AT28HC256-12DM/883				
	5962-88634 **01 YX**				AT28HC256-12LM/883				
	5962-88634 **01 ZX**				AT28HC256-12FM/883				
	5962-88634 **03 UX**				AT28HC256-90UM/883				
	5962-88634 **03 XX**				AT28HC256-90DM/883				
	5962-88634 **03 YX**				AT28HC256-90LM/883				
Atmel Cage No. 1FN41	5962-88634 **03 ZX**				AT28HC256-90FM/883				

Case Outline	
U	28U, 28 Pin, Ceramic Pin Grid Array (PGA)
X	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
Y	32L, 32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
Z	28F, 28 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)
Lead Finish	
X	Denotes no preference in lead finish; Finish A will be supplied (per paragraph 30.6.2.7 of MIL-I-38535B Appendix A)
A	Hot Solder Dip

Table 1. Atmel SMD Part Types, Listed by Atmel Part Number

AT28HC256F									
Generic Number	**Standard Microcircuit Drawing Number**				**Description**				
28HC256F	**Drawing Number**	**Device Type**	**Case Outline**	**Lead Finish**	**Circuit Description End Write Indicator**	**Write Mode**	**Access Time (ns)**	**Write Speed (ms)**	**Endurance (Cycles)**
	5962-88634	02	U, X, Y, Z	X, A	32K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	120	3	10K
	5962-88634	04	U, X, Y, Z	X, A	32K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	90	3	10K
	Example: Atmel Order Number				**Atmel Similar Part Number**				
	5962-88634 **02 UX**				AT28HC256F-12UM/883				
	5962-88634 **02 XX**				AT28HC256F-12DM/883				
	5962-88634 **02 YX**				AT28HC256F-12LM/883				
	5962-88634 **02 ZX**				AT28HC256F-12FM/883				
	5962-88634 **04 UX**				AT28HC256F-90UM/883				
	5962-88634 **04 XX**				AT28HC256F-90DM/883				
	5962-88634 **04 YX**				AT28HC256F-90LM/883				
Atmel Cage No. 1FN41	5962-88634 **04 ZX**				AT28HC256F-90FM/883				
Case Outline									
U	28U, 28 Pin, Ceramic Pin Grid Array (PGA)								
X	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)								
Y	32L, 32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)								
Z	28F, 28 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)								
Lead Finish									
X	Denotes no preference in lead finish; Finish A will be supplied (per paragraph 30.6.2.7 of MIL-I-38535B Appendix A)								
A	Hot Solder Dip								

Table 1. Atmel SMD Part Types, Listed by Atmel Part Number

AT28C010

Generic Number	Standard Microcircuit Drawing Number				Description				
28C010	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description End Write Indicator	Write Mode	Access Time (ns)	Write Spd (ms)	Endurance (Cycles)
	5962-38267	01	T, U, X, Y, Z	X, A	128K x 8, 1M bit EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	250	10	10K
	5962-38267	03	T, U, X, Y, Z	X, A	128K x 8, 1M bit EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	200	10	10K
	5962-38267	05	T, U, X, Y, Z	X, A	128K x 8, 1M bit EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	150	10	10K
	5962-38267	07	U, X, Y, Z	X, A	128K x 8, 1M bit EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	120	10	10K

	Example: Atmel Order Number	Atmel Similar Part Number
Atmel Cage No. 1FN41	5962-38267 **01M TX**	AT28C010-25UM/883
	5962-38267 **01M UX**	AT28C010-25EM/883
	5962-38267 **01M XX**	AT28C010-25DM/883
	5962-38267 **01M YX**	AT28C010-25LM/883
	5962-38267 **01M ZX**	AT28C010-25FM/883
	5962-38267 **03M TX**	AT28C010-20UM/883
	5962-38267 **03M UX**	AT28C010-20EM/883
	5962-38267 **03M XX**	AT28C010-20DM/883
	5962-38267 **03M YX**	AT28C010-20LM/883
	5962-38267 **03M ZX**	AT28C010-20FM/883
	5962-38267 **05M TX**	AT28C010-15UM/883
	5962-38267 **05M UX**	AT28C010-15EM/883
	5962-38267 **05M XX**	AT28C010-15DM/883
	5962-38267 **05M YX**	AT28C010-15LM/883
	5962-38267 **05M ZX**	AT28C010-15FM/883
	5962-38267 **07M UX**	AT28C010-12EM/883
	5962-38267 **07M XX**	AT28C010-12DM/883
	5962-38267 **07M YX**	AT28C010-12LM/883
	5962-38267 **07M ZX**	AT28C010-12FM/883

Case Outline	
T	30U, 30 Pin, Ceramic Pin Grid Array (PGA)
U	32L, 32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
X	32D6, 32 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
Y	44L, 44 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
Z	32F, 32 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)

Lead Finish	
X	Denotes no preference in lead finish; Finish A will be supplied (per paragraph 30.6.2.7 of MIL-I-38535B Appendix A)
A	Hot Solder Dip

Table 2. Atmel SMD Part Types, Listed by SMD Number

5962-38267						
Atmel Order Number	Atmel Similar Part Number	Circuit Description End Write Indicator	Write Mode	Access Time (ns)	Write Spd. (ms)	Endur. (Cycles)
5962-38267 01M XX	AT28C010-25DM/883	128K x 8, 1M bit EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	250	10	10K
5962-38267 01M YX	AT28C010-25LM/883	128K x 8, 1M bit EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	250	10	10K
5962-38267 01M ZX	AT28C010-25FM/883	128K x 8, 1M bit EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	250	10	10K
5962-38267 03M XX	AT28C010-20DM/883	128K x 8, 1M bit EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	200	10	10K
5962-38267 03M YX	AT28C010-20LM/883	128K x 8, 1M bit EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	200	10	10K
5962-38267 03M ZX	AT28C010-20FM/883	128K x 8, 1M bit EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	200	10	10K
5962-38267 05M XX	AT28C010-15DM/883	128K x 8, 1M bit EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	150	10	10K
5962-38267 05M YX	AT28C010-15LM/883	128K x 8, 1M bit EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	150	10	10K
5962-38267 05M ZX	AT28C010-15FM/883	128K x 8, 1M bit EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	150	10	10K
5962-38267 07M XX	AT28C010-12DM/883	128K x 8, 1M bit EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	120	10	10K
5962-38267 07M YX	AT28C010-12LM/883	128K x 8, 1M bit EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	120	10	10K
5962-38267 07M ZX	AT28C010-12FM/883	128K x 8, 1M bit EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	120	10	10K

Table 2. Atmel SMD Part Types, Listed by SMD Number

5962-87514						
Atmel Order Number	Atmel Similar Part Number	Circuit Description End Write Indicator	Write Mode	Access Time (ns)	Write Spd. (ms)	Endur. (Cycles)
5962-87514 08 XX	AT28C64B-25DM/883	8K x 8 EEPROM Data Polling	Byte/ Page	250	10	10K
5962-87514 09 XX	AT28C64B-20DM/883	8K x 8 EEPROM Data Polling	Byte/ Page	200	10	10K
5962-87514 10 XX	AT28HC64B-12DM/883	8K x 8 EEPROM Data Polling	Byte/ Page	120	2	10K
5962-87514 11 XX	AT28HC64B-90DM/883	8K x 8 EEPROM Data Polling	Byte/ Page	90	2	10K
5962-87514 12 XX	AT28HC64B-70DM/883	8K x 8 EEPROM Data Polling	Byte/ Page	70	2	10K
5962-87514 13 XX	AT28C64-35DM/883	8K x 8 EEPROM Rdy/Busy	Byte	350	1	10K
5962-87514 13 YX	AT28C64-35LM/883	8K x 8 EEPROM Rdy/Busy	Byte	350	1	10K
5962-87514 13 ZX	AT28C64-35FM/883	8K x 8 EEPROM Rdy/Busy	Byte	350	1	10K
5962-87514 14 XX	AT28C64-30DM/883	8K x 8 EEPROM Rdy/Busy	Byte	300	1	10K
5962-87514 14 YX	AT28C64-30LM/883	8K x 8 EEPROM Rdy/Busy	Byte	300	1	10K
5962-87514 15 XX	AT28C64-25DM/883	8K x 8 EEPROM Rdy/Busy	Byte	250	1	10K
5962-87514 15 YX	AT28C64-25LM/883	8K x 8 EEPROM Rdy/Busy	Byte	250	1	10K
5962-87514 15 ZX	AT28C64-25FM/883	8K x 8 EEPROM Rdy/Busy	Byte	250	1	10K
5962-87514 16 XX	AT28C64-20DM/883	8K x 8 EEPROM Rdy/Busy	Byte	200	1	10K
5962-87514 16 YX	AT28C64-20LM/883	8K x 8 EEPROM Rdy/Busy	Byte	200	1	10K
5962-87514 17 XX	AT28C64-15DM/883	8K x 8 EEPROM Rdy/Busy	Byte	150	1	10K
5962-87514 17 YX	AT28C64-15LM/883	8K x 8 EEPROM Rdy/Busy	Byte	150	1	10K
5962-87514 18 XX	AT28C64X-35DM/883	8K x 8 EEPROM Data Polling	Byte	350	1	10K
5962-87514 18 YX	AT28C64X-35LM/883	8K x 8 EEPROM Data Polling	Byte	350	1	10K
5962-87514 19 XX	AT28C64X-30DM/883	8K x 8 EEPROM Data Polling	Byte	300	1	10K

Table 2. Atmel SMD Part Types, Listed by SMD Number

5962-87514 (Continued)						
Atmel Order Number	**Atmel Similar Part Number**	**Circuit Description End Write Indicator**	**Write Mode**	**Access Time (ns)**	**Write Spd. (ms)**	**Endur. (Cycles)**
5962-87514 19 YX	AT28C64X-30LM/883	8K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte	300	1	10K
5962-87514 20 XX	AT28C64X-25DM/883	8K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte	250	1	10K
5962-87514 20 YX	AT28C64X-25LM/883	8K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte	250	1	10K
5962-87514 20 ZX	AT28C64X-25FM/883	8K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte	250	1	10K
5962-87514 21 XX	AT28C64X-20DM/883	8K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte	200	1	10K
5962-87514 21 YX	AT28C64X-20LM/883	8K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte	200	1	10K
5962-87514 22 XX	AT28C64X-15DM/883	8K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte	150	1	10K
5962-87514 22 YX	AT28C64X-15LM/883	8K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte	150	1	10K
5962-87514 28 XX	AT28C64F-20DM/883	8K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte	200	0.2	10K
5962-87514 28 YX	AT28C64X-20LM/883	8K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte	200	0.2	10K
5962-87514 28 ZX	AT28C64X-20FM/883	8K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte	200	0.2	10K

Table 2. Atmel SMD Part Types, Listed by SMD Number

5962-88525						
Atmel Order Number	**Atmel Similar Part Number**	**Circuit Description End Write Indicator**	**Write Mode**	**Access Time (ns)**	**Write Spd. (ms)**	**Endur. (Cycles)**
5962-88525 01 UX	AT28C256-35UM/883	32K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	350	10	10K
5962-88525 01 XX	AT28C256-35DM/883	32K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	350	10	10K
5962-88525 01 YX	AT28C256-35LM/883	32K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	350	10	10K
5962-88525 01 ZX	AT28C256-35FM/883	32K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	350	10	10K
5962-88525 02 UX	AT28C256-30UM/883	32K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	300	10	10K
5962-88525 02 XX	AT28C256-30DM/883	32K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	300	10	10K
5962-88525 02 YX	AT28C256-30LM/883	32K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	300	10	10K
5962-88525 02 ZX	AT28C256-30FM/883	32K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	300	10	10K
5962-88525 03 UX	AT28C256-25UM/883	32K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	250	10	10K
5962-88525 03 XX	AT28C256-25DM/883	32K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	250	10	10K
5962-88525 03 YX	AT28C256-25LM/883	32K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	250	10	10K
5962-88525 03 ZX	AT28C256-25FM/883	32K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	250	10	10K
5962-88525 04 UX	AT28C256-20UM/883	32K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	200	10	10K
5962-88525 04 XX	AT28C256-20DM/883	32K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	200	10	10K
5962-88525 04 YX	AT28C256-20LM/883	32K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	200	10	10K
5962-88525 04 ZX	AT28C256-20FM/883	32K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	200	10	10K
5962-88525 05 UX	AT28C256E-25UM/883	32K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	250	10	100K
5962-88525 05 XX	AT28C256E-25DM/883	32K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	250	10	100K
5962-88525 05 YX	AT28C256E-25LM/883	32K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	250	10	100K
5962-88525 05 ZX	AT28C256E-25FM/883	32K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	250	10	100K

Table 2. Atmel SMD Part Types, Listed by SMD Number

5962-88525 (Continued)

Atmel Order Number	Atmel Similar Part Number	Circuit Description End Write Indicator	Write Mode	Access Time (ns)	Write Spd. (ms)	Endur. (Cycles)
5962-88525 06 UX	AT28C256-15UM/883	32K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	150	10	10K
5962-88525 06 XX	AT28C256-15DM/883	32K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	150	10	10K
5962-88525 06 YX	AT28C256-15LM/883	32K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	150	10	10K
5962-88525 06 ZX	AT28C256-15FM/883	32K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	150	10	10K
5962-88525 07 UX	AT28C256F-15UM/883	32K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	150	3	10K
5962-88525 07 XX	AT28C256F-15DM/883	32K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	150	3	10K
5962-88525 07 YX	AT28C256F-15LM/883	32K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	150	3	10K
5962-88525 07 ZX	AT28C256F-15FM/883	32K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	150	3	10K
5962-88525 08 UX	AT28C256E-15UM/883	32K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	150	10	100K
5962-88525 08 XX	AT28C256E-15DM/883	32K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	150	10	100K
5962-88525 08 YX	AT28C256E-15LM/883	32K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	150	10	100K
5962-88525 08 ZX	AT28C256E-15FM/883	32K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	150	10	100K
5962-88525 09 UX(1)	AT28C256-35UM/883	32K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	350	10	10K
5962-88525 09 XX(1)	AT28C256-35DM/883	32K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	350	10	10K
5962-88525 09 YX(1)	AT28C256-35LM/883	32K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	350	10	10K
5962-88525 09 ZX(1)	AT28C256-35FM/883	32K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	350	10	10K
5962-88525 10 UX(1)	AT28C256-30UM/883	32K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	300	10	10K
5962-88525 10 XX(1)	AT28C256-30DM/883	32K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	300	10	10K
5962-88525 10 Y 1)	AT28C256-30LM/883	32K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	300	10	10K
5962-88525 10 ZX(1)	AT28C256-30FM/883	32K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	300	10	10K
5962-88525 11 UX(1)	AT28C256-25UM/883	32K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	250	10	10K

Table 2. Atmel SMD Part Types, Listed by SMD Number

5962-88525 (Continued)

Atmel Order Number	Atmel Similar Part Number	Circuit Description End Write Indicator	Write Mode	Access Time (ns)	Write Spd. (ms)	Endur. (Cycles)
5962-88525 11 X[1]	AT28C256-25DM/883	32K x 8 EEPROM Data Polling	Byte/ Page	250	10	10K
5962-88525 11 YX[1]	AT28C256-25LM/883	32K x 8 EEPROM Data Polling	Byte/ Page	250	10	10K
5962-88525 11 ZX[1]	AT28C256-25FM/883	32K x 8 EEPROM Data Polling	Byte/ Page	250	10	10K
5962-88525 12 UX[1]	AT28C256-20UM/883	32K x 8 EEPROM Data Polling	Byte/ Page	200	10	10K
5962-88525 12 XX[1]	AT28C256-20DM/883	32K x 8 EEPROM Data Polling	Byte/ Page	200	10	10K
5962-88525 12 YX[1]	AT28C256-20LM/883	32K x 8 EEPROM Data Polling	Byte/ Page	200	10	10K
5962-88525 12 ZX[1]	AT28C256-20FM/883	32K x 8 EEPROM Data Polling	Byte/ Page	200	10	10K
5962-88525 13 UX [1]	AT28C256E-25UM/883	32K x 8 EEPROM Data Polling	Byte/ Page	250	10	100K
5962-88525 13 XX[1]	AT28C256E-25DM/883	32K x 8 EEPROM Data Polling	Byte/ Page	250	10	100K
5962-88525 13 YX[1]	AT28C256E-25LM/883	32K x 8 EEPROM Data Polling	Byte/ Page	250	10	100K
5962-88525 13 ZX[1]	AT28C256E-25FM/883	32K x 8 EEPROM Data Polling	Byte/ Page	250	10	100K
5962-88525 14 UX[1]	AT28C256-15UM/883	32K x 8 EEPROM Data Polling	Byte/ Page	150	10	10K
5962-88525 14 XX[1]	AT28C256-15DM/883	32K x 8 EEPROM Data Polling	Byte/ Page	150	10	10K
5962-88525 14 YX[1]	AT28C256-15LM/883	32K x 8 EEPROM Data Polling	Byte/ Page	150	10	10K
5962-88525 14 ZX[1]	AT28C256-15FM/883	32K x 8 EEPROM Data Polling	Byte/ Page	150	10	10K
5962-88525 15 UX[1]	AT28C256F-15UM/883	32K x 8 EEPROM Data Polling	Byte/ Page	150	3	10K
5962-88525 15 XX[1]	AT28C256F-15DM/883	32K x 8 EEPROM Data Polling	Byte/ Page	150	3	10K
5962-88525 15 YX[1]	AT28C256F-15LM/883	32K x 8 EEPROM Data Polling	Byte/ Page	150	3	10K
5962-88525 15 ZX[1]	AT28C256F-15FM/883	32K x 8 EEPROM Data Polling	Byte/ Page	150	3	10K
5962-88525 16 UX[1]	AT28C256E-15UM/883	32K x 8 EEPROM Data Polling	Byte/ Page	150	10	100K

Table 2. Atmel SMD Part Types, Listed by SMD Number

5962-88525 (Continued)						
Atmel Order Number	Atmel Similar Part Number	Circuit Description End Write Indicator	Write Mode	Access Time (ns)	Write Spd. (ms)	Endur. (Cycles)
5962-88525 16 XX[1]	AT28C256E-15DM/883	32K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	150	10	100K
5962-88525 16 YX[1]	AT28C256E-15LM/883	32K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	150	10	100K
5962-88525 16 ZX[1]	AT28C256E-15FM/883	32K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	150	10	100K

Table 2. Atmel SMD Part Types, Listed by SMD Number

5962-88634						
Atmel Order Number	**Atmel Similar Part Number**	**Circuit Description End Write Indicator**	**Write Mode**	**Access Time (ns)**	**Write Spd. (ms)**	**Endur. (Cycles)**
5962-88634 01 UX	AT28HC256-12UM/883	32K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	120	10	10K
5962-88634 01 XX	AT28HC256-12DM/883	32K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	120	10	10K
5962-88634 01 YX	AT28HC256-12LM/883	32K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	120	10	10K
5962-88634 01 ZX	AT28HC256-12FM/883	32K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	120	10	10K
5962-88634 02 UX	AT28HC256F-12UM/883	32K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	120	3	10K
5962-88634 02 XX	AT28HC256F-12DM/883	32K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	120	3	10K
5962-88634 02 YX	AT28HC256F-12LM/883	32K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	120	3	10K
5962-88634 02 ZX	AT28HC256F-12FM/883	32K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	120	3	10K
5962-88634 03 UX	AT28HC256-90UM/883	32K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	90	10	10K
5962-88634 03 XX	AT28HC256-90DM/883	32K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	90	10	10K
5962-88634 03 YX	AT28HC256-90LM/883	32K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	90	10	10K
5962-88634 03 ZX	AT28HC256-90FM/883	32K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	90	10	10K
5962-88634 04 UX	AT28HC256F-90UM/883	32K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	90	3	10K
5962-88634 04 XX	AT28HC256F-90DM/883	32K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	90	3	10K
5962-88634 04 YX	AT28HC256F-90LM/883	32K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	90	3	10K
5962-88634 04 ZX	AT28HC256F-90FM/883	32K x 8 EEPROM $\overline{\text{Data}}$ Polling	Byte/ Page	90	3	10K

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Section 8 Die Products
Parallel EEPROM Die Products 8-3

Features

- High Performance CMOS Technology
- Low Power Dissipation - Active and Standby
- Hardware and Software Data Protection Features
- $\overline{\text{DATA}}$ Polling for End of Write Detection
- High Reliability
  - Endurance: 10^4 Cycles
  - Data Retention: 10 years
- Single 5V ± 10% Supply
- Single 3V ± 10% Supply
- CMOS Compatible Inputs and Outputs
- 0°C to +70°C Operating Range
- Typical Die Thickness of 22 Mils
- Extended Endurance: 10^5 Cycles
- Military Product Performance (-55°C to +125°C)
- Element Evaluation Program

Description

Atmel Parallel EEPROMs are available in die form. All die products are 100% electrically tested in wafer form and visually inspected after saw and clean. Atmel's EEPROM die products are processed with an advanced CMOS floating gate technology. As with all Atmel products, they are designed and tested to ensure high quality and manufacturability. The devices include such features as internal error correction for extended endurance and improved data retention characteristics.

Atmel offers a full line of 5V and 3V die products (see ordering information table). An optional Element Evaluation test flow which entails sample packaging and electrical screening in accordance with MIL-STD 883 M5008 is available for military and automotive grade applications. Standard shipping methods for Atmel die products include protective waffle and wafer carriers. Optional packaging methods are available, including wafer ring mounting and wafer orientation to accommodate the customer's manufacturing equipment.

Testing

Reference Parallel EEPROM Die Product Test Flow. Die product Sort Test includes checks for DC parameters such as I_{CC} and input leakage as well as for AC switching parameters. Data pattern testing, several oxide stress tests, and data retention high temperature bake tests are performed on a 100% basis to guard against pattern sensitivity and infant mortality, and ensure integrity of the core cell oxides. Contact Atmel for a detailed Die Product Test Flow Diagram, including all test conditions.

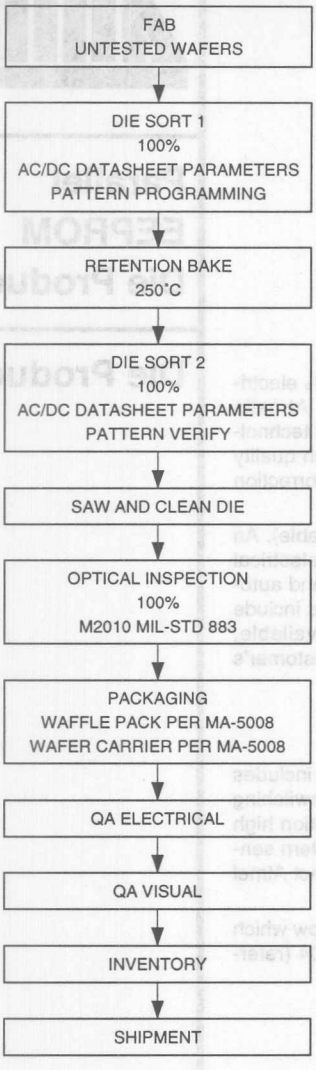
Atmel also supplies die product processed to the Element Evaluation Test Flow which includes wafer lot assembly and test in accordance with MIL-STD 883 M5004 (reference Atmel Military MIL-STD 883 Test Flow, Section 7).

Parallel EEPROM Die Products

Die Products

Rev. 0554C–06/98

Parallel EEPROM Die Product Test Flow



Die Information

- Handling: Instructions for Parallel EEPROM Die Product is available from Atmel.
- Backside Condition: Silicon (grind).
- Connection: Connect substrate to GND.
- Die Map Logo: Not to scale and is shown only as a reference for proper orientation of the wafer.

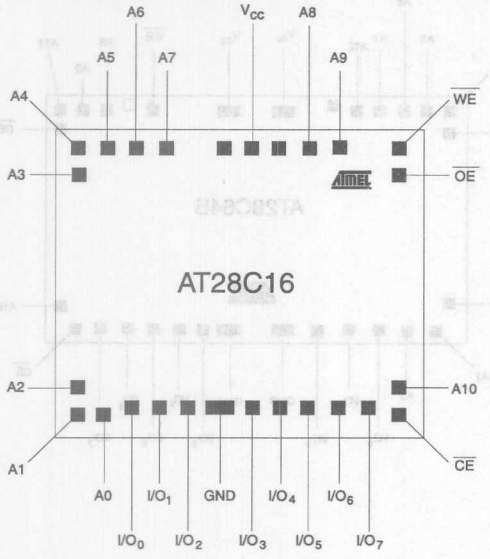
Die Product Offering – Battery Volt, 5 Volt, Low Volt

Ordering Code[1]	V_{CC}	Device T_{AA}	Package Configuration
AT28BV16-W	2.7V - 3.6V	250 ns	Die
AT28BV16-DWF	2.7V - 3.6V	250 ns	Wafer
AT28BV64-W	2.7V - 3.6V	250 ns	Die
AT28BV64-DWF	2.7V - 3.6V	250 ns	Wafer
AT28BV64B-W	2.7V - 3.6V	250 ns	Die
AT28BV64B-DWF	2.7V - 3.6V	250 ns	Wafer
AT28BV256-W	2.7V - 3.6V	250 ns	Die
AT28BV256-DWF	2.7V - 3.6V	250 ns	Wafer
AT28LV010-W	3.0V - 3.6V	250 ns	Die
AT28LV010-DWF	3.0V - 3.6V	250 ns	Wafer
AT28C16-W	4.5V - 5.5V	200 ns	Die
AT28C16-DWF	4.5V - 5.5V	200 ns	Wafer
AT28C64-W	4.5V - 5.5V	200 ns	Die
AT28C64-DWF	4.5V - 5.5V	200 ns	Wafer
AT28C64B-W	4.5V - 5.5V	200 ns	Die
AT28C64B-DWF	4.5V - 5.5V	200 ns	Wafer
AT28HC64B-W	4.5V - 5.5V	120 ns	Die
AT28HC64B-DWF	4.5V - 5.5V	120 ns	Wafer
AT28C256-W	4.5V - 5.5V	200 ns	Die
AT28C256-DWF	4.5V - 5.5V	200 ns	Wafer
AT28HC256-W	4.5V - 5.5V	120 ns	Die
AT28HC256-DWF	4.5V - 5.5V	120 ns	Wafer
AT28C010-W	4.5V - 5.5V	200 ns	Die
AT28C010-DWF	4.5V - 5.5V	200 ns	Wafer

Note: 1. Represents standard die product commercial temperature range guarantee.

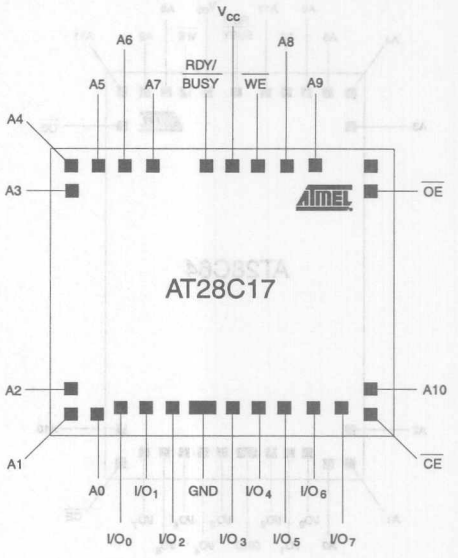
AT28C16 Die Map

Die Size: 137 X 117 mils
Connect Substrate to Ground



AT28C17 Die Map

Die Size: 137 X 117 mils
Connect Substrate to Ground



Die Pad Coordinates*

Signal Name	X (µ)	Y (µ)
A_0	-1130	-1270
A_1	-1420	-1270
A_2	-1420	-920
A_3	-1370	950
A_4	-1370	1230
A_5	-1140	1230
A_6	-900	1230
A_7	-660	1230
A_8	680	1230
A_9	920	1230
A_{10}	1630	-1000
I/O_0	-870	-1190

Signal Name	X (µ)	Y (µ)
I/O_1	-610	-1190
I/O_2	-360	-1190
I/O_3	230	-1190
I/O_4	480	-1190
I/O_5	740	-1190
I/O_6	990	-1190
I/O_7	1250	-1190
GND	-60	-1190
V_{CC}	210	1230
$\overline{WE}$	1630	1230
$\overline{OE}$	1630	1000
$\overline{CE}$	1630	-1220

*Coordinates are calculated from die center point

Die Pad Coordinates*

Signal Name	X (µ)	Y (µ)
A_0	-1130	-1270
A_1	-1420	-1270
A_2	-1420	-920
A_3	-1370	950
A_4	-1370	1230
A_5	-1140	1230
A_6	-900	1230
A_7	-660	1230
A_8	680	1230
A_9	920	1230
A_{10}	1630	-1000
I/O_0	-870	-1190
I/O_1	-610	-1190

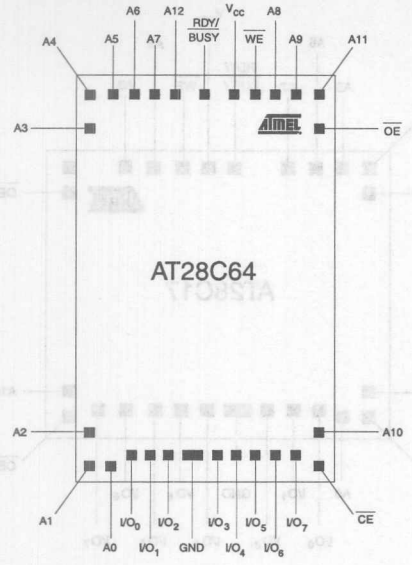
Signal Name	X (µ)	Y (µ)
I/O_2	-360	-1190
I/O_3	230	-1190
I/O_4	480	-1190
I/O_5	740	-1190
I/O_6	990	-1190
I/O_7	1250	-1190
RDY/$\overline{BSY}$	-100	1230
GND	-60	-1190
V_{CC}	210	1230
$\overline{WE}$	450	1230
$\overline{OE}$	1630	1000
$\overline{CE}$	1630	-1220

*Coordinates are calculated from die center point

Note: Die size is subject to change. Contact the Atmel Sales Representative to confirm die size.

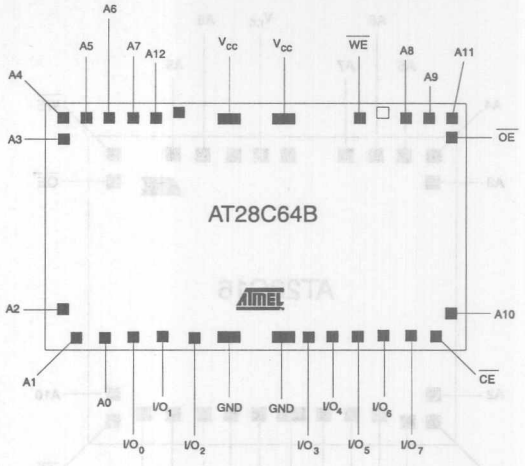
AT28C64 Die Map

Die Size: 88 X 139 mils
Connect Substrate to Ground



AT28C64B Die Map

Die Size: 178 X 120 mils
Connect Substrate to Ground



Die Pad Coordinates*

Signal Name	X (μ)	Y (μ)
A_0	-861	-1604
A_1	-1015	-1613
A_2	-1016	-1459
A_3	-987	1308
A_4	-992	1461
A_5	-838	1461
A_6	-685	1461
A_7	-532	1461
A_8	343	1461
A_9	496	1461
A_{10}	908	-1406
A_{11}	872	1506
A_{12}	-378	1461
I/O_0	-655	-1557

Signal Name	X (μ)	Y (μ)
I/O_1	-494	-1557
I/O_2	-337	-1557
I/O_3	58	-1557
I/O_4	223	-1557
I/O_5	389	-1557
I/O_6	546	-1557
I/O_7	703	-1557
RDY/$\overline{BSY}$	-122	1496
GND	-141	-1634
V_{CC}	32	1471
$\overline{WE}$	189	1461
$\overline{OE}$	870	1294
$\overline{CE}$	903	-1557

*Coordinates are calculated from die center point

Die Pad Coordinates*

Signal Name	X (μ)	Y (μ)
A_0	-1721	-1401
A_1	-1966	-1401
A_2	-2142	-1131
A_3	-2142	939
A_4	-2125	1171
A_5	-1884	1171
A_6	-1440	1171
A_7	-1237	1171
A_8	1657	1171
A_9	1832	1171
A_{10}	2035	-1128
A_{11}	2035	1171
A_{12}	-1063	1171
I/O_0	-1425	-1362

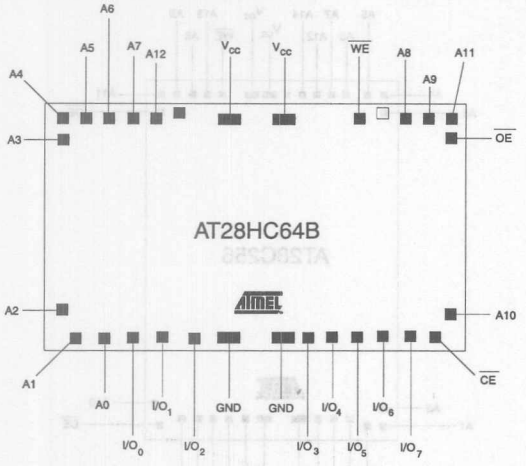
Signal Name	X (μ)	Y (μ)
I/O_1	-1126	-1362
I/O_2	-796	-1362
I/O_3	406	-1362
I/O_4	735	-1362
I/O_5	1035	-1362
I/O_6	1365	-1362
I/O_7	1664	-1362
GND	57	-1353
GND	-446	-1353
V_{CC}	-443	1240
V_{CC}	-98	1240
$\overline{WE}$	1272	1171
$\overline{OE}$	2039	939
$\overline{CE}$	1954	-1401

*Coordinates are calculated from die center point

Note: Die size is subject to change. Contact the Atmel Sales Representative to confirm die size.

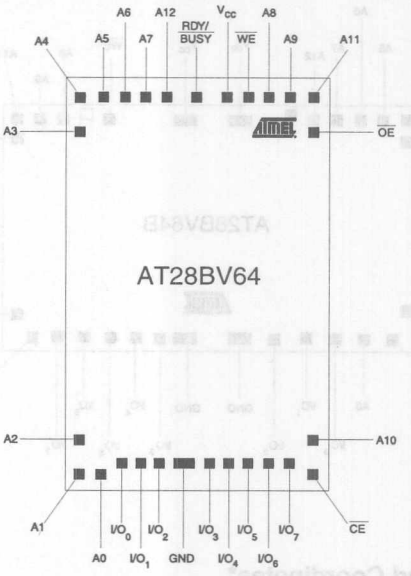
AT28HC64B Die Map

Die Size: 178 X 120 mils
Connect Substrate to Ground



AT28BV64 Die Map

Die Size: 100 X 168 mils
Connect Substrate to Ground



Die Pad Coordinates*

Signal Name	X (μ)	Y (μ)
A_0	-1721	-1401
A_1	-1966	-1401
A_2	-2142	-1131
A_3	-2142	939
A_4	-2125	1171
A_5	-1884	1171
A_6	-1440	1171
A_7	-1237	1171
A_8	1657	1171
A_9	1832	1171
A_{10}	2035	-1128
A_{11}	2035	1171
A_{12}	-1063	1171
I/O_0	-1425	-1362

Signal Name	X (μ)	Y (μ)
I/O_1	-1126	-1362
I/O_2	-796	-1362
I/O_3	406	-1362
I/O_4	735	-1362
I/O_5	1035	-1362
I/O_6	1365	-1362
I/O_7	1664	-1362
GND	57	-1353
GND	-446	-1353
V_{CC}	-443	1240
V_{CC}	-98	1240
$\overline{WE}$	1272	1171
$\overline{OE}$	2039	939
$\overline{CE}$	1954	-1401

*Coordinates are calculated from die center point

Die Pad Coordinates*

Signal Name	X (μ)	Y (μ)
A_0	-921	-1867
A_1	-1078	-1867
A_2	-1113	-1710
A_3	-1080	1702
A_4	-1075	1870
A_5	-882	1870
A_6	-721	1870
A_7	-528	1870
A_8	446	1870
A_9	607	1870
A_{10}	1097	-1720
A_{11}	1070	1924
A_{12}	-367	1870
I/O_0	-693	-1826

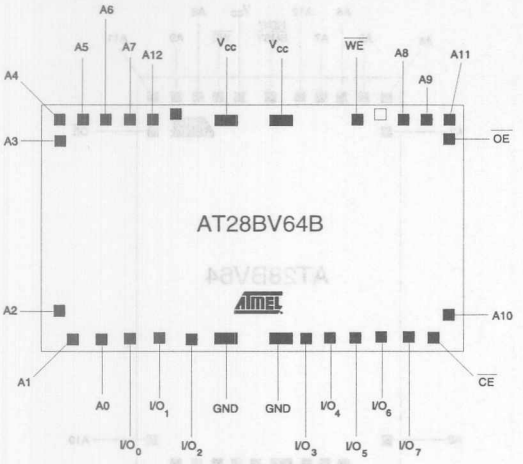
Signal Name	X (μ)	Y (μ)
I/O_1	-507	-1826
I/O_2	-326	-1826
I/O_3	124	-1826
I/O_4	315	-1826
I/O_5	506	-1826
I/O_6	688	-1826
I/O_7	869	-1826
RDY/$\overline{BSY}$	-77	1924
GND	-100	-1910
V_{CC}	89	1895
$\overline{WE}$	253	1870
$\overline{OE}$	1060	1679
$\overline{CE}$	1090	-1872

*Coordinates are calculated from die center point

Note: Die size is subject to change. Contact the Atmel Sales Representative to confirm die size.

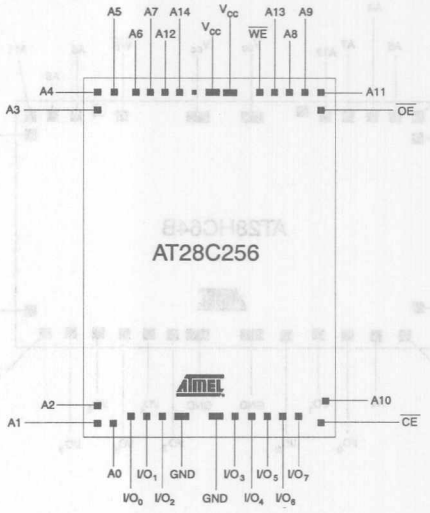
AT28BV64B Die Map

Die Size: 178 X 120 mils
Connect Substrate to Ground



AT28C256 Die Map

Die Size: 178 X 242 mils
Connect Substrate to Ground



Die Pad Coordinates*

Signal Name	X (µ)	Y (µ)
A_0	-1721	-1401
A_1	-1966	-1401
A_2	-2142	-1131
A_3	-2142	939
A_4	-2125	1171
A_5	-1884	1171
A_6	-1440	1171
A_7	-1237	1171
A_8	1657	1171
A_9	1832	1171
A_{10}	2035	-1128
A_{11}	2035	1171
A_{12}	-1063	1171
I/O_0	-1425	-1362

Signal Name	X (µ)	Y (µ)
I/O_1	-1126	-1362
I/O_2	-796	-1362
I/O_3	406	-1362
I/O_4	735	-1362
I/O_5	1035	-1362
I/O_6	1365	-1362
I/O_7	1664	-1362
GND	57	-1353
GND	-446	-1353
V_{CC}	-443	1240
V_{CC}	-98	1240
$\overline{WE}$	1272	1171
$\overline{OE}$	2039	939
$\overline{CE}$	1954	-1401

*Coordinates are calculated from die center point

Die Pad Coordinates*

Signal Name	X (µ)	Y (µ)
A_0	-1792	-2951
A_1	-2037	-2951
A_2	-2126	-2711
A_3	-2126	2490
A_4	-2108	2722
A_5	-1868	2722
A_6	-1432	2722
A_7	-1228	2722
A_8	1658	2722
A_9	1832	2722
A_{10}	2035	-2677
A_{11}	2035	2722
A_{12}	-1054	2722
A_{13}	1454	2722
A_{14}	-851	2722

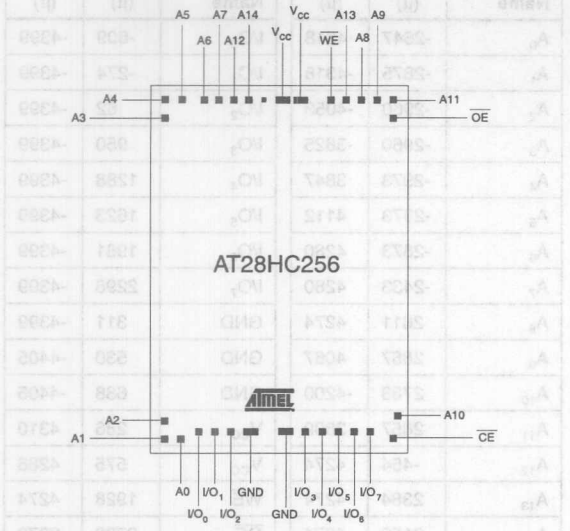
Signal Name	X (µ)	Y (µ)
I/O_0	-1416	-2911
I/O_1	-1117	-2911
I/O_2	-787	-2911
I/O_3	415	-2911
I/O_4	745	-2911
I/O_5	1044	-2911
I/O_6	1374	-2911
I/O_7	1673	-2911
GND	-438	-2902
GND	66	-2902
V_{CC}	-435	2790
V_{CC}	-89	2790
$\overline{WE}$	1280	2722
$\overline{OE}$	2039	2490
$\overline{CE}$	2035	-2951

*Coordinates are calculated from die center point

Note: Die size is subject to change. Contact the Atmel Sales Representative to confirm die size.

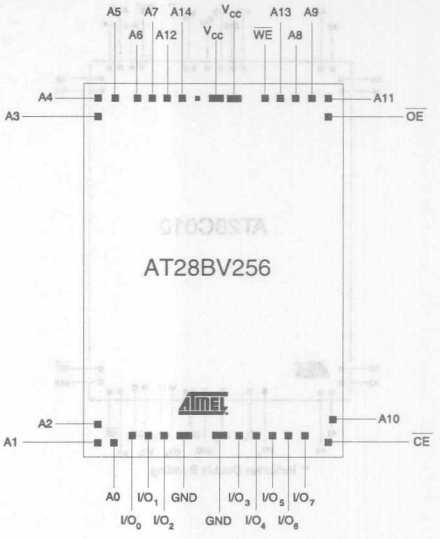
AT28HC256 Die Map

Die Size: 178 X 242 mils
Connect Substrate to Ground



AT28BV256 Die Map

Die Size: 178 X 242 mils
Connect Substrate to Ground



Die Pad Coordinates*

Signal Name	X (µ)	Y (µ)	Signal Name	X (µ)	Y (µ)
A_0	-1792	-2951	I/O_0	-1416	-2911
A_1	-2037	-2951	I/O_1	-1117	-2911
A_2	-2126	-2711	I/O_2	-787	-2911
A_3	-2126	2490	I/O_3	415	-2911
A_4	-2108	2722	I/O_4	745	-2911
A_5	-1868	2722	I/O_5	1044	-2911
A_6	-1432	2722	I/O_6	1374	-2911
A_7	-1228	2722	I/O_7	1673	-2911
A_8	1658	2722	GND	-438	-2902
A_9	1832	2722	GND	66	-2902
A_{10}	2035	-2677	V_{CC}	-435	2790
A_{11}	2035	2722	V_{CC}	-89	2790
A_{12}	-1054	2722	$\overline{WE}$	1280	2722
A_{13}	1454	2722	$\overline{OE}$	2039	2490
A_{14}	-851	2722	$\overline{CE}$	2035	-2951

*Coordinates are calculated from die center point

Die Pad Coordinates*

Signal Name	X (µ)	Y (µ)	Signal Name	X (µ)	Y (µ)
A_0	-1792	-2951	I/O_0	-1416	-2911
A_1	-2037	-2951	I/O_1	-1117	-2911
A_2	-2126	-2711	I/O_2	-787	-2911
A_3	-2126	2490	I/O_3	415	-2911
A_4	-2108	2722	I/O_4	745	-2911
A_5	-1868	2722	I/O_5	1044	-2911
A_6	-1432	2722	I/O_6	1374	-2911
A_7	-1228	2722	I/O_7	1673	-2911
A_8	1658	2722	GND	-438	-2902
A_9	1832	2722	GND	66	-2902
A_{10}	2035	-2677	V_{CC}	-435	2790
A_{11}	2035	2722	V_{CC}	-89	2790
A_{12}	-1054	2722	$\overline{WE}$	1280	2722
A_{13}	1454	2722	$\overline{OE}$	2039	2490
A_{14}	-851	2722	$\overline{CE}$	2035	-2951

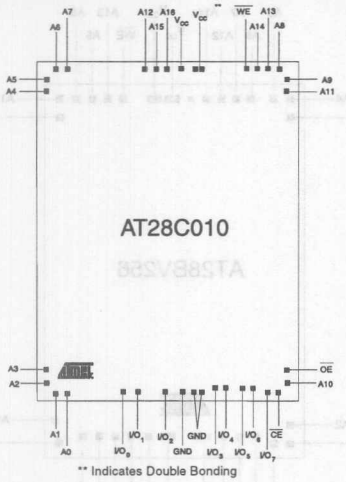
*Coordinates are calculated from die center point

Note: Die size is subject to change. Contact the Atmel Sales Representative to confirm die size.

AT28C010 Die Map

Die Size: 245 X 361 mils

Connect Substrate to Ground



Die Pad Coordinates*

Signal Name	X (µ)	Y (µ)	Signal Name	X (µ)	Y (µ)
A_0	-2647	-4318	I/O_0	-609	-4399
A_1	-2875	-4318	I/O_1	-274	-4399
A_2	-2960	-4053	I/O_2	62	-4399
A_3	-2960	-3825	I/O_3	950	-4399
A_4	-2973	3847	I/O_4	1288	-4399
A_5	-2973	4112	I/O_5	1623	-4399
A_6	-2673	4280	I/O_6	1961	-4399
A_7	-2433	4280	I/O_7	2296	-4399
A_8	2611	4274	GND	311	-4399
A_9	2857	4067	GND	530	-4405
A_{10}	2783	-4200	GND	688	-4405
A_{11}	2857	3839	V_{CC}	286	4310
A_{12}	-454	4274	V_{CC}	575	4286
A_{13}	2384	4274	$\overline{WE}$	1928	4274
A_{14}	2156	4274	$\overline{OE}$	2783	-3973
A_{15}	-226	4274	$\overline{CE}$	2716	-4444
A_{16}	2	4274			

*Coordinates are calculated from die center point

Note: Die size is subject to change. Contact the Atmel Sales Representative to confirm die size.

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Contents

Section 9 Package Outlines

Standard Package Outlines 9-3

Thermal Characteristics of Atmel Packages 9-33

Available Packing Methods and Quantities 9-37

Each Atmel data sheet includes an Ordering Information Section which specifies the package types available. This section provides size specifications and outlines for all package types.[1]

Standard Package Outlines

Package	Description	See Page
44A	44-Lead, Thin (1.0 mm) Plastic Quad Flat Package (TQFP)	9-7
48A	48-Lead, Low Profile (1.4) Plastic Quad Flat Package (LQFP)	9-7
64A	64-Lead Thin (1.0 mm) Plastic Quad Flat Package (TQFP)	9-7
100A	100-Lead, Thin (1.0 mm) Plastic Quad Flat Package (TQFP)	9-7
144A	144-Lead, Low Profile (1.4 mm) Plastic Quad Flat Package (LQFP)	9-8
32B	32-Lead, 0.600" Wide, Ceramic Side Braze Dual Inline (Side Braze)	9-8
40B	40-Lead, 0.600" Wide, Ceramic Side Braze Dual Inline (Side Braze)	9-8
8C	8-Lead,0.230" Wide, Leadless Array Package (LAP)	9-8
8C1	8-Lead,0.300" Wide, Leadless Array Package (LAP)	9-9
24C1	24-Ball, Plastic Chip-Size Ball Grid Array Package (CBGA)	9-9
24C2	24-Ball, Plastic Chip-Size Ball Grid Array Package (CBGA)	9-9
42C1	42-Ball, Plastic Chip-Size Ball Grid Array Package (CBGA)	9-9
42C2	42-Ball, Plastic Chip-Size Ball Grid Array Package (CBGA)	9-10
48C1	48-Ball, Plastic Chip-Size Ball Grid Array Package (CBGA)	9-10
48C2	48-Ball, Plastic Chip-Size Ball Grid Array Package (CBGA)	9-10
72C1	72-Ball, Plastic Chip-Size Ball Grid Array Package (CBGA)	9-10
120C1	120-Ball, Plastic Chip-Size Ball Grid Array Package (CBGA)	9-11
16D3	16-Lead, 0.300" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)	9-11
20D3	20-Lead, 0.300" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)	9-11
24D3	24-Lead, 0.300" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)	9-11
24D6	24-Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)	9-12
28D6	28-Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)	9-12

Note: 1. Dimensions shown do not include lead plating or mold flash.

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Package	Description	See Page
32D6	32-Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)	9-12
40D6	40-Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)	9-12
24DW3	24-Lead, 0.300" Wide, WIndowed, Ceramic Dual Inline Package (Cerdip)	9-13
24DW6	24-Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)	9-13
28DW6	28-Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)	9-13
32DW6	32-Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)	9-13
40DW6	40-Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)	9-14
42DW6	42-Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)	9-14
28F	28-Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)	9-14
32F	32-Lead, Non-WIndowed, Ceramic Bottom-Brazed Flat Package (Flatpack)	9-14
20J	20-Lead, Plastic J-Leaded Chip Carrier (PLCC)	9-15
28J	28-Lead, Plastic J-Leaded Chip Carrier (PLCC)	9-15
32J	32-Lead, Plastic J-Leaded Chip Carrier (PLCC)	9-15
44J	44-Lead, Plastic J-Leaded Chip Carrier (PLCC)	9-15
68J	68-Lead, Plastic J-Leaded Chip Carrier (PLCC)	9-16
84J	84-Lead, Plastic J-Leaded Chip Carrier (PLCC)	9-16
32K	32-Lead, Non-Windowed, Ceramic J-Leaded Chip Carrier (JLCC)	9-16
44K	44-Lead, Non-Windowed, Ceramic J-Leaded Chip Carrier (JLCC)	9-16
28KW	28-Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)	9-17
32KW	32-Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)	9-17
44KW	44-Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)	9-17
68KW	68-Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)	9-17
20L	20-Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)	9-18
28L	28-Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)	9-18
32L	32-Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)	9-18
44L	44-Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)	9-18
28LW	28-Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)	9-19
32LW	32-Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)	9-19
44LW	44-Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)	9-19
8M	8-Lead, 0.118" Wide, Miniature Small Outline (MSOP)	9-19
48M1	48-Ball, Micro Ball Grid Array Package (mBGA)	9-20
8P3	8-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)	9-20
16P3	16-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)	9-20
20P3	20-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)	9-20
24P3	24-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)	9-21
28P3	28-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)	9-21

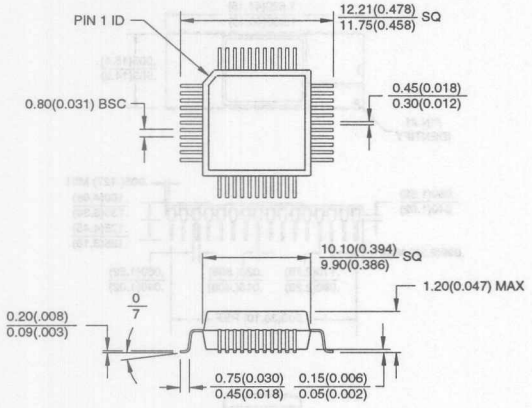
Packages

Package	Description	See Page
24P6	24-Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)	9-21
28P6	28-Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)	9-21
32P6	32-Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)	9-22
40P6	40-Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)	9-22
42P6	42-Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)	9-22
44Q	44-Lead, Plastic Gull Wing Quad Flat Package (PQFP)	9-22
132Q	132-Lead, Bumpered Plastic Gull Wing Quad Flat Package (BQFP)	9-23
136Q	136-Lead, Plastic Gull Wing Quad Flat Package (PQFP)	9-23
144Q	144-Lead, Plastic Gull Wing Quad Flat Package (PQFP)	9-23
160Q	160-Lead, Plastic Gull Wing Quad Flat Package (PQFP)	9-23
208Q	208-Lead, Plastic Gull Wing Quad Flat Package (PQFP)	9-24
240Q	240-Lead, Plastic Gull Wing Quad Flat Package (PQFP)	9-24
100Q1	100-Lead Plastic Quad Flat Package (PQFP)	9-24
100Q2	100-Lead Plastic Quad Flat Package (PQFP)	9-24
28R	28-Lead, 0.330" Wide, Plastic Gull Wing Small Outline (SOIC)	9-25
32R	32-Lead, 0.440" Wide, Plastic Gull Wing Small Outline (SOIC)	9-25
40R	40-Lead, 0.440" Wide, Plastic Gull Wing Small Outline (SOIC)	9-25
44R	44-Lead, 0.525" Wide, Plastic Gull Wing Small Outline (SOIC)	9-25
14S	14-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)	9-26
16S	16-Lead, 0.300" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)	9-26
16S1	16-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)	9-26
20S	20-Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)	9-26
24S	24-Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)	9-26
28S	28-Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)	9-27
8S1	8-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)	9-27
8S2	8-Lead, 0.210" Wide, Plastic Gull Wing Small Outline (EIAJ SOIC)	9-27
8T	8-Lead, Plastic Thin Shrink Small Outline Package (TSSOP)	9-27
14T	14-Lead, 0.170" Wide, Thin Shrink Small Outline Package (TSSOP)	9-28
20T	20-Lead, 0.170" Wide, Thin Shrink Small Outline Package (TSSOP)	9-28
28T	28-Lead, Plastic Thin Small Outline Package (TSOP)	9-28
32T	32-Lead, Plastic Thin Small Outline Package (TSOP)	9-28
40T	40-Lead, Plastic Thin Small Outline Package (TSOP)	9-29
48T	48-Lead, Plastic Thin Small Outline Package (TSOP)	9-29
86T	86-Lead, Plastic Thin Small Outline Package (TSOP)	9-29
28U	28-Pin, Ceramic Pin Grid Array (PGA)	9-29
30U	30-Pin, Ceramic Pin Grid Array (PGA)	9-30

Package	Description	See Page
180U	180-Pin, Ceramic Pin Grid Array (PGA)	9-30
68UW	68-Pin, Ceramic Pin Grid Array (PGA)	9-30
32V	32-Lead, Plastic Thin Small Outline Package (TSOP)	9-30
40V	40-Lead, Plastic Thin Small Outline Package (TSOP)	9-31
20X	20-Lead, 4.4 mm Wide, Plastic Thin Shrink Small Outline (TSSOP)	9-31
24X	24-Lead, 4.4 mm Wide, Plastic Thin Shrink Small Outline (TSSOP)	9-31
20Y	20-Lead, 5.3 mm Wide, Plastic Shrink Small Outline (SSOP)	9-31

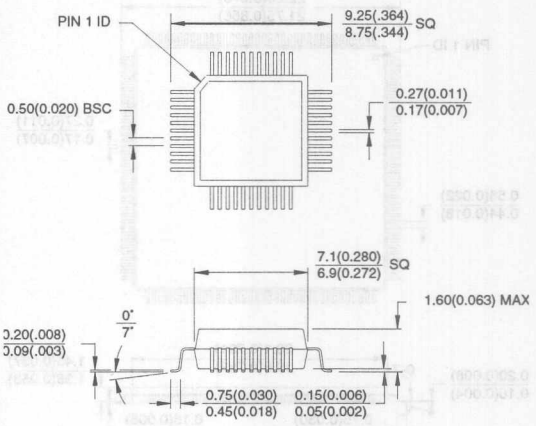
Packaging Information

44A, 44-Lead, Thin (1.0 mm) Plastic Quad Flat Package (TQFP)
Dimensions in Millimeters and (Inches)*
JEDEC STANDARD MS-026 ACB



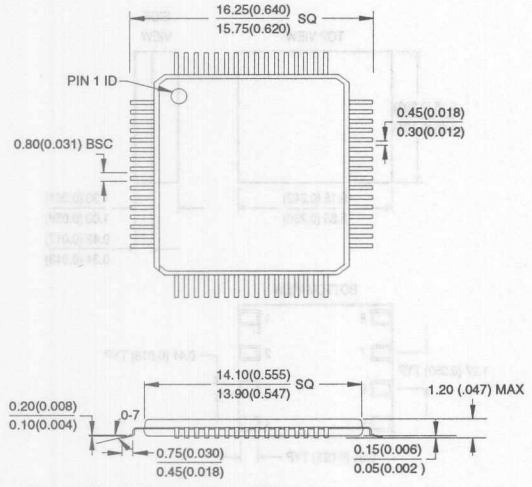
*Controlling dimension: millimeters

48A, 48-Lead, Low Profile (1.4 mm) Plastic Quad Flat Package (LQFP)
Dimensions in Millimeters and (Inches)*
JEDEC STANDARD MS-026 ACB



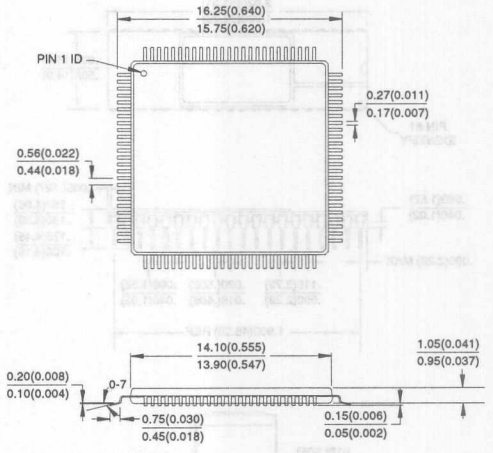
*Controlling dimension: millimeters

64A, 64-Lead, Thin (1.0 mm) Plastic Quad Flat Package (TQFP)
Dimensions in Millimeters and (Inches)*
JEDEC STANDARD MS-026 AEB



*Controlling dimension: millimeters

100A, 100-Lead, Thin (1.0 mm) Plastic Quad Flat Package (TQFP)
Dimensions in Millimeters and (Inches)*
JEDEC STANDARD MS-026 AED

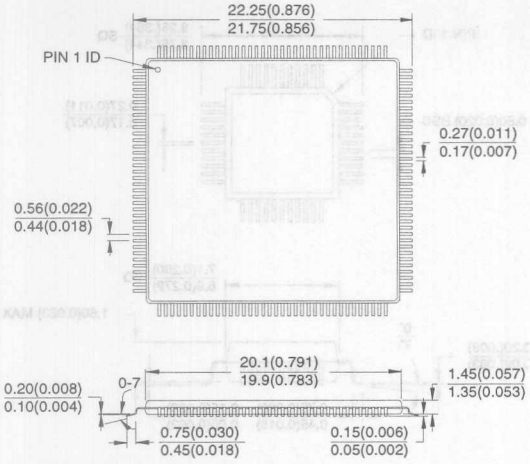


*Controlling dimension: millimeters

9

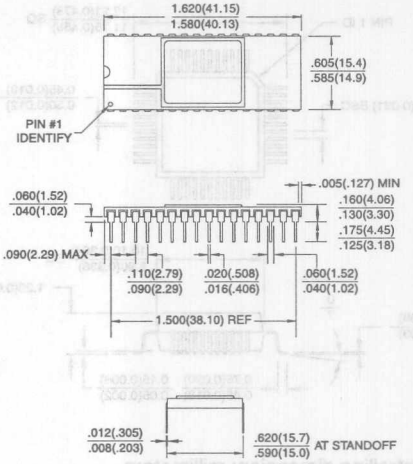
Packaging Information

144A, 144-Lead, Low Profile (1.4 mm) Plastic Quad Flat Package (LQFP)
Dimensions in Millimeters and (Inches)*
JEDEC STANDARD MS-026 BFB

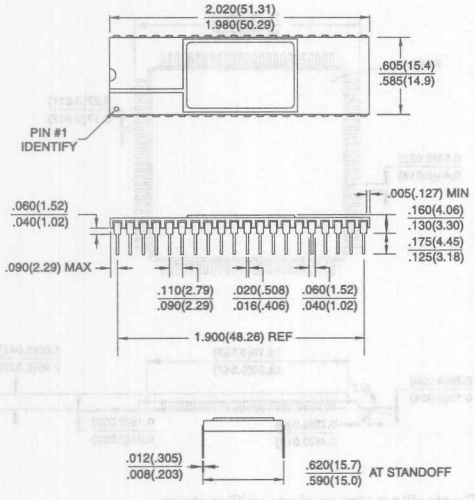


*Controlling dimension: millimeters

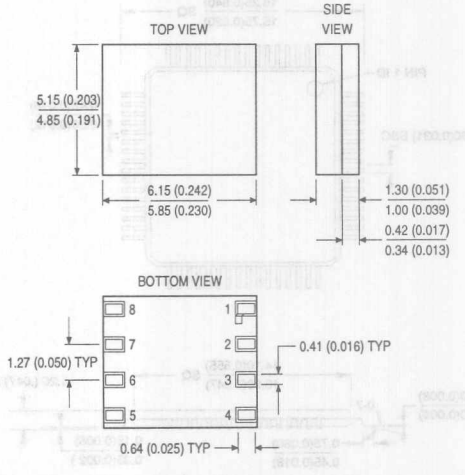
32B, 32-Lead, 0.600" Wide, Ceramic Side Braze Dual Inline (Side Braze)
Dimensions in Inches and (Millimeters)
MIL-STD-1835 D-16 CONFIG C



40B, 40-Lead, 0.600" Wide, Ceramic Side Braze Dual Inline (Side Braze)
Dimensions in Inches and (Millimeters)
MIL-STD-1835 D-5 CONFIG C



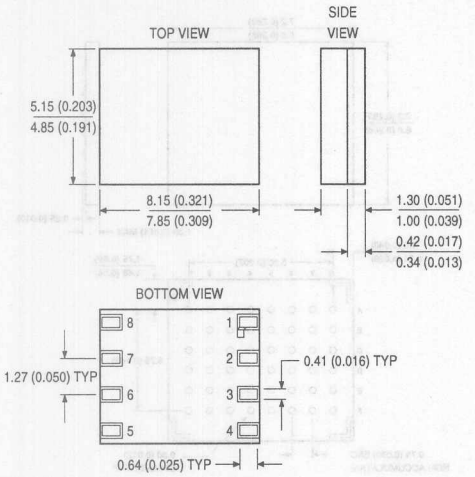
8C, 8-Lead,0.230" Wide, Leadless Array Package (LAP)
Dimensions in Millimeters and (Inches)*



* Controlling dimension: millimeters

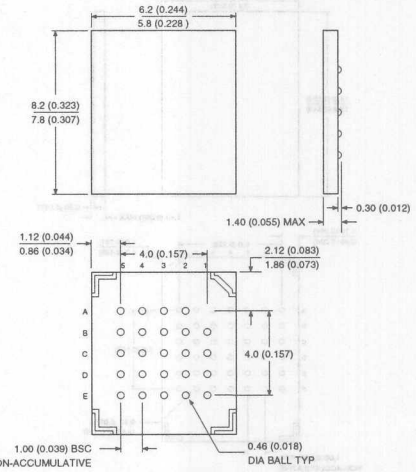
Packaging Information

8C1, 8-Lead 0.300" Wide, Leadless Array Package (LAP)
Dimensions in Millimeters and (Inches)*



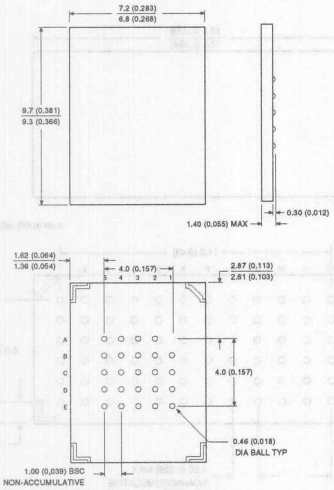
* Controlling dimension: millimeters

24C1, 24-Ball (5 x 5 Array), 1.0mm Pitch, 8 x 6mm Plastic Chip-Scale Ball Grid Array Package (CBGA)
Dimensions in Millimeters and (Inches)*



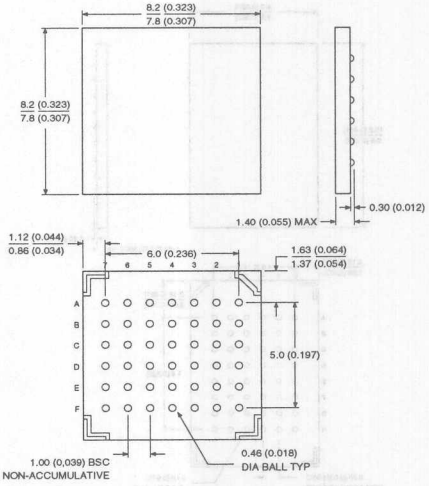
* Controlling dimension: millimeters

24C2, 24-Ball (5 x 5 Array), 1.0mm Pitch, 7 x 9.5mm Plastic Chip-Scale Ball Grid Array Package (CBGA)
Dimensions in Millimeters and (Inches)*



* Controlling dimension: millimeters

42C1, 42-Ball (7 x 6 Array), 1.0mm Pitch, 8 x 8mm Plastic Chip-Scale Ball Grid Array Package (CBGA)
Dimensions in Millimeters and (Inches)*

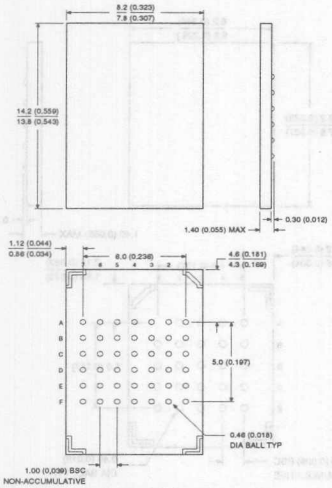


*Controlling dimension: millimeters

9

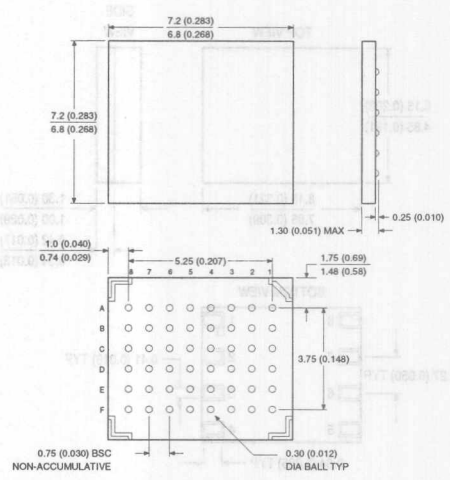
Packaging Information

42C2, 42-Ball (7 x 6 Array), 1.0mm Pitch, 8 x 14mm
Plastic Chip-Scale Ball Grid Array Package (CBGA)
Dimensions in Millimeters and (Inches)*



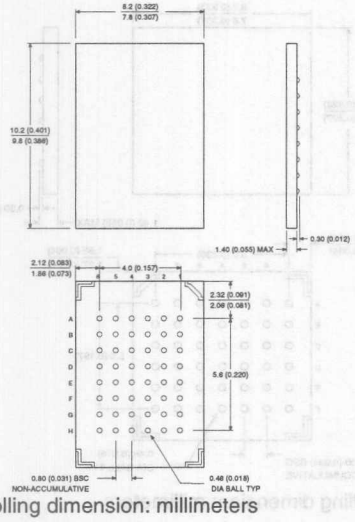
*Controlling dimension: millimeters

48C1, 48-Ball (8 x 6 Array), 0.75mm Pitch, 7 x 7mm
Plastic Chip-Scale Ball Grid Array Package (CBGA)
Dimensions in Millimeters and (Inches)*



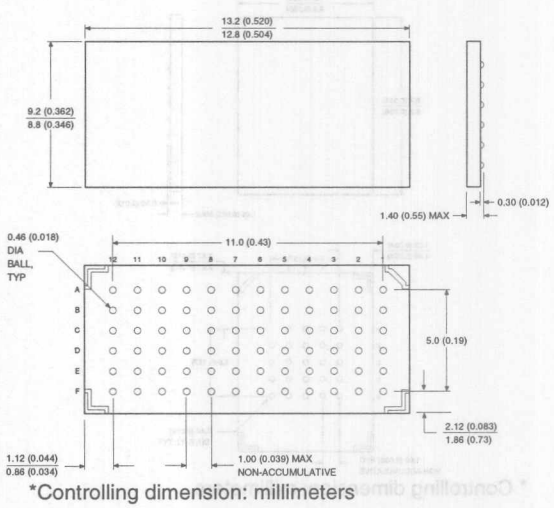
*Controlling dimension: millimeters

48C2, 48-Ball (6 x 8 Array), 0.80mm Pitch, 8 x 10mm
Plastic Chip-Scale Ball Grid Array Package (CBGA)
Dimensions in Millimeters and (Inches)*



*Controlling dimension: millimeters

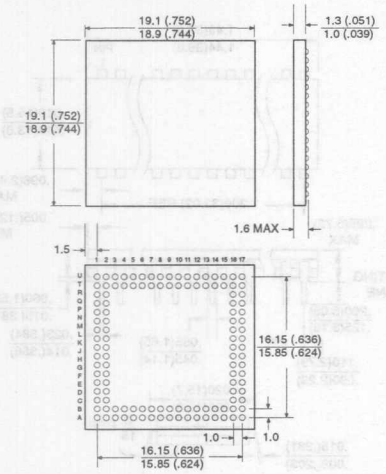
72C1, 72-Ball (12 x 6 Array), 1.0mm Pitch, 13 x 9mm
Plastic Chip-Scale Ball Grid Array Package (CBGA)
Dimensions in Millimeters and (Inches)*



*Controlling dimension: millimeters

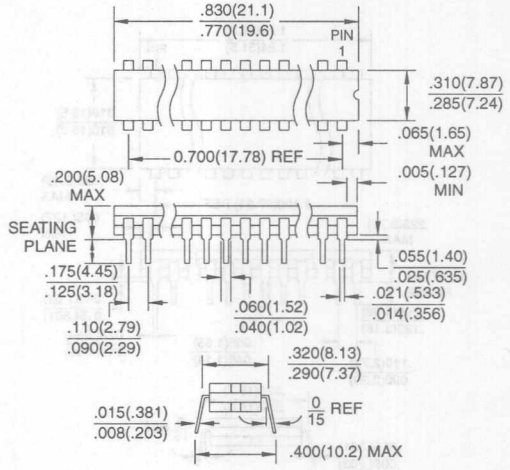
Packaging Information

120C1, 120-Ball (17 x 17 Array), 1.0 Pitch, 19 x 19mm
Ceramic Multi-Die Ball Grid Array Package (CerMBGA)
Dimensions in Millimeters and (Inches)*

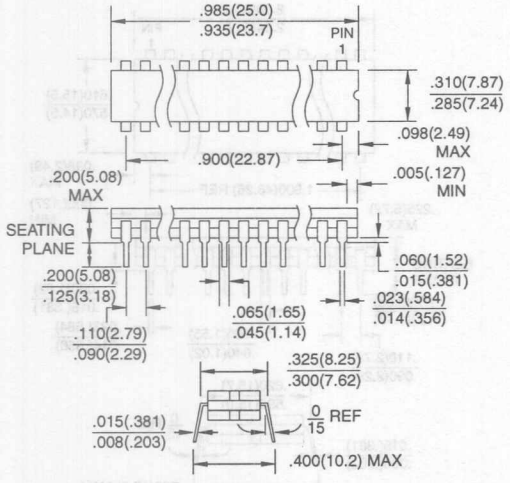


*Controlling dimension: millimeters

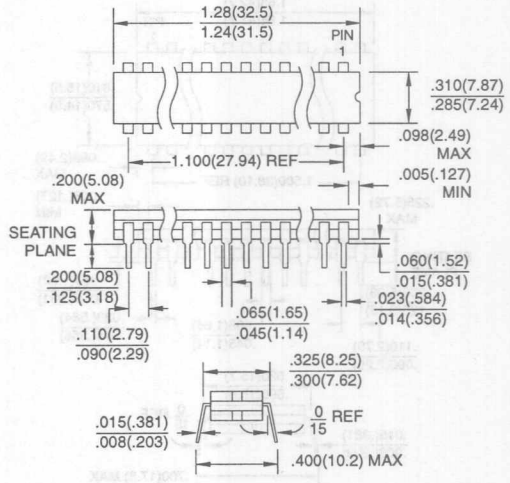
16D3, 16-Lead, 0.300" Wide, Non-Windowed,
Ceramic Dual Inline Package (Cerdip)
Dimensions in Inches and (Millimeters)
MIL-STD-1835 D-2 CONFIG A



20D3, 20-Lead, 0.300" Wide, Non-Windowed,
Ceramic Dual Inline Package (Cerdip)
Dimensions in Inches and (Millimeters)
MIL-STD-1835 D-8 CONFIG A

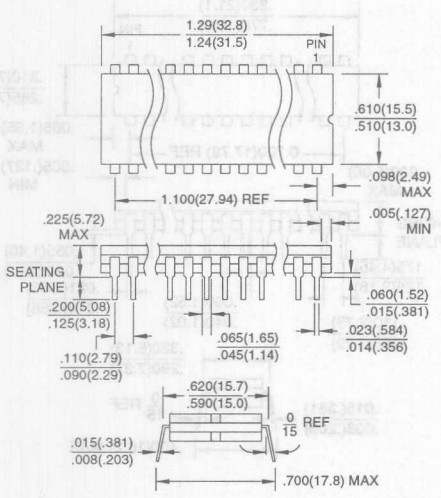


24D3, 24-Lead, 0.300" Wide, Non-Windowed,
Ceramic Dual Inline Package (Cerdip)
Dimensions in Inches and (Millimeters)
MIL-STD-1835 D-9 CONFIG A

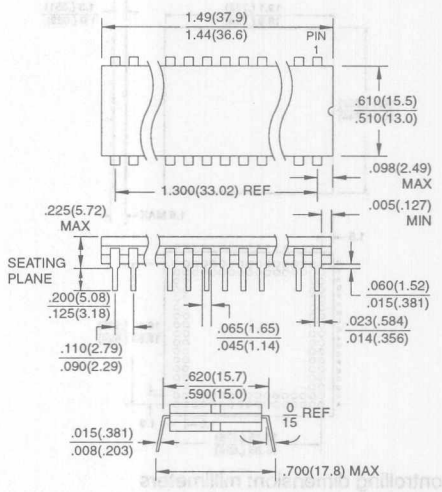


Packaging Information

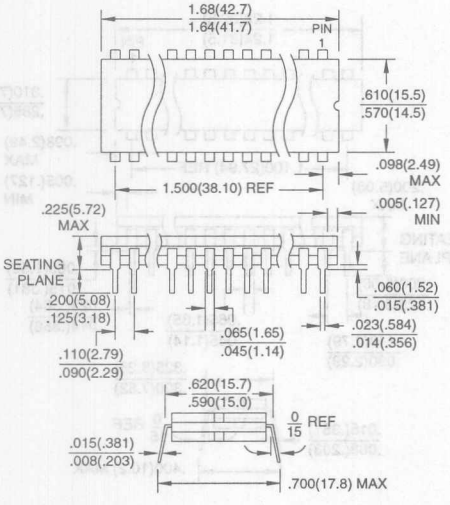
24D6, 24-Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
Dimensions in Inches and (Millimeters)
MIL-STD-1835 D-3 CONFIG A



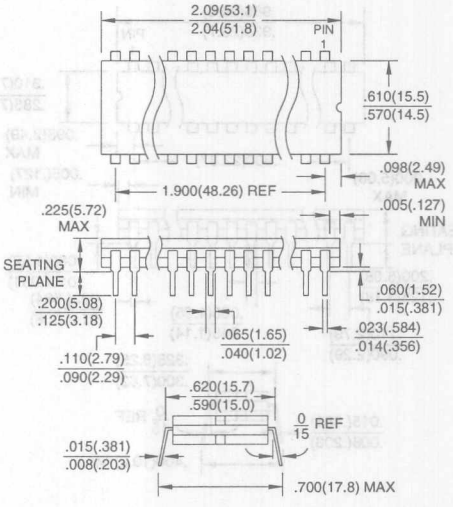
28D6, 28-Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
Dimensions in Inches and (Millimeters)
MIL-STD-1835 D-10 CONFIG A



32D6, 32-Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
Dimensions in Inches and (Millimeters)
MIL-STD-1835 D-16 CONFIG A

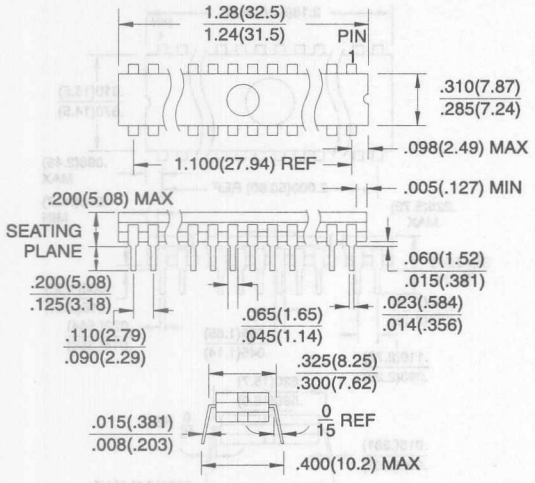


40D6, 40-Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
Dimensions in Inches and (Millimeters)
MIL-STD-1835 D-5 CONFIG A

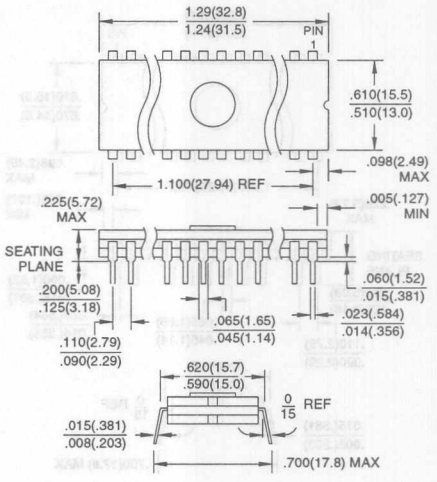


Packaging Information

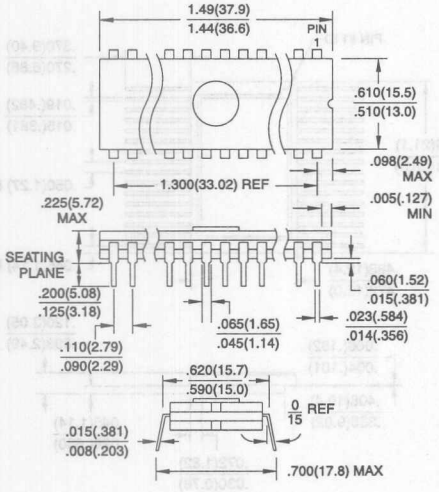
24DW3, 24-Lead, 0.300" Wide, WIndowed, Ceramic Dual Inline Package (Cerdip)
Dimensions in Inches and (Millimeters)
MIL-STD-1835 D-9 CONFIG A



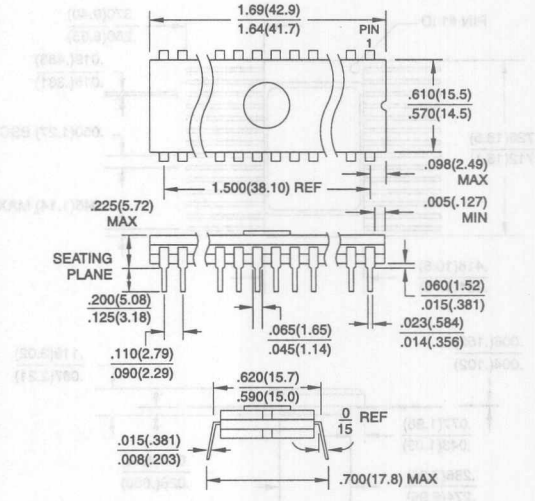
24DW6, 24-Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
Dimensions in Inches and (Millimeters)
MIL-STD-1835 D-3 CONFIG A



28DW6, 28-Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
Dimensions in Inches and (Millimeters)
MIL-STD-1835 D-10 CONFIG A



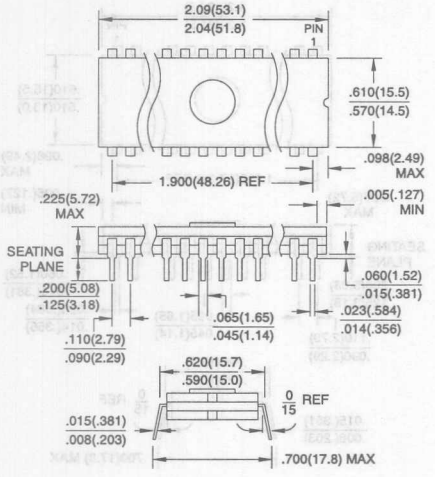
32DW6, 32-Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
Dimensions in Inches and (Millimeters)
MIL-STD-1835 D-16 CONFIG A



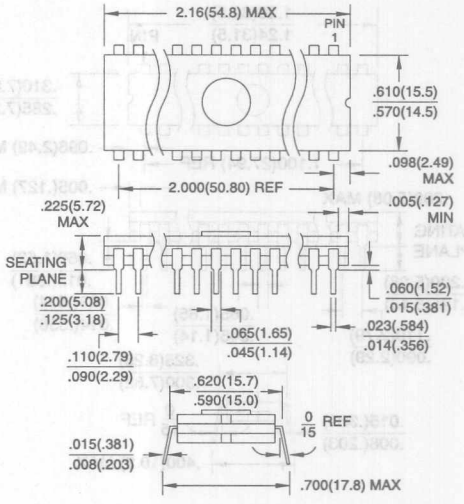
9

Packaging Information

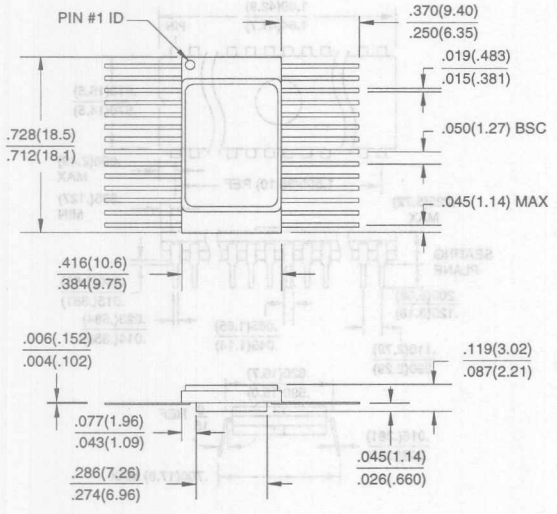
40DW6, 40-Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
Dimensions in Inches and (Millimeters)
MIL-STD-1835 D-5 CONFIG A



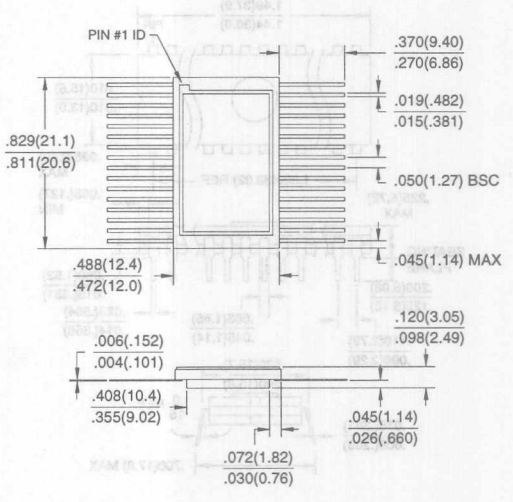
42DW6, 42-Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
Dimensions in Inches and (Millimeters)



28F, 28-Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)
Dimensions in Inches (Millimeters)
MIL-STD-1835 F-12 CONFIG B

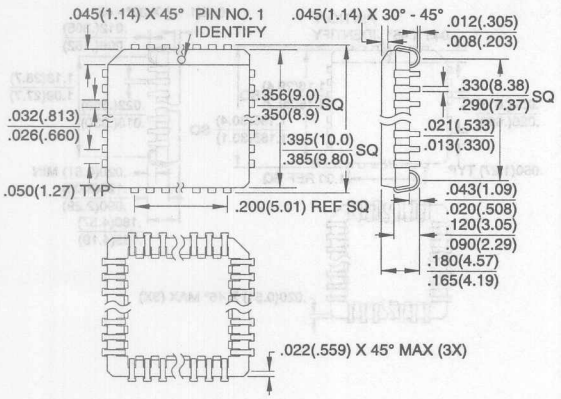


32F, 32-Lead, Non-WIndowed, Ceramic Bottom-Brazed Flat Package (Flatpack)
Dimensions in Inches and (Millimeters)
MIL-STD-1835 F-18 CONFIG B
JEDEC OUTLINE MO-115

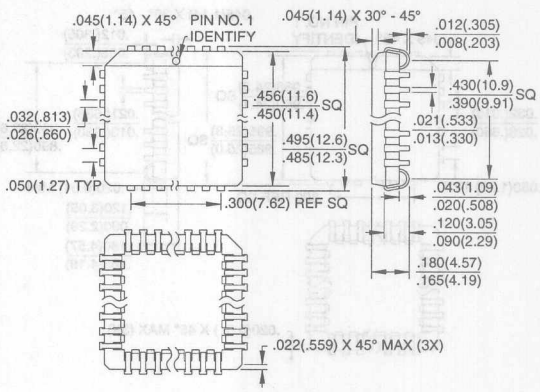


Packaging Information

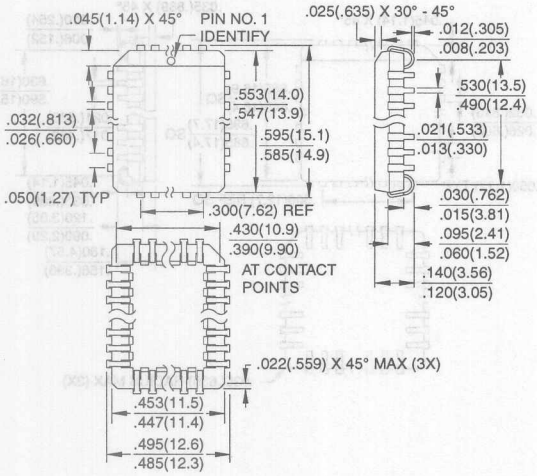
20J, 20-Lead, Plastic J-Leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-018 AA



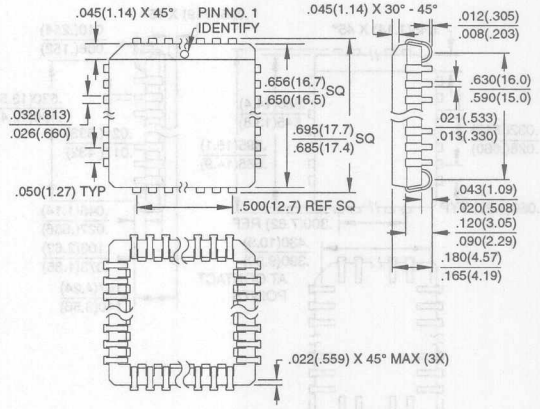
28J, 28-Lead, Plastic J-Leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-018 AB



32J, 32-Lead, Plastic J-Leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-016 AE



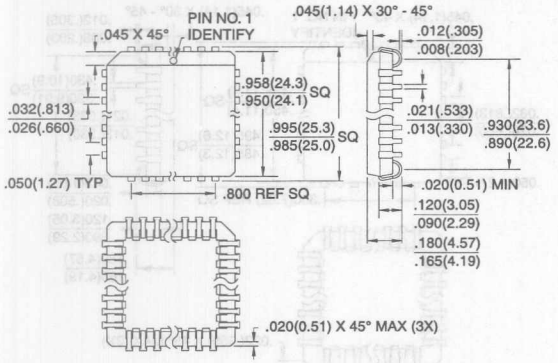
44J, 44-Lead, Plastic J-Leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-018 AC



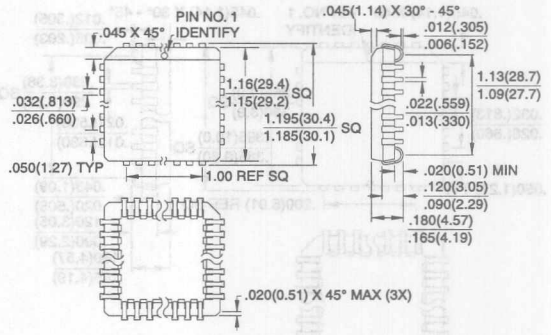
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Packaging Information

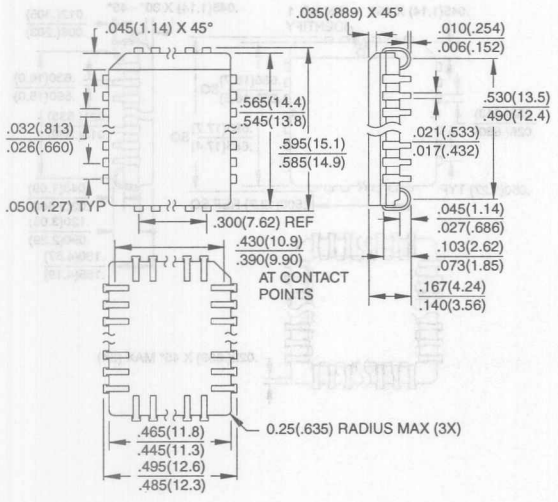
68J, 68-Lead, Plastic J-Leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-018 AE



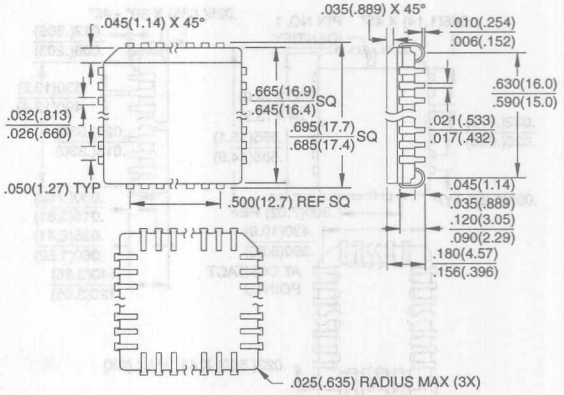
84J, 84-Lead, Plastic J-Leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-018 AF



32K, 32-Lead, Non-Windowed, Ceramic J-Leaded
Chip Carrier (JLCC)
Dimensions in Inches and (Millimeters)

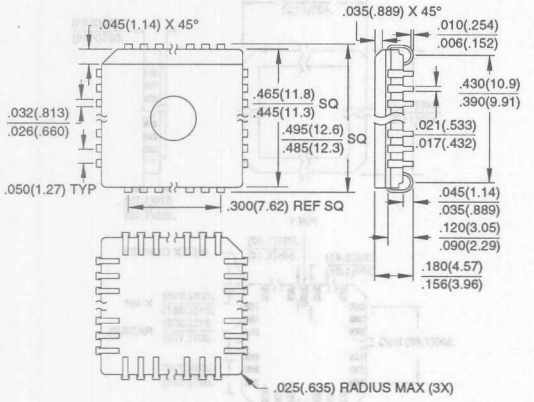


44K, 44-Lead, Non-Windowed, Ceramic J-Leaded
Chip Carrier (JLCC)
DImension in Inches and (Millimeters)

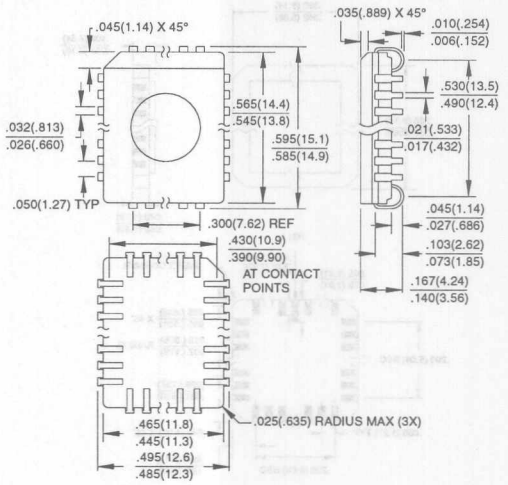


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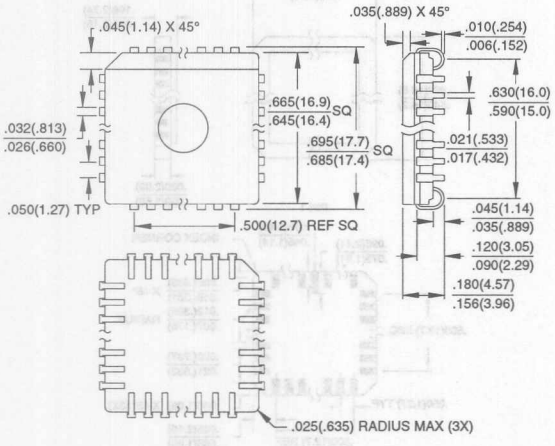
28KW, 28-Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
Dimensions in Inches and (Millimeters)
MIL-STD-1835 C-J7
JEDEC OUTLINE MO-087 AA



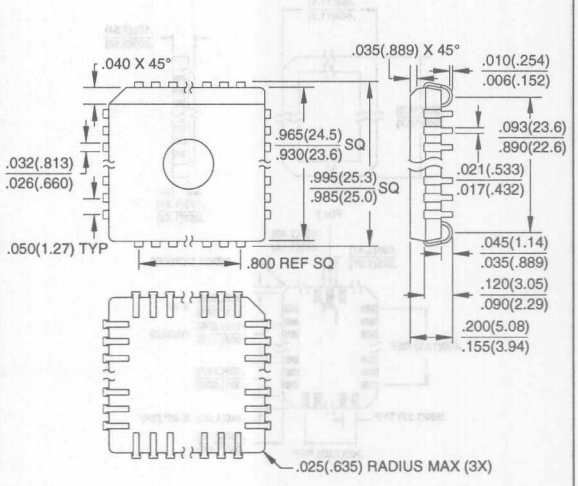
32KW, 32-Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
Dimensions and Inches and (Millimeters)



44KW, 44-Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
Dimensions in Inches and (Millimeters)
MIL-STD-1835 CJ1



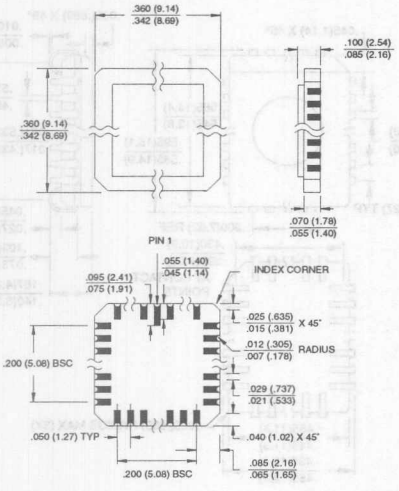
68KW, 68-Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
Dimensions in Inches and (Millimeters)
MIL-STD-1835 C-J2
JEDEC OUTLINE MO-087 AD



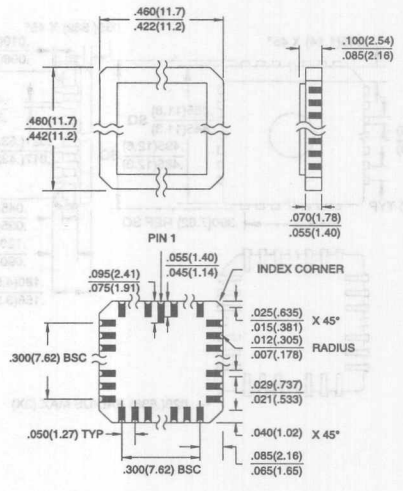
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Packaging Information

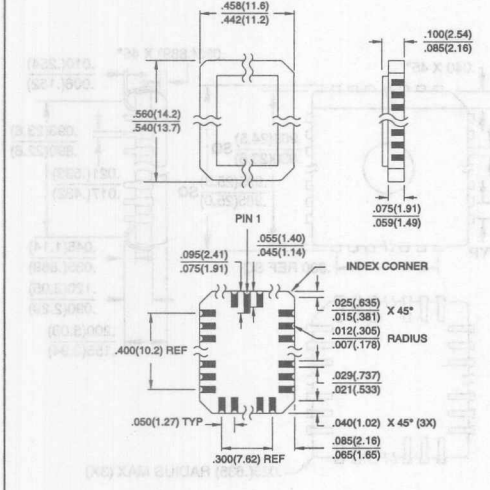
20L, 20-Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
Dimensions in Inches and (Millimeters)
MIL-STD-1835 C-2



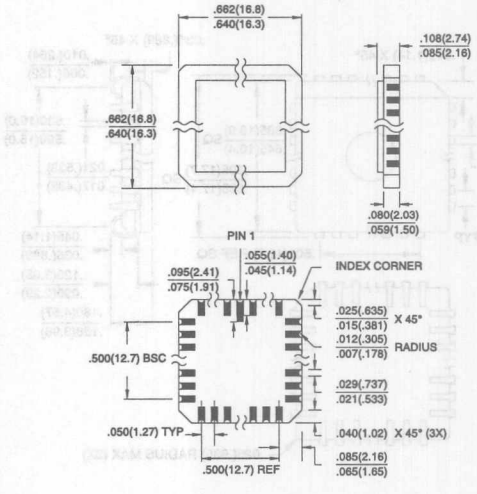
28L, 28-Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
Dimensions in Inches and (Millimeters)
MIL-STD-1835 C-4



32L, 32-Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
Dimensions in Inches and (Millimeters)
MIL-STD-1835 C-12

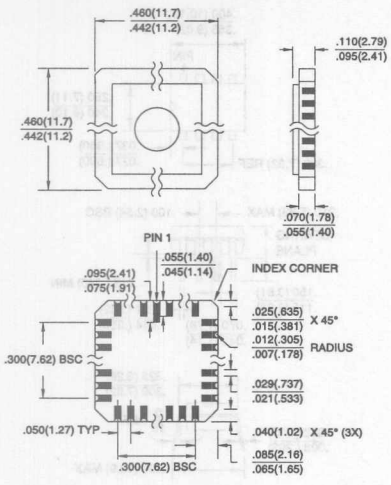


44L, 44-Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
Dimensions in Inches and (Millimeters)
MIL-STD-1835 C-5

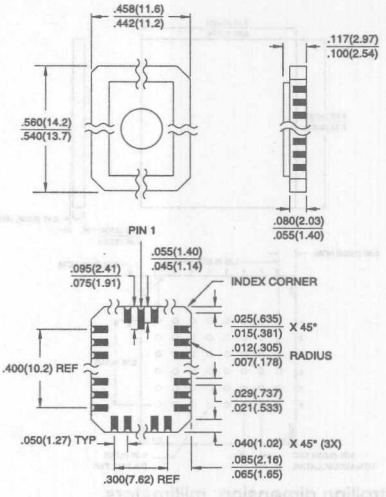


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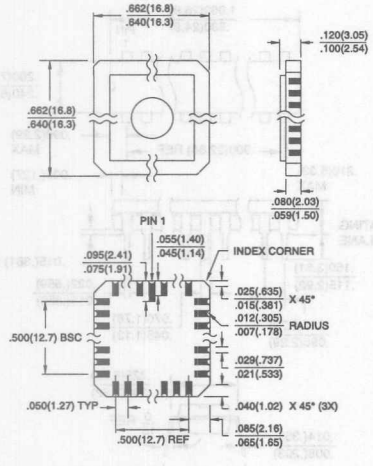
28LW, 28-Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
Dimensions in Inches and (Millimeters)
MIL-STD-1835 C-4



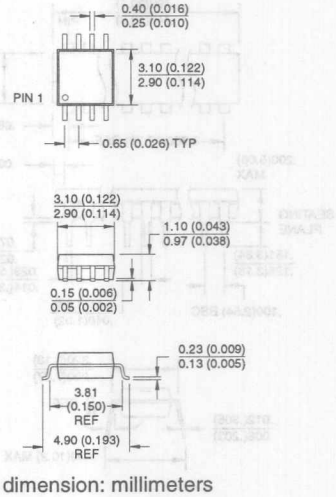
32LW, 32-Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
Dimensions in Inches and (Millimeters)
MIL-STD-1835 C-12



44LW, 44-Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
Dimensions in Inches and (Millimeters)
MIL-STD-1835 C-5



8M, 8-Lead, 0.118" Wide, Miniature Small Outline (MSOP)
Dimensions in Millimeters and (Inches)*

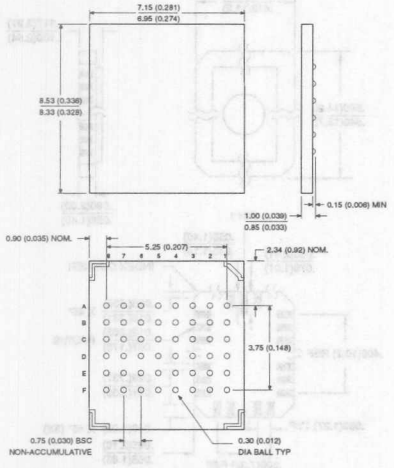


* Controlling dimension: millimeters

9

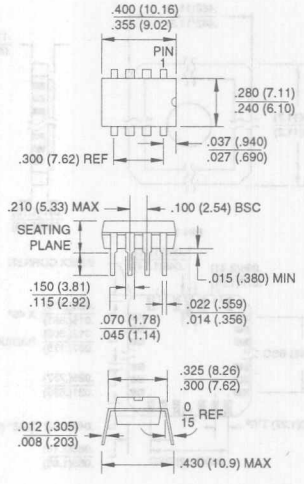
Packaging Information

48M1, 48-Ball, (8 x 6 Array), 0.75mm Pitch, Micro Ball Grid Array (mBGA)
Dimensions in Millimeters and (Inches)*

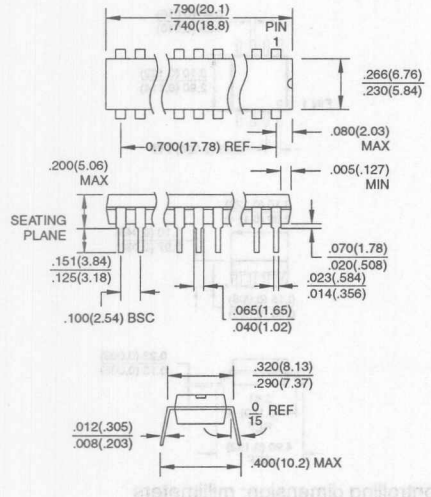


* Controlling dimension: millimeters

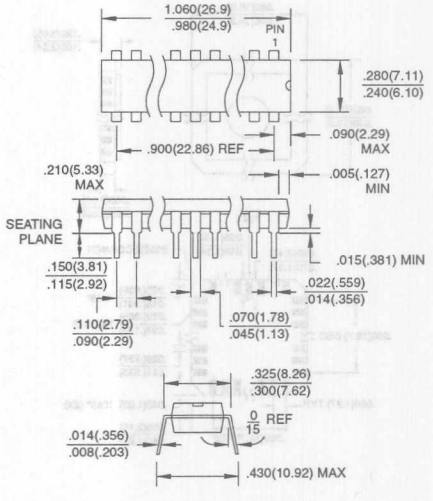
8P3, 8-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)



16P3, 16-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-001 BB

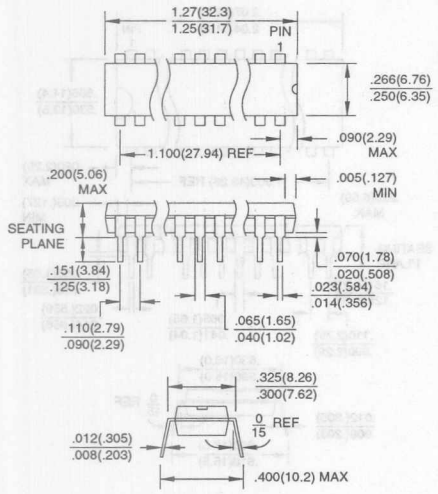


20P3, 20-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-001 AD

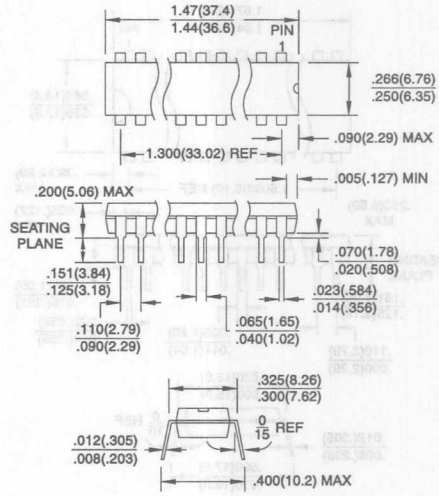


Packaging Information

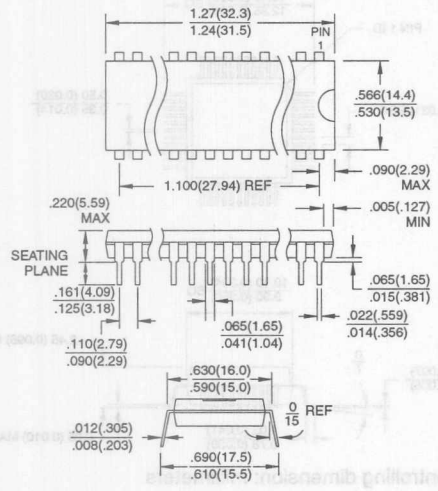
24P3, 24-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-001 AF



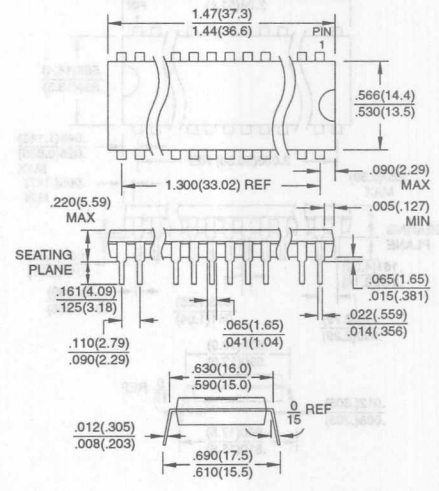
28P3, 28-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)



24P6, 24-Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-011 AA

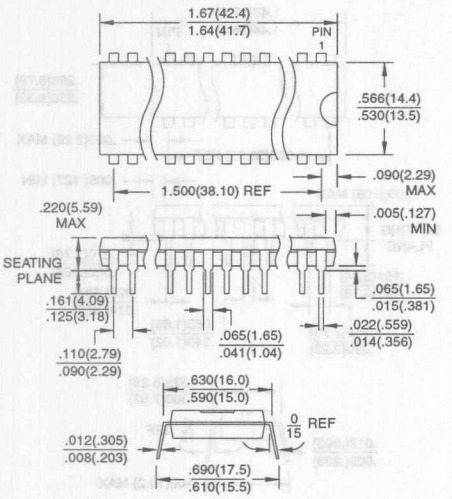


28P6, 28-Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-011 AB

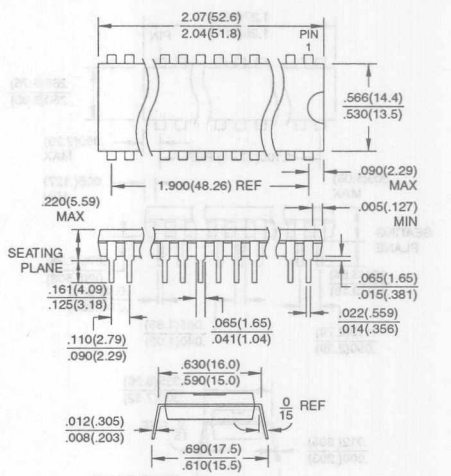


Packaging Information

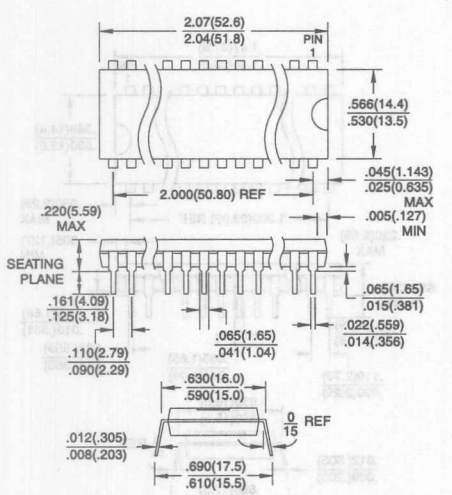
32P6, 32-Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)



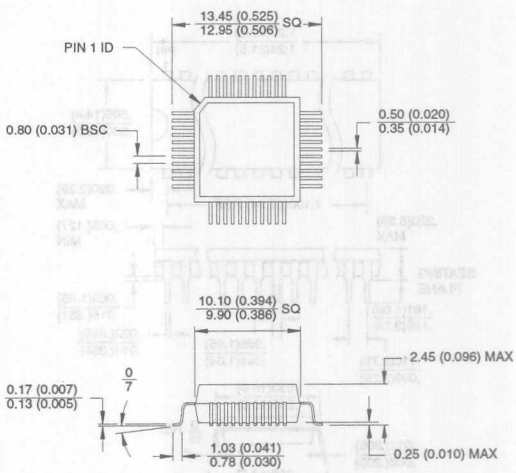
40P6, 40-Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-011 AC



42P6, 42-Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)



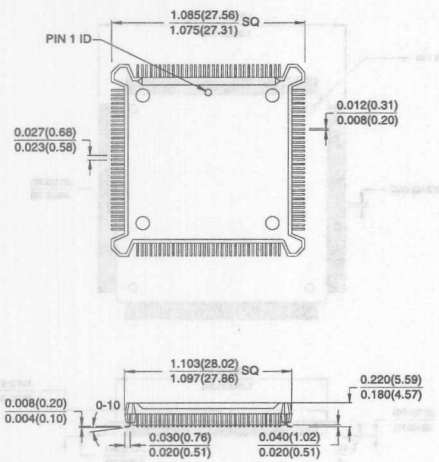
44Q, 44-Lead, Plastic Quad Flat Package (PQFP)
Dimensions in Millimeters and (Inches)*
JEDEC STANDARD MS-022 AB



* Controlling dimension: millimeters

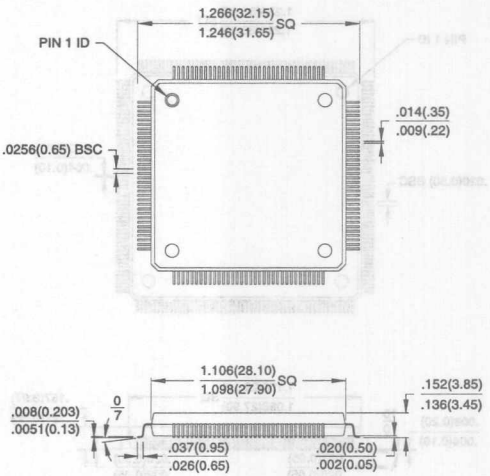
Packaging Information

132Q, 132-Lead, Bumpered Plastic Quad Flat Package (BQFP)
Dimensions in Millimeters and (Inches)*



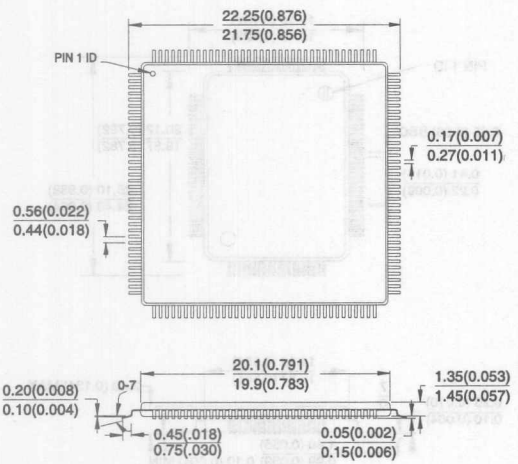
* Controlling dimension: millimeters

136Q, 136-Lead, Plastic Quad Flat Package (PQFP)
Dimensions in Millimeters and (Inches)*



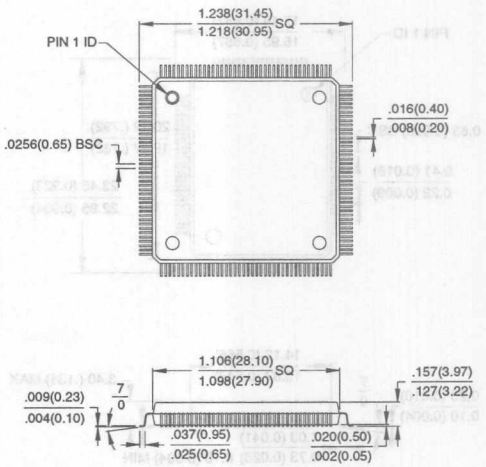
* Controlling dimension: millimeters

144Q, 144-Lead, Plastic Gull Wing Quad Flat Package (PQFP)
Dimensions in Millimeters and (Inches)*



* Controlling dimension: millimeters

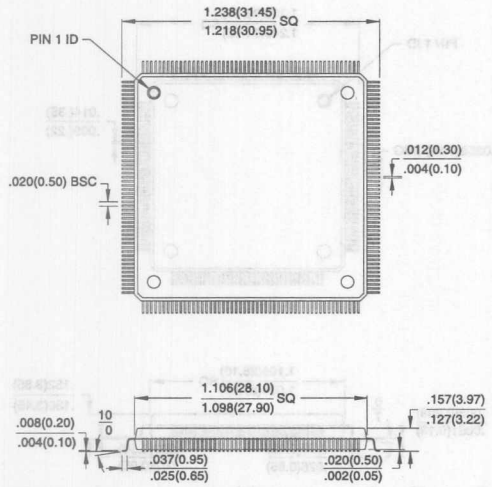
160Q, 160-Lead, Plastic Gull Wing Quad Flat Package (PQFP)
Dimensions in Millimeters and (Inches)*



* Controlling dimension: millimeters

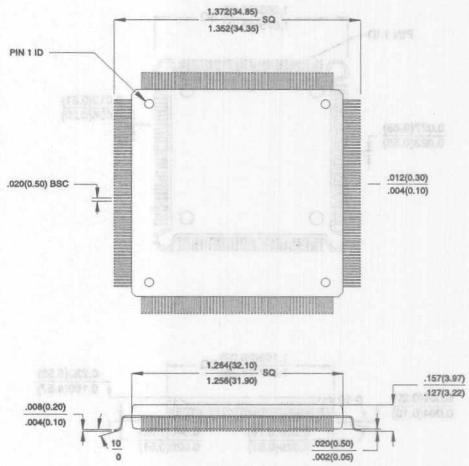
Packaging Information

208Q, 208-Lead, Plastic Gull Wing Quad Flat Package (PQFP)
Dimensions in Millimeters and (Inches)*



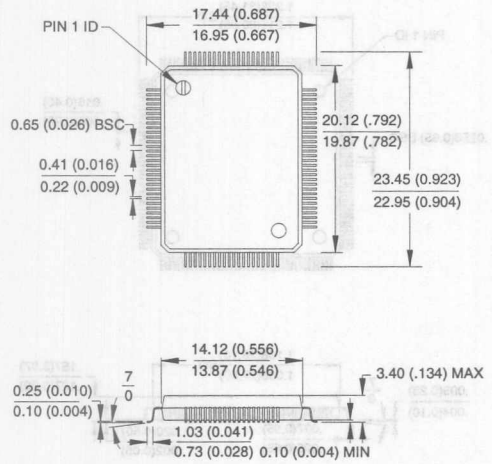
* Controlling dimension: millimeters

240Q, 240-Lead, Plastic Gull Wing Quad Flat Package (PQFP)
Dimensions in Millimeters and (Inches)*



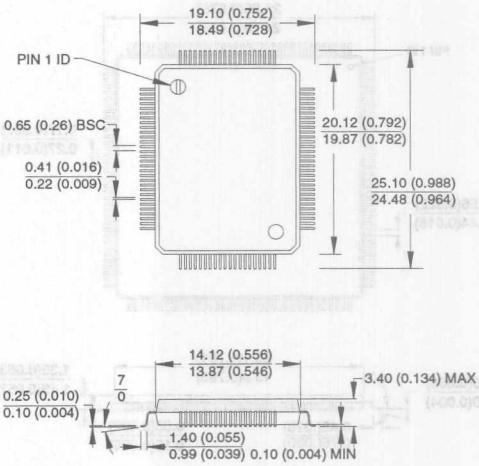
* Controlling dimension: millimeters

100Q1, 100-Lead Plastic Quad Flat Package (PQFP)
Body +3.2 mm Footprint
Dimensions in Millimeters and (Inches)*



* Controlling dimension: millimeters

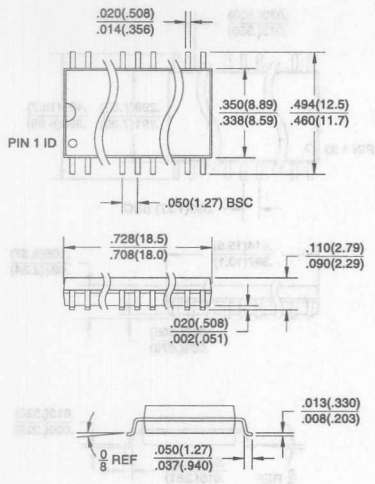
100Q2,100-Lead Plastic Quad Flat Package (PQFP)
Dimensions in Millimeters and (Inches)*



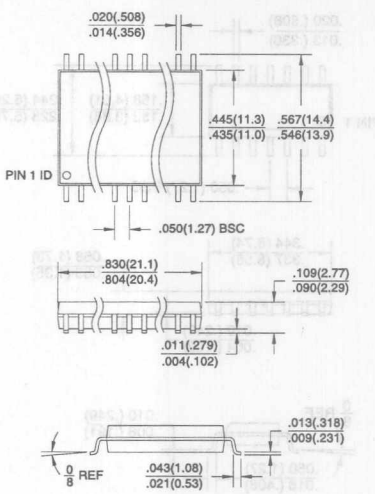
* Controlling dimension: millimeters

Packaging Information

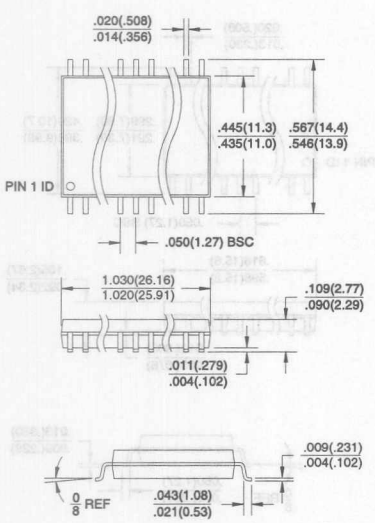
28R, 28-Lead, 0.330" Wide, Plastic Gull Wing Small Outline (SOIC)
Dimensions in Inches and (Millimeters)



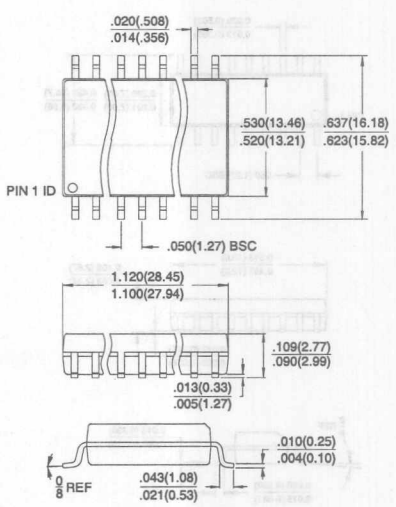
32R, 32-Lead, 0.440" Wide, Plastic Gull Wing Small Outline (SOIC)
Dimensions in Inches and (Millimeters)



40R, 40-Lead, 0.440" Wide, Plastic Gull Wing Small Outline (SOIC)
Dimensions in Inches and (Millimeters)



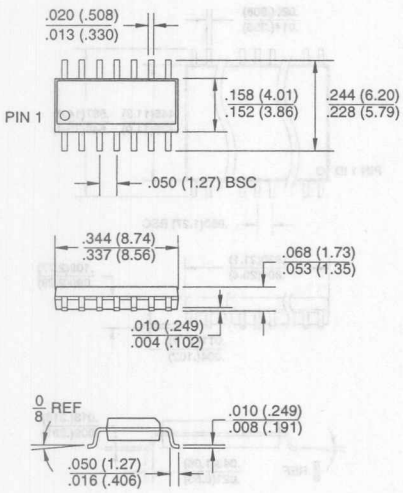
44R, 44-Lead, 0.525" Wide, Plastic Gull Wing Small Outline (SOIC)
Dimensions in Inches and (Millimeters)



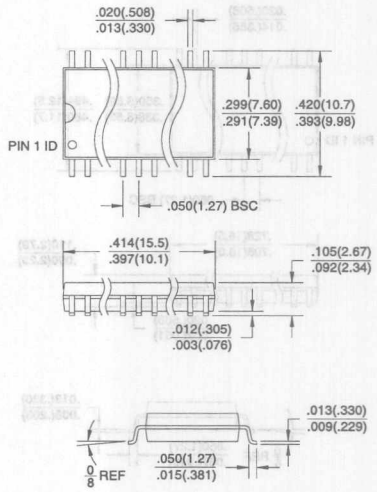
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Packaging Information

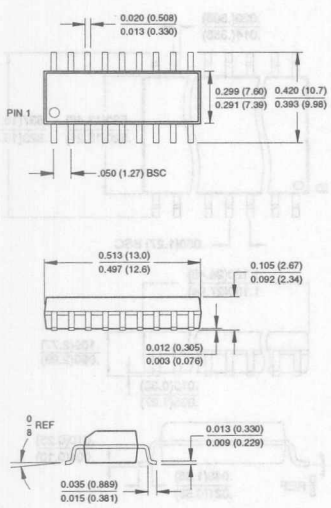
14S, 14-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
Dimensions in Inches and (Millimeters)



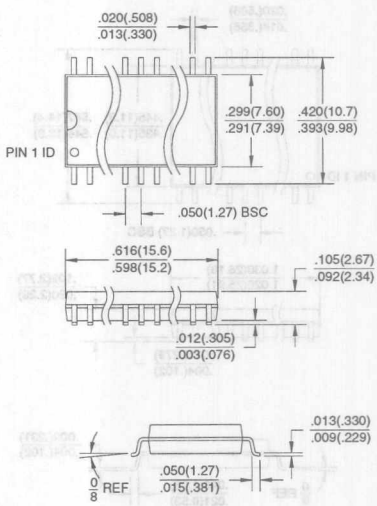
16S, 16-Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
Dimensions in Inches and (Millimeters)



20S, 20-Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
Dimensions in Inches and (Millimeters)

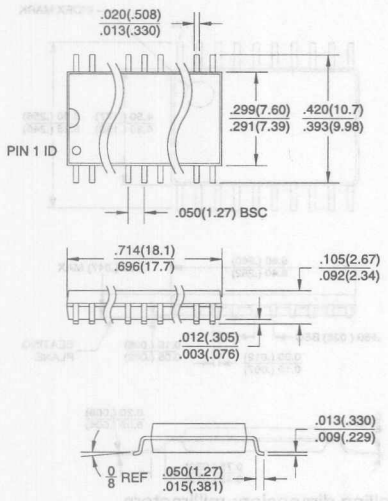


24S, 24-Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
Dimensions in Inches and (Millimeters)

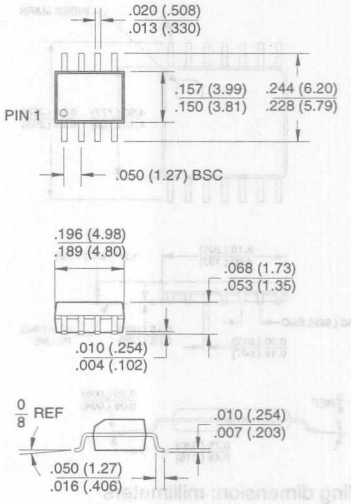


Packaging Information

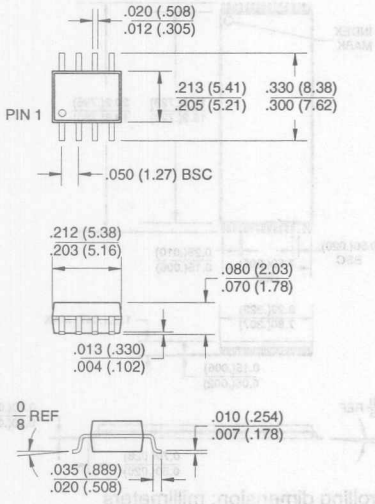
28S, 28-Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
Dimensions in Inches and (Millimeters)



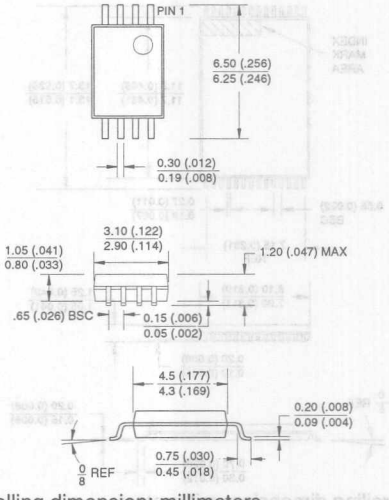
8S1, 8-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
Dimensions in Inches and (Millimeters)



8S2, 8-Lead, 0.210" Wide, Plastic Gull Wing Small Outline (EIAJ SOIC)
Dimensions in Inches and (Millimeters)



8T, 8-Lead, Plastic Thin Shrink Small Outline Package (TSSOP)
Dimensions in Millimeters and (Inches)*

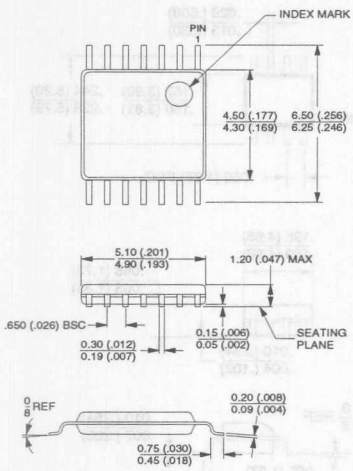


*Controlling dimension: millimeters

9

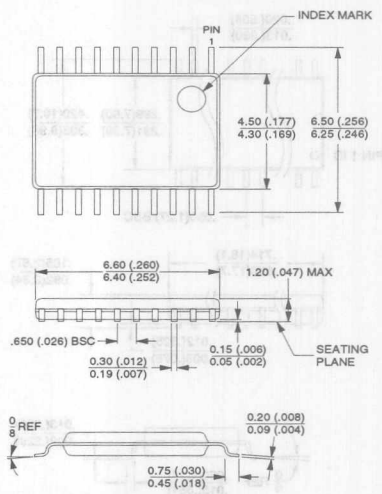
Packaging Information

14T, 14-Lead, 0.170" Wide, Thin Shrink Small Outline Package (TSSOP)
Dimensions in Millimeters and (Inches)*



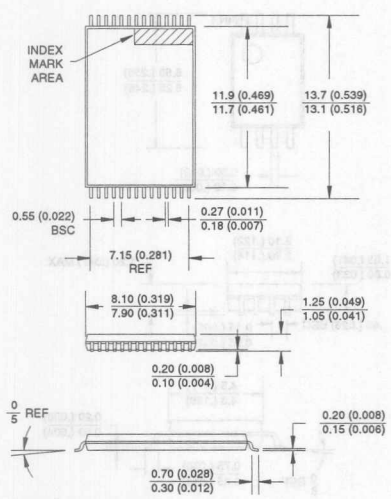
*Controlling dimension: millimeters

20T, 20-Lead, 0.170" Wide, Thin Shrink Small Outline Package (TSSOP)
Dimensions in Millimeters and (Inches)*



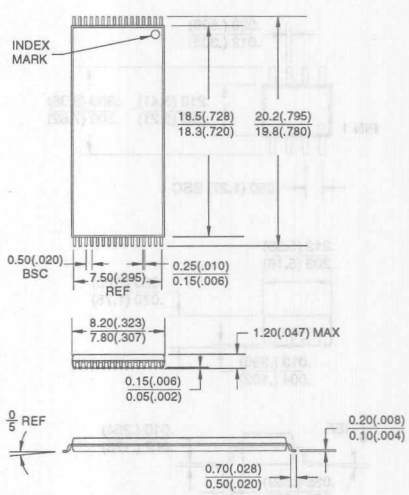
*Controlling dimension: millimeters

28T, 28-Lead, Plastic Thin Small Outline Package (TSOP)
Dimensions in Millimeters and (Inches)*



*Controlling dimension: millimeters

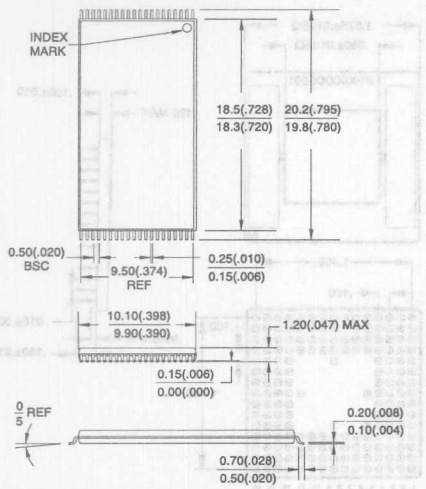
32T, 32-Lead, Plastic Thin Small Outline Package (TSOP)
Dimensions in Millimeters and (Inches)*
JEDEC OUTLINE MO-142 BD



*Controlling dimension: millimeters

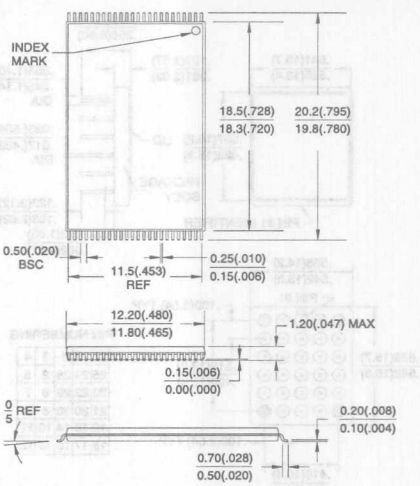
Packaging Information

40T, 40-Lead, Plastic Thin Small Outline Package (TSOP)
Dimensions in Millimeters and (Inches)*



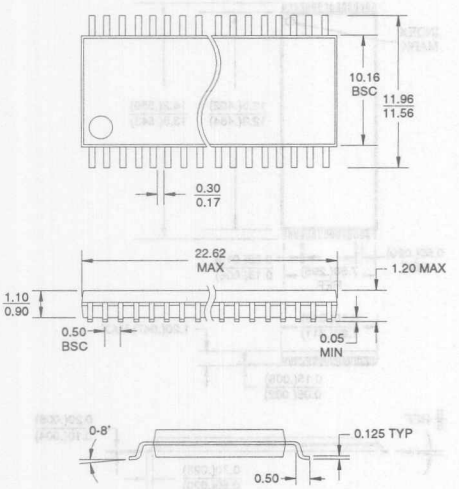
*Controlling dimension: millimeters

48T, 48-Lead, Plastic Thin Small Outline Package (TSOP)
Dimensions in Millimeters and (Inches)*
JEDEC OUTLINE MO-142 DD

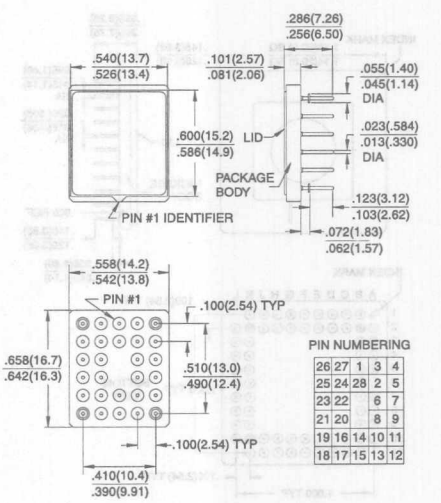


*Controlling dimension: millimeters

86T, 86-Lead, Plastic Thin Small Outline Package (TSOP Type II)
Dimensions in Millimeters



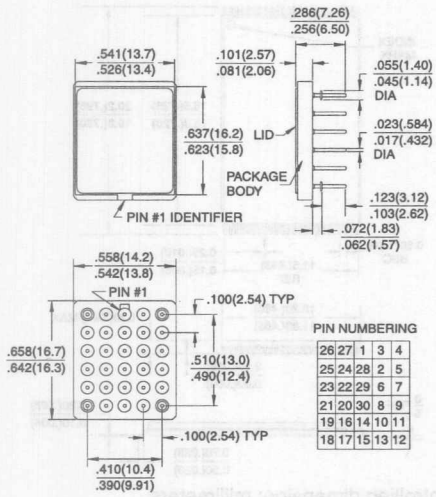
28U, 28-Pin, Ceramic Pin Grid Array (PGA)
Dimensions in Inches and (Millimeters)



9

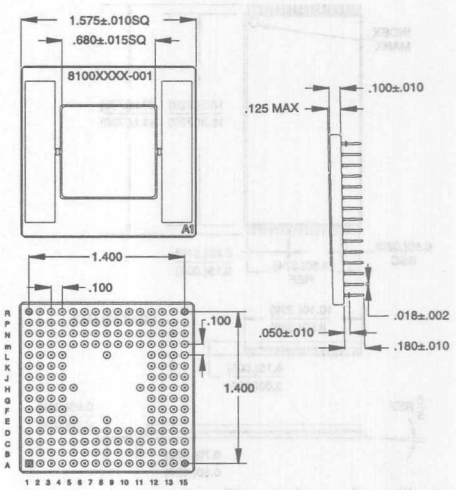
Packaging Information

30U, 30-Pin, Ceramic Pin Grid Array (PGA)
Dimensions in Inches and (Millimeters)

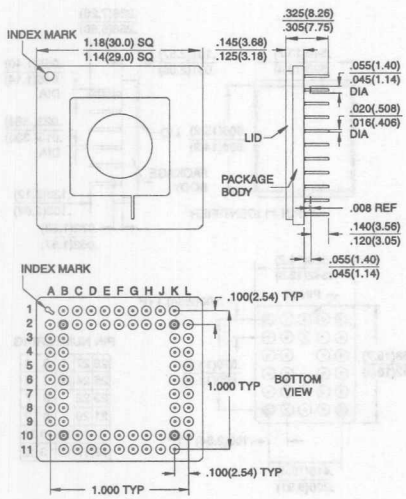


26	27	1	3	4
25	24	28	2	5
23	22	29	6	7
21	20	30	8	9
19	16	14	10	11
18	17	15	13	12

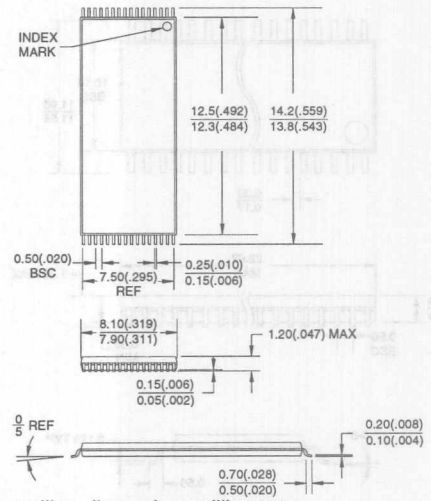
180U, 180-Pin, Ceramic Pin Grid Array (PGA)
Dimensions in Inches and (Millimeters)



68UW, 68-Pin, Ceramic Pin Grid Array (PGA)
Dimensions in Inches and (Millimeters)



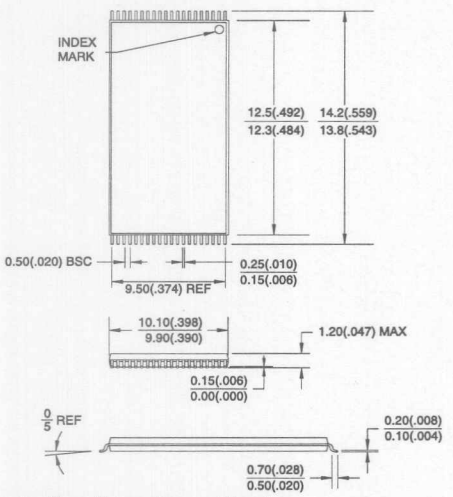
32V, 32-Lead, Plastic Thin Small Outline Package (TSOP)
Dimensions in Millimeters and (Inches)*



*Controlling dimension: millimeters

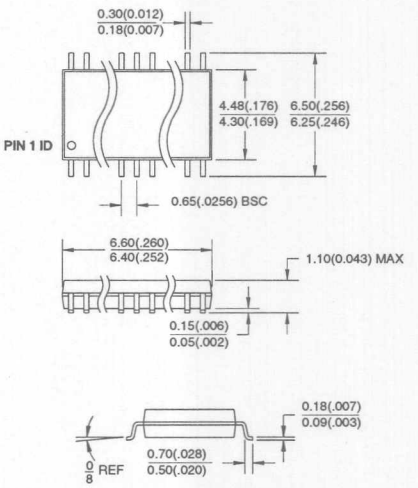
Packaging Information

40V, 40-Lead, Plastic Thin Small Outline Package (TSOP)
Dimensions in Millimeters and (Inches)*
JEDEC OUTLINE MO-142 CA



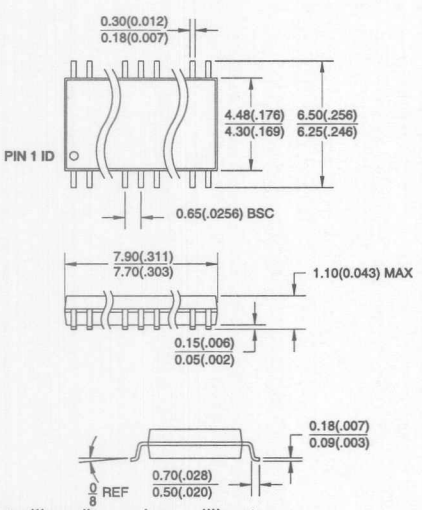
*Controlling dimension: millimeters

20X, 20-Lead, 4.4 mm Wide, Plastic Thin Shrink Small Outline (TSSOP)
Dimensions in Millimeters and (Inches)*



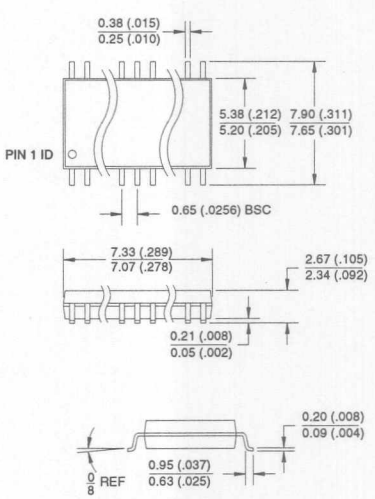
*Controlling dimension: millimeters

24X, 24-Lead, 4.4 mm Wide, Plastic Thin Shrink Small Outline (TSSOP)
Dimensions in Millimeters and (Inches)*



*Controlling dimension: millimeters

20Y, 20-Lead, 5.3 mm Wide, Plastic Shrink Small Outline (SSOP)
Dimensions in Millimeters and (Inches)*



*Controlling dimension: millimeters

9

Thermal Characteristics of Atmel Packages

The thermal performance of the semiconductor package is a very important consideration for the board designer. The reliability and functional life of the device is directly related to its junction operating temperature. As the temperature of the device increases, the stability of its junctions decline, as does its reliable life. The thermal performance is also important to the board design, because it may limit the board density, or dictate the board location of high power-dissipating devices, or require expensive cooling methods for the system. As devices have become more complex and boards have become denser, the need to account for the thermal characteristics of packages has shifted from being a minor consideration to being a necessary consideration.

The thermal performance of a package is measured by its ability to dissipate the power required by the device into its surroundings. The electrical power drawn by the device generates heat on the top surface of the die. This heat is conducted through the package to the surface and then transferred to the surrounding air by convection. Each heat transfer step has a corresponding resistance to the heat flow, which is given the value θ, the thermal resistance coefficient. Subscripts are added to the coefficient to specify the two points that the heat is transferred between. Commonly used coefficients are θ_{JA} (junction to ambient air), θ_{JC} (junction to package case), and θ_{CA} (case to ambient air).

An electrical analogy can be made, as shown in the figure below, to illustrate the heat flow of a package. The heat transfer can be characterized mathematically by the following equation,

$$Tj - Ta = P \times \theta_{JA}$$

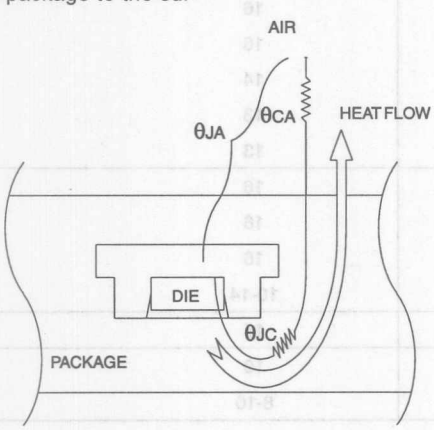
where,

P = Device operating power [watts]

Tj = Temperature of a junction on the device [°C]

Ta = Temperature of the surrounding ambient air [°C]

(continued)



Two conclusions can be made after examining this analogy. First, the lower the value of θ_{JA}, the better the heat dissipation of the package. Secondly, the value of θ_{JA} is directly dependent upon both the conductive (θ_{JC}) and convective (θ_{CA}) properties of the package. θ_{JC} is a function of the package material, the adhesion between the package materials, and device size. θ_{CA} is a function of the package size and configuration, package mounting method, and air flow across the package. Lower θ_{JA} values can be achieved by specifying ceramic packages instead of plastic packages, choosing larger packages, or improving air flow across the package.

The thermal resistance values of Atmel standard packages are listed on the following page. The figures shown are maximum values for θ, typical values are lower dependent upon the device type.

Thermal Resistance Coefficients

		θ_{JC} [°CW]	θ_{JA} [°CW] Airflow = 0 ft/min
Ceramic DIP	24D3/DW3	9	65
	24D6/DW6	10-15	45
	28D6/DW6	10-15	45
	32D6/DW6	10	45
	40D6/DW6	7	40
Plastic DIP	20P3	19	61
	24P3	22	82
	24P6	39	82
	28P6	36	77
	32P6	34	72
	40P6	30	68
Leadless Chip Carrier (LCC)	28L/LW	12	68
	32L/LW	10	65
	44L/LW	8-10	60
	68L/LW	6-8	50-60
Plastic Leaded Chip Carrier (PLCC)	20J	35	
	28J	16	60
	32J	16	60
	44J	14	50
	68J	13	45
	84J	13	32
J-Leaded Chip Carrier (JLCC)	28K/KW	16	72
	32K/KW	16	72
	44K/KW	16	68
	44K/KW	10-14	47
Cerpack	24C/CW	15	81
Flatpack	28F	10	65
	32F	8-10	60

Thermal Resistance Coefficients (Continued)

		θ_{JC} [°CW]	θ_{JA} [°CW] Airflow = 0 ft/min
PGA	28U	10	65
	30U	10	65
Sidebraze	32S	8-10	40-50
SOIC	20S	17	88
	24S	17	77
PQFP	44Q	15	60
	100Q	12	42
	160Q	8	37
TQFP	44A	17	62
	100A	10	50
TSOP	28T	66	141
	32T	45	113
	40T	35	95
	40(V)	55	130
	48T	30	82
TSSOP	20X		
	24X		
	28X		

		θ_{JC} [°C/W]	θ_{JA} [°C/W] Airflow = 0 ft/min
PDIP	300	10	55
	600	10	55
Sidebraze	325	8-10	40-50
SOIC	209	17	88
	246	17	77
PQFP	44Q	15	80
	100Q	12	42
	160Q	8	37
TQFP	44A	17	62
	100A	10	50
TSOP	28T	66	141
	32T	45	113
	40T	35	95
	40(V)	55	130
	48T	30	82
TSSOP	20X		
	24X		
	28X		

Available Packing Methods and Quantities

Atmel provides four different packing methods to provide maximum protection for our product and to best suit our customer's needs: 1) Shipping Tubes, 2) Shipping Trays, 3) Unit Packing, and 4) Tape and Reel. These first three methods are our standard pack, but we also provide tape and reel upon customer request.

1. Shipping Tubes

- **Material: Clear polyvinyl chloride**
- **ESD: Topically coated with anti-static solution**

Quantity Per Tube

Package	Lead Count	Package Code	Quantity/Tube
Cerdip (300 mil)	16	D3/DW3	24
	20	D3/DW3	19
	24	D3/DW3	15
Cerdip (600 mil)	24	D6/DW6	16
	28	D6/DW6	14
	32	D6/DW6	12
	40	D6/DW6	10
	42	DW6	9
Flatpack	28	F	15
	32	F	15
LCC	20	L/LW	54
	28	L/LW	42
	32	L/LW	34
	44	L/LW	29
Plastic Dip (300 mil)	8	P3	50
	20	P3	19
	24	P3	15
Plastic Dip (600 mil)	24	P6	16
	28	P6	14
	32	P6	12
	40	P6	10
	42	P6	10
PLCC	20	J	48
	28	J	38
	32	J	32
	44	J	27

(continued)

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Quantity Per Tube (Continued)

Package	Lead Count	Package Code	Quantity/Tube
SOIC (150 mil)	8	S1	100
	14	S	56
SOIC (210 mil)	8	S2	94
SOIC (300 mil)	20	S	31
	24	S	31
	28	S	27
SOIC (330 mil)	28	R	26
	32	R	22
SOIC (450 mil)	32	R	23
Sidebraze	32	B	12

2. Shipping Trays

- **Conforms to JEDEC Thin Matrix Tray outlines**
- **Bakeable and Conductive**

Quantity Per Tray

Package	Lead Count	Package Code	Quantity/Tray
TSOP	28	T	234
	32	T	156
	40	T	120
	40	V	160
	48	T	96

3. Unit Pack/Boxes

- **In order to maximize protection, each unit is packed in specially designed carriers/boxes.**

Quantity Per Unit Pack/Box

Package	Lead Count	Package Code	Method	Quantity
Pin Grid Array	28	U	Box	20
	30	U	Box	20

4. Tape and Reel

- Meets or exceeds the requirements of EIA-481-x, Carrier Taping of SMC for Automated Handling
- Material: Carrier Tape = Black, conductive PVC or polystyrene
  Cover Tape = Clear, anti-static polyester film
  Reel = 13 inch diameter plastic reel; 7 inch diameter plastic reel used for 500 piece quantities
- Each reel is individually packed into its own box, with a bar code label attached to both the reel and box

Quantity Per Reel

Package	Lead Count	Package Code	Width	Pitch	Quantity
PLCC	28	J	24 mm	16 mm	750
	32	J	24 mm	16 mm	750
	44	J	32 mm	24 mm	500
SOIC(150 mil)	8	S1	12 mm	8 mm	Up to 3000 in 500 piece increments
	14	S	12 mm	8 mm	
SOIC (210 mil)	8	S2	16 mm	12 mm	Up to 2000 in 500 piece increments
SOIC (300 mil)	20	S	24 mm	12 mm	1000
	24	S	24 mm	12 mm	1000
	28	S	24 mm	12 mm	1000
SOIC (330 mil)	28	R	24 mm	16 mm	1000
TSOP	28	T	24 mm	12 mm	2000
	32	T	32 mm	16 mm	1500
	40	T	32 mm	16 mm	1250

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Data Memory Selection Guide

DataFlash®

Part Number	Speed	Density	Description	Availability
Battery-Voltage **(2.7V to 3.6V)**				
AT45DB011	13 MHz	1M bit	2.7-Volt Only Serial Interface Flash with One 264-Byte SRAM Buffer	Now
AT45DB021	5 MHz	2M bit	2.7-Volt Only Serial-Interface Flash with Two 264-Byte SRAM Buffers	Now
AT45DB041	5 MHz	4M bit	2.7-Volt Only Serial-Interface Flash with Two 264-Byte SRAM Buffers	Now
AT45DB080	2 MHz	8M bit	2.7-Volt Only Sequential Access Parallel I/O Flash with Two 264-Byte SRAM Buffers	Now
AT45DB081	10 MHz	8M bit	2.7-Volt Only Serial-Interface Flash with Two 264-Byte SRAM Buffers	Now
AT45DB161	13 MHz	16M bit	2.7-Volt Only Serial-Interface Flash with Two 528-Byte SRAM Buffers	Now
AT45DB321	13 MHz	32M bit	2.7-Volt Only Serial Interface Flash with Two 528-Byte SRAM Buffers	4Q98
Standard Voltage (5.0V)				
AT45D011	15 MHz	1M bit	5.0-Volt Only Serial Interface Flash with One 264-Byte SRAM Buffer	Now
AT45D021	10 MHz	2M bit	5.0-Volt Only Serial-Interface Flash with Two 264-Byte SRAM Buffers	Now
AT45D041	10 MHz	4M bit	5.0-Volt Only Serial-Interface Flash with Two 264-Byte SRAM Buffers	Now
AT45D081	10 MHz	8M bit	5.0-Volt Only Serial-Interface Flash with Two 264-Byte SRAM Buffers	Now
AT45D161	15 MHz	16M bit	5.0-Volt Only Serial-Interface Flash with Two 528-Byte SRAM Buffers	Now
AT45D321	15 MHz	32M bit	2.7-Volt Only Serial Interface Flash with Two 528-Byte SRAM Buffers	4Q98

FPGA Serial Configuration EEPROM

Part Number	Memory Size	Description	Availability
Standard Voltage (5.0V)			
AT17C65	65,536 x 1	65K-bit FPGA Configuration EEPROM	Now
AT17C65A	65,536 x 1	65K-bit FPGA Configuration EEPROM, Altera pinout	Now
AT17C128	131,072 x 1	128K-bit FPGA Configuration EEPROM	Now
AT17C256	262,144 x 1	256K-bit FPGA Configuration EEPROM	Now
AT17C256A	262,144 x 1	256K-bit FPGA Configuration EEPROM, Altera pinout	Now
AT17C512	524,288 x 1	512K-bit FPGA Configuration EEPROM	Now
AT17C512A	524,288 x 1	512K-bit FPGA Configuration EEPROM, Altera pinout	Now
AT17C010	1,048,576 x 1	1M-bit FPGA Configuration EEPROM	Now
AT17C010A	1,048,576 x 1	1M-bit FPGA Configuration EEPROM, Altera pinout	Now
Low-Voltage (3.3V)			
AT17LV65	65,536 x 1	65K-bit FPGA Configuration EEPROM, 3.3-Volt	Now
AT17LV65A	65,536 x 1	65K-bit FPGA Configuration EEPROM, 3.3-Volt, Altera pinout	Now
AT17LV128	131,072 x 1	128K-bit FPGA Configuration EEPROM, 3.3-Volt	Now
AT17LV256	262,144 x 1	256K-bit FPGA Configuration EEPROM, 3.3-Volt	Now
AT17LV256A	262,144 x 1	256K-bit FPGA Configuration EEPROM, 3.3-Volt, Altera pinout	Now
AT17LV512	524,288 x 1	512K-bit FPGA Configuration EEPROM, 3.3-Volt	Now
AT17LV512A	524,288 x 1	512K-bit FPGA Configuration EEPROM, 3.3-Volt, Altera pinout	Now

FPGA Serial Configuration EEPROM (Continued)

Part Number	Memory Size	Description	Availability
AT17LV010	1,048,576 x 1	1M-bit FPGA Configuration EEPROM, 3.3-Volt	Now
AT17LV010A	1,048,576 x 1	1M-bit FPGA Configuration EEPROM, 3.3-Volt, Altera pinout	Now

Parallel EEPROMs

Part Number	Organization	Speeds	Description	Availability
High-Speed				
AT28HC64B	8K x 8	55-120 ns	64K-bit EEPROM with 64-Byte Page & Software Data Protection	Now
AT28HC256	32K x 8	70-120 ns	256K-bit EEPROM with 64-Byte Page & Software Data Protection	Now
AT28HC256E	32K x 8	70-120 ns	256K-bit EEPROM with Extended Endurance	Now
AT28HC256F	32K x 8	70-120 ns	256K-bit EEPROM with Fast Write	Now
Battery-Voltage **(2.7V to 3.6V)**				
AT28BV16	2K x 8	200-250 ns	16K-bit EEPROM, 2.7-Volt	Now
AT28BV64	8K x 8	200-250 ns	64K-bit EEPROM, 2.7-Volt	Now
AT28LV010	128K x 8	200-250 ns	1M-bit EEPROM with 128-Byte Page & Software Data Protection, 3.0-Volt	Now
AT28BV64B	8K x 8	200-250 ns	64K-bit EEPROM with 64-Byte Page & Software Data Protection, 2.7-Volt	Now
AT28BV256	32K x 8	200-250 ns	256K-bit EEPROM with 64-Byte Page & Software Data Protection, 2.7-Volt	Now
Standard Voltage (5.0V)				
AT28C16	2K x 8	150 ns	16K-bit EEPROM	Now
AT28C16E	2K x 8	150 ns	16K-bit EEPROM with Extended Endurance & Fast Write	Now
AT28C17	2K x 8	150 ns	16K-bit EEPROM with Ready/Busy	Now
AT28C17E	2K x 8	150 ns	16K-bit EEPROM with Ready/Busy & Extended Endurance & Fast Write	Now
AT28C64	8K x 8	120-250 ns	64K-bit EEPROM	Now
AT28C64E	8K x 8	120-250 ns	64K-bit EEPROM with Extended Endurance & Fast Write	Now
AT28C64X	8K x 8	120-250 ns	64K-bit EEPROM without Ready/Busy	Now
AT28C64B	8K x 8	150-250 ns	64K-bit EEPROM with 64-Byte Page & Software Data Protection	Now
AT28C256	32K x 8	150-250 ns	256K-bit EEPROM with 64-Byte Page & Software Data Protection	Now
AT28C256E	32K x 8	150-250 ns	256K-bit EEPROM with Extended Endurance	Now
AT28C256F	32K x 8	150-250 ns	256K-bit EEPROM with Fast Write	Now
AT28C010	128K x 8	120-250 ns	1M-bit EEPROM with 128-Byte Page & Software Data Protection	Now
AT28C010E	128K x 8	120-250 ns	1M-bit EEPROM with 128-Byte Page & Extended Endurance & Software Data Protection	Now
AT28C040	512K x 8	200-250 ns	4M-bit EEPROM with 256-Byte Page & Software Data Protection	Now

Parallel EEPROM Die Product

Part Number	V_{CC}	Device T_{AA}	Package Configuration
AT28BV16-W	2.7 - 3.6V	250 ns	Die
AT28BV16-DWF	2.7 - 3.6V	250 ns	Wafer
AT28BV64-W	2.7 - 3.6V	250 ns	Die
AT28BV64-DWF	2.7 - 3.6V	250 ns	Wafer
AT28BV64B-W	2.7 - 3.6V	250 ns	Die
AT28BV64B-DWF	2.7 - 3.6V	250 ns	Wafer
AT28BV256-W	2.7 - 3.6V	250 ns	Die
AT28BV256-DWF	2.7 - 3.6V	250 ns	Wafer
AT28LV010-W	3.0 - 3.6V	250 ns	Die
AT28LV010-DWF	3.0 - 3.6V	250 ns	Wafer
AT28C16-W	4.5 - 5.5V	200 ns	Die
AT28C16-DWF	4.5 - 5.5V	200 ns	Wafer
AT28C64-W	4.5 - 5.5V	200 ns	Die
AT28C64-DWF	4.5 - 5.5V	200 ns	Wafer
AT28C64B-W	4.5 - 5.5V	200 ns	Die
AT28C64B-DWF	4.5 - 5.5V	200 ns	Wafer
AT28HC64B-W	4.5 - 5.5V	120 ns	Die
AT28HC64B-DWF	4.5 - 5.5V	120 ns	Wafer
AT28C256-W	4.5 - 5.5V	200 ns	Die
AT28C256-DWF	4.5 - 5.5V	200 ns	Wafer
AT28HC256-W	4.5 - 5.5V	120 ns	Die
AT28HC256-DWF	4.5 - 5.5V	120 ns	Wafer
AT28C010-W	4.5 - 5.5V	200 ns	Die
AT28C010-DWF	4.5 - 5.5V	200 ns	Wafer

Serial EEPROMs

Part Number	Organization	V_{CC}	Description	Availability
AT24C01	128 x 8	1.8, 2.5, 2.7, 5.0 V	1K-bit, 2-Wire Bus Serial EEPROM, Non-Cascadable	Now
AT24C21	128 x 8	2.5 V	1K-bit, 2-Wire Bus Serial EEPROM, Dual Mode, Plug & Play Operation	Now
AT24C01A	128 x 8	1.8, 2.5, 2.7, 5.0 V	1K-bit, 2-Wire Bus Serial EEPROM with Full Hardware Write Protection	Now
AT24C02	256 x 8	1.8, 2.5, 2.7, 5.0 V	2K-bit, 2-Wire Bus Serial EEPROM with Full Hardware Write Protection	Now
AT24C02A	256 x 8	1.8, 2.5, 2.7, 5.0 V	2K-bit, 2-Wire Bus Serial EEPROM with Full Hardware Write Protection	Now

Serial EEPROMs (Continued)

Part Number	Organization	V_{CC}	Description	Availability
AT34C02	256 x 8	1.8, 2.7, 5.0 V	2K-bit, 2-Wire Serial EEPROM with Software Write Protection	Now
AT24C04	512 x 8	1.8, 2.5, 2.7, 5.0 V	4K-bit, 2-Wire Bus Serial EEPROM with Full Hardware Write Protection	Now
AT24C04A	512 x 8	1.8, 2.5, 2.7, 5.0 V	4K-bit, 2-Wire Bus Serial EEPROM with Full Hardware Write Protection	Now
AT24C08	1K x 8	1.8, 2.5, 2.7, 5.0 V	8K-bit, 2-Wire Bus Serial EEPROM	Now
AT24C08A	1K x 8	1.8, 2.5, 2.7, 5.0 V	8K-bit, 2-Wire Bus Serial EEPROM with Full Hardware Write Protection	Now
AT24C16	2K x 8	1.8, 2.5, 2.7, 5.0 V	16K-bit, 2-Wire Bus Serial EEPROM with Half Hardware Write Protection	Now
AT24C164	2K x 8	1.8, 2.5, 2.7, 5.0 V	16K-bit, 2-Wire Bus Serial EEPROM with Cascadable Feature	Now
AT24C32	4K x 8	1.8, 2.5, 2.7, 5.0 V	32K-bit, 2-Wire Bus Serial EEPROM with Cascadable Feature	Now
AT24C64	8K x 8	1.8, 2.5, 2.7, 5.0 V	64K-bit, 2-Wire Bus Serial EEPROM with Cascadable Feature	Now
AT24C128	16K x 8	1.8, 2.7, 5.0 V	128K-bit, 2-Wire Bus Serial EEPROM with Cascadable Feature	Now
AT24C256	32K x 8	1.8, 2.7, 5.0 V	256K-bit, 2-Wire Bus Serial EEPROM with Cascadable Feature	Now
AT24C512	64K x 8	1.8, 2.7, 5.0 V	512K-bit, 2-Wire Bus Serial EEPROM with Cascadable Feature	Now
AT25010	128 x 8	1.8, 2.7, 5.0 V	1K-bit, SPI Bus Serial EEPROM, SPI Mode 0 and 3	Now
AT25020	256 x 8	1.8, 2.7, 5.0 V	2K-bit, SPI Bus Serial EEPROM, SPI Mode 0 and 3	Now
AT25040	512 x 8	1.8, 2.7, 5.0 V	4K-bit, SPI Bus Serial EEPROM, SPI Mode 0 and 3	Now
AT25080	1K x 8	1.8, 2.7, 5.0 V	8K-bit, SPI Bus Serial EEPROM, SPI Mode 0 and 3	Now
AT25160	2K x 8	1.8, 2.7, 5.0 V	16K-bit, SPI Bus Serial EEPROM, SPI Mode 0 and 3	Now
AT25320	4K x 8	1.8, 2.7, 5.0 V	32K-bit, SPI Bus Serial EEPROM, SPI Mode 0 and 3	Now
AT25640	8K x 8	1.8, 2.7, 5.0 V	64K-bit, SPI Bus Serial EEPROM, SPI Mode 0 and 3	Now
AT25128	16K x 8	1.8, 2.7, 5.0 V	128K-bit, SPI Bus Serial EEPROM, SPI Mode 0 and 3	Now
AT25256	32K x 8	1.8, 2.7, 5.0 V	256K-bit, SPI Bus Serial EEPROM, SPI Mode 0 and 3	Now
AT25HP256	32K x 8	1.8, 2.7, 5.0 V	256K-bit, SPI Bus Serial EEPROM, High-Speed, Page-Write Only, SPI Mode 0 and 3	4Q98
AT25HP512	64K x 8	1.8, 2.7, 5.0 V	512K-bit, SPI Bus Serial EEPROM, High-Speed, Page-Write Only, SPI Mode 0 and 3	4Q98
AT25P1024	1M x 8	1.8, 2.7, 5.0 V	1M-bit, SPI Bus Serial EEPROM, Page-Write Only, SPI Mode 0 and 3	Now
AT93C46	64 x 16 / 128 x 8	1.8, 2.5, 2.7, 5.0 V	1K-bit, 3-Wire Bus Serial EEPROM	Now
AT93C46A	64 x 16	2.5, 2.7, 5.0 V	1K-bit, 3-Wire Bus Serial EEPROM	Now

Serial EEPROMs (Continued)

Part Number	Organization	V_{CC}	Description	Availability
AT93C46C	64 x 16	2.5, 2.7, 5.0 V	1K-bit, 7-Wire Bus Serial EEPROM with Schmitt Trigger Inputs	Now
AT93C56	128 x 16 / 256 x 8	2.5, 2.7, 5.0 V	2K-bit, 3-Wire Bus Serial EEPROM	Now
AT93C57	128 x 16 / 256 x 8	2.5, 2.7, 5.0 V	2K-bit, 3-Wire Bus Serial EEPROM with Special Address	Now
AT93C66	256 x 16 / 512 x 8	2.5, 2.7, 5.0 V	4K-bit, 3-Wire Bus Serial EEPROM	Now
AT59C11	64 x 16 / 128 x 8	2.5, 2.7, 5.0 V	1K-bit, 4-Wire Bus Serial EEPROM	Now
AT59C22	128 x 16 / 256 x 8	2.5, 2.7, 5.0 V	2K-bit, 4-Wire Bus Serial EEPROM	Now
AT59C13	256 x 16 / 512 x 8	2.5, 2.7, 5.0 V	4K-bit, 4-Wire Bus Serial EEPROM	Now

EPROMs

Part Number	Organization	Speeds	Description	Availability
***Battery-Voltage*™ (2.7V to 3.6V)**				
AT27BV256	32K x 8	70-150 ns	256K-bit, 2.7-Volt to 3.6-Volt EPROM	Now
AT27BV512	64K x 8	70-150 ns	512K-bit, 2.7-Volt to 3.6-Volt EPROM	Now
AT27BV010	128K x 8	90-150 ns	1M-bit, 2.7-Volt to 3.6-Volt EPROM	Now
AT27BV1024	64K x 16	90-150 ns	1M-bit, 2.7-Volt to 3.6-Volt EPROM	Now
AT27BV020	256K x 8	90-150 ns	2M-bit, 2.7-Volt to 3.6-Volt EPROM	Now
AT27BV040	512K x 8	120-150 ns	4M-bit, 2.7-Volt to 3.6-Volt EPROM	Now
AT27BV4096	256K x 16	120-150 ns	4M-bit, 2.7-Volt to 3.6-Volt EPROM	Now
AT27BV400	512K x 8 / 256K x 16	150 ns	4M-bit, Byte-Selectable 2.7-Volt to 3.6-Volt EPROM	Nov 98
AT27BV800	1M x 8 / 512K x 16	150 ns	8M-bit, Byte-Selectable 2.7-Volt to 3.6-Volt EPROM	Nov 98
Low-Voltage (3.0 to 3.6V)				
AT27LV256A	32K x 8	55-150 ns	256K-bit, 3-Volt EPROM	Now
AT27LV512A	64K x 8	70-150 ns	512K-bit, 3-Volt EPROM	Now
AT27LV520	64K x 8	90 ns	512K-bit, Latched 3-Volt EPROM	Now
AT27LV010A	128K x 8	70-150 ns	1M-bit, 3-Volt EPROM	Now
AT27LV1026	2 x 32K x 16	35-55 ns	1M-bit, Interleaved 3-Volt EPROM	Now
AT27LV020A	256K x 8	90-150 ns	2M-bit, 3-Volt EPROM	Now
AT27LV040A	512K x 8	90-150 ns	4M-bit, 3-Volt EPROM	Now
Standard Voltage (5.0V)				
AT27C256R	32K x 8	45-150 ns	256K-bit, 5-Volt EPROM	Now
AT27C512R	64K x 8	45-150 ns	512K-bit, 5-Volt EPROM	Now
AT27C516	32K x 16	45-100 ns	512K-bit, 5-Volt EPROM	Now
AT27C520	64K x 8	70, 90 ns	512K-bit, Latched 5-Volt EPROM	Now
AT27C010,L	128K x 8	45-150 ns	1M-bit, 5-Volt EPROM Standard & Low-Power	Now
AT27C1024	64K x 16	45-150 ns	1M-bit, 5-Volt EPROM	Now
AT27C020	256K x 8	55-150 ns	2M-bit, 5-Volt EPROM	Now
AT27C2048	128K x 16	55-150 ns	2M-bit, 5-Volt EPROM	Now
AT27C040	512K x 8	70-150 ns	4M-bit, 5-Volt EPROM	Now
AT27C4096	256K x 16	55-150 ns	4M-bit, 5-Volt EPROM	Now
AT27C400	512K x 8 / 256K x 16	70-150 ns	4M-bit, Byte-Selectable 5-Volt EPROM	Nov 98
AT27C080	1M x 8	90-150 ns	8M-bit, 5-Volt EPROM	Now
AT27C800	1M x 8 / 512K x 16	100-150 ns	8M-bit, Byte-Selectable 5-Volt EPROM	Now

Flash

Part Number	Organization	Speeds	Description	Availability
Lithium *Battery-Voltage* (2.5V to 3.0V)				
AT49LBV010	128K x 8	120-200 ns	1M-bit, 2.5-Volt Read and 2.5-Volt Byte-Write Flash	Now
AT49LBV020	256K x 8	120-200 ns	2M-bit, 2.5-Volt Read and 2.5-Volt Byte-Write Flash	Now
AT49LBV040	512K x 8	120-200 ns	4M-bit, 2.5-Volt Read and 2.5-Volt Byte-Write Flash	Now
AT49LBV080	1M x 8	120-200 ns	8M-bit, 2.5-Volt Read and 2.5-Volt Byte-Write Flash	Now
AT49LBV080T	1M x 8	120-200 ns	8M-bit, 2.5-Volt Read and 2.5-Volt Byte-Write Flash (Top Boot)	Now
AT49LBV008	1M x 8	120-200 ns	8M-bit, 2.5-Volt Read and 2.5-Volt Byte-Write Flash	Now
AT49LBV008T	1M x 8	120-200 ns	8M-bit, 2.5-Volt Read and 2.5-Volt Byte-Write Flash (Top Boot)	Now

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Flash (Continued)

Part Number	Organization	Speeds	Description	Availability
Battery-Voltage **(2.7V to 3.6V)**				
AT29BV010A	128K x 8	200-250 ns	1M-bit, 2.7-Volt Read and 2.7-Volt Write Sectored Flash	Now
AT29BV020	256K x 8	250 ns	2M-bit, 2.7-Volt Read and 2.7-Volt Write Sectored Flash	Now
AT29BV040A	512K x 8	250 ns	4M-bit, 2.7-Volt Read and 2.7-Volt Write Sectored Flash	Now
AT49BV512	64K x 8	120-150 ns	512K-bit, 2.7-Volt Read and 2.7-Volt Byte-Write Flash	Now
AT49BV010	128K x 8	120-150 ns	1M-bit, 2.7-Volt Read and 2.7-Volt Byte-Write Flash	Now
AT49HBV010	128K x 8	90-150 ns	1M-bit, 2.7-Volt Read and 2.7-Volt Byte-Write Flash (High-Speed)	Now
AT49BV001	128K x 8	70-120 ns	1M-bit, 2.7-Volt Read and 2.7-Volt Byte-Write Sectored Flash	4Q98
AT49BV001N	128K x 8	70-120 ns	1M-bit, 2.7-Volt Read and 2.7-Volt Byte-Write Sectored Flash	4Q98
AT49BV001T	128K x 8	70-120 ns	1M-bit, 2.7-Volt Read and 2.7-Volt Byte-Write Sectored Flash (Top Boot)	Now
AT49BV020	256K x 8	90-150 ns	2M-bit, 2.7-Volt Read and 2.7-Volt Byte-Write Flash	Now
AT49BV002	256K x 8	70-120 ns	2M-bit, 2.7-Volt Read and 2.7-Volt Byte-Write Sectored Flash	Now
AT49BV002N	256K x 8	70-120 ns	2M-bit, 2.7-Volt Read and 2.7-Volt Byte-Write Sectored Flash	Now
AT49BV002T	256K x 8	70-120 ns	2M-bit, 2.7-Volt Read and 2.7-Volt Byte-Write Sectored Flash (Top Boot)	Now
AT49BV2048	128K x 16	120-150 ns	2M-bit, 2.7-Volt Read and 2.7-Volt Byte-Write Flash	Now
AT49BV2048A	128K x 16	150-200 ns	2M-bit, 2.7-Volt Read and 2.7-Volt Byte-Write Sectored Flash	Now
AT49BV040	512K x 8	120-150 ns	4M-bit, 2.7-Volt Read and 2.7-Volt Byte-Write Flash	Now
AT49BV040T	512K x 8	150-200 ns	4M-bit, 2.7-Volt Read and 2.7-Volt Byte-Write Sectored Flash (Top Boot)	Now
AT49BV004	512K x 8	120-200 ns	4M-bit, 2.7-Volt Read and 2.7-Volt Byte-Write Sectored Flash	4Q98
AT49BV004T	512K x 8	120-200 ns	4M-bit, 2.7-Volt Read and 2.7-Volt Byte-Write Sectored Flash (Top Boot)	4Q98
AT49BV4096	256K x 16	120-150 ns	4M-bit, 2.7-Volt Read and 2.7-Volt Byte-Write Flash	Now
AT49BV4096A	256K x 16	120-200 ns	4M-bit, 2.7-Volt Read and 2.7-Volt Byte-Write Sectored Flash	Now
AT49BV4096AT	256K x 16	120-200 ns	4M-bit, 2.7-Volt Read and 2.7-Volt Byte-Write Sectored Flash (Top Boot)	Now
AT49BV080	1M x 8	120-150 ns	8M-bit, 2.7-Volt Read and 2.7-Volt Byte-Write Flash	Now
AT49BV080T	1M x 8	120-150 ns	8M-bit, 2.7-Volt Read and 2.7-Volt Byte-Write Flash (Top Boot)	Now
AT49BV008	1M x 8	120-150 ns	8M-bit, 2.7-Volt Read and 2.7-Volt Byte-Write Flash	Now
AT49BV8192	512K x 16	120-150 ns	8M-bit, 2.7-Volt Read and 2.7-Volt Byte-Write Flash	Now
AT49BV8192A	512K x 16	120-200 ns	8M-bit, 2.7-Volt Read and 2.7-Volt Byte-Write Sectored Flash	Now
AT49BV8192AT	512K x 16	120-200 ns	8M-bit, 2.7-Volt Read and 2.7-Volt Byte-Write Sectored Flash (Top Boot)	Now
AT49BV8192T	512K x 16	120-150 ns	8M-bit, 2.7-Volt Read and 2.7-Volt Byte-Write Flash (Top Boot)	Now
AT49BV1604	1M x 16	120-150 ns	16M-bit, 2.7-Volt Read and 2.7-Volt Byte-Write Sectored Flash	Now
AT49BV1604T	1M x 16	90,120 ns	16M-bit, 2.7-Volt Read and 2.7-Volt Byte-Write Sectored Flash (Top Boot)	Now
AT49BV1614	2M x 8	90,120 ns	16M-bit, 2.7-Volt Read and 2.7-Volt Byte-Write Sectored Flash	Now
AT49BV1614T	2M x 8	90,120 ns	16M-bit, 2.7-Volt Read and 2.7-Volt Byte-Write Sectored Flash (Top Boot)	Now

Flash (Continued)

Part Number	Organization	Speeds	Description	Availability
Low-Voltage (3.0V to 3.6V)				
AT29LV256	32K x 8	150-250 ns	256K-bit, 3-Volt Read and 3-Volt Write Sectored Flash	Now
AT29LV512	64K x 8	150-250 ns	512K-bit, 3-Volt Read and 3-Volt Write Sectored Flash	Now
AT29LV010A	128K x 8	150-250 ns	1M-bit, 3-Volt Read and 3-Volt Write Sectored Flash	Now
AT29LV1024	64K x 16	150-250 ns	1M-bit, 3-Volt Read and 3-Volt Write Sectored Flash	Now
AT29LV020	256K x 8	200-250 ns	2M-bit, 3-Volt Read and 3-Volt Write Sectored Flash	Now
AT29LV040A	512K x 8	200-250 ns	4M-bit, 3-Volt Read and 3-Volt Write Sectored Flash	Now
AT49LV512	64K x 8	90-120 ns	512K-bit, 3-Volt Read and 2.7-Volt Byte-Write Flash	Now
AT49LV010	128K x 8	120-150 ns	1M-bit, 3-Volt Read and 3-Volt Byte-Write Flash	Now
AT49HLV010	128K x 8	90 ns	1M-bit, 3-Volt Read and 3-Volt Byte-Write Flash (High-Speed)	Now
AT49LV001	128K x 8	55-120 ns	1M-bit, 3-Volt Read and 3-Volt Byte-Write Sectored Flash	4Q98
AT49LV001N	128K x 8	55-120 ns	1M-bit, 3-Volt Read and 3-Volt Byte-Write Sectored Flash	4Q98
AT49LV001T	128K x 8	55-90 ns	1M-bit, 3-Volt Read and 2.7-Volt Byte-Write Sectored Flash (Top Boot)	Now
AT49LV020	256K x 8	90-150 ns	2M-bit, 3-Volt Read and 3-Volt Byte-Write Flash	Now
AT49LV002	256K x 8	55-120 ns	2M-bit, 3-Volt Read and 3-Volt Byte-Write Sectored Flash	Now
AT49LV002N	256K x 8	55-120 ns	2M-bit, 3-Volt Read and 3-Volt Byte-Write Sectored Flash	Now
AT49LV002T	256K x 8	55-90 ns	2M-bit, 3-Volt Read and 2.7-Volt Byte-Write Sectored Flash (Top Boot)	Now
AT49LV2048	128K x 16	120-150 ns	2M-bit, 3-Volt Read and 3-Volt Byte-Write Flash	Now
AT49LV040	512K x 8	90-150 ns	4M-bit, 3-Volt Read and 3-Volt Byte-Write Flash	Now
AT49LV040T	512K x 8	120-200 ns	4M-bit, 3-Volt Read and 3-Volt Byte-Write Sectored Flash (Top Boot)	Now
AT49LV4096	256K x 16	120-150 ns	4M-bit, 3-Volt Read and 3-Volt Byte-Write Flash	Now
AT49LV080	1M x 8	120-150 ns	8M-bit, 3-Volt Read and 3-Volt Byte-Write Flash	Now
AT49LV080T	1M x 8	120-150 ns	8M-bit, 3-Volt Read and 3-Volt Byte-Write Flash (Top Boot)	Now
AT49LV008	1M x 8	120-150 ns	8M-bit, 3-Volt Read and 3-Volt Byte-Write Flash	Now
AT49LV008T	1M x 8	110,120ns	8M-bit, 3-volt Read and 3-Volt Byte-Write Sectored Flash (Top Boot)	Now
AT49LV8192	512K x 16	120-150 ns	8M-bit, 3-Volt Read and 3-Volt Byte-Write Flash	Now
AT49LV8192T	512K x 16	120-150 ns	8M-bit, 3-Volt Read and 3-Volt Byte-Write Flash (Top Boot)	Now
Standard Voltage (5.0V)				
AT29C256	32K x 8	70-150 ns	256K-bit, 5-Volt Read and 5-Volt Write Sectored Flash	Now
AT29C257	32K x 8	70-150 ns	256K-bit, 5-Volt Read and 5-Volt Write Sectored Flash	Now
AT29C512	64K x 8	70-150 ns	512K-bit, 5-Volt Read and 5-Volt Write Sectored Flash	Now
AT29C010A	128K x 8	70-150 ns	1M-bit, 5-Volt Read and 5-Volt Write Sectored Flash	Now
AT29C1024	64K x 16	70-150 ns	1M-bit, 5-Volt Read and 5-Volt Write Sectored Flash	Now
AT29C020	256K x 8	90-150 ns	2M-bit, 5-Volt Read and 5-Volt Write Sectored Flash	Now
AT29C040A	512K x 8	100-200 ns	4M-bit, 5-Volt Read and 5-Volt Write Sectored Flash	Now
AT49F512	64K x 8	55-90 ns	512K-bit, 5-Volt Read and 5-Volt Byte-Write Flash	Now
AT49F010	128K x 8	70-120 ns	1M-bit, 5-Volt Read and 5-Volt Byte-Write Flash	Now
AT49HF010	128K x 8	45-55 ns	1M-bit, 5-Volt Read and 5-Volt Byte-Write Flash (High-Speed)	Now
AT49F001	128K x 8	55-120 ns	1M-bit, 5-volt Read and 5-Volt Byte-Write Sectored Flash	4Q98
AT49F001N	128K x 8	55-120 ns	1M-bit, 5-volt Read and 5-Volt Byte-Write Sectored Flash	4Q98
AT49F001T	128K x 8	55-90 ns	1M-bit, 5-Volt Read and 5-Volt Byte-Write Sectored Flash (Top Boot)	Now
AT49F1024	64K x 16	55-90 ns	1M-bit, 5-Volt Read and 5-Volt Byte-Write Flash	Now
AT49F1025	64K x 16	55-90 ns	1M-bit, 5-Volt Read and 5-Volt Byte-Write Flash	Now

Flash (Continued)

Part Number	Organization	Speeds	Description	Availability
AT49F020	256K x 8	55-120 ns	2M-bit, 5-Volt Read and 5-Volt Byte-Write Flash	Now
AT49F002	256K x 8	50-120 ns	2M-bit, 5-Volt Read and 5-Volt Byte-Write Sectored Flash	Now
AT49F002N	256K x 8	50-120 ns	2M-bit, 5-Volt Read and 5-Volt Byte-Write Sectored Flash	Now
AT49F002T	256K x 8	50-70 ns	2M-bit, 5-Volt Read and 5-Volt Byte-Write Sectored Flash	Now
AT49F2048	128K x 16	70-120 ns	2M-bit, 5-Volt Read and 5-Volt Byte-Write Flash	Now
AT49F2048A	128K x 16	70-120 ns	2M-bit, 5-Volt Read and 5-Volt Byte-Write Sectored Flash	Now
AT49F040	512K x 8	70-150 ns	4M-bit, 5-Volt Read and 5-Volt Byte-Write Flash	Now
AT49F040T	512K x 8	90-150 ns	4M-bit, 5-Volt Read and 5-Volt Byte-Write Sectored Flash (Top Boot)	Now
AT49F004	512K x 8	70-120 ns	4M-bit, 5-Volt Read and 5-Volt Byte-Write Sectored Flash	4Q98
AT49F004T	512K x 8	70-120 ns	4M-bit, 5-volt Read and 5-Volt Byte-Write Sectored Flash (Top Boot)	4Q98
AT49F4096	256K x 16	90-120 ns	4M-bit, 5-Volt Read and 5-Volt Byte-Write Flash	Now
AT49F4096A	256K x 16	70-120 ns	4M-bit, 5-Volt Read and 5-Volt Byte-Write Sectored Flash	Now
AT49F4096AT	256K x 16	70-120 ns	4M-bit, 5-Volt Read and 5-Volt Byte-Write Sectored Flash (Top Boot)	Now
AT49F080	1M x 8	90-150 ns	8M-bit, 5-Volt Read and 5-Volt Byte-Write Flash	Now
AT49F080T	1M x 8	90-150 ns	8M-bit, 5-Volt Read and 5-Volt Byte-Write Flash (Top Boot)	Now
AT49F008	1M x 8	90,120,150 ns	8M-bit, 5-Volt Read and 5-Volt Byte-Write Sectored Flash	Now
AT49F008T	1M x 8	90,120,150 ns	8M-bit, 5-Volt Read and 5-Volt Byte-Write Sectored Flash (Top Boot)	Now
AT49F8192	512K x 16	90,120 ns	8M-bit, 5-Volt Read and 5-Volt Byte-Write Sectored Flash	Now
AT49F8192A	512K x 16	70-120 ns	8M-bit, 5-Volt Read and 5-Volt Byte-Write Sectored Flash	Now
AT49F8192AT	512K x 16	70-120 ns	8M-bit, 5-Volt Read and 5-Volt Byte-Write Sectored Flash (Top Boot)	Now
AT49F8192T	512K x 16	90, 120 ns	8M-bit, 5-Volt Read and 5-Volt Byte-Write Sectored Flash (Top Boot)	Now
AT49F1604	1M x 16	70, 90 ns	16M-bit, 5-Volt Read and 5-Volt Byte-Write Sectored Flash	Now
AT49F1604T	1M x 16	70, 90 ns	16M-bit, 5-Volt Read and 5-Volt Byte-Write Sectored Flash (Top Boot)	Now
AT49F1614	2M x 8	70, 90 ns	16M-bit, 5-Volt Read and 5-Volt Byte-Write Sectored Flash	Now
AT49F1614T	2M x 8	70, 90 ns	16M-bit, 5-Volt Read and 5-Volt Byte-Write Sectored Flash (Top Boot)	Now

Flash Memory Cards

Part Number	Organization	V_{CC}	Description	Availability
AT5FC001	1M byte	5-Volt	PCMCIA Compatible Flash Memory Card	Now
AT5FC002	2M byte	5-Volt	PCMCIA Compatible Flash Memory Card	Now
AT5FC004	4M byte	5-Volt	PCMCIA Compatible Flash Memory Card	Now
AT5FC008	8M byte	5-Volt	PCMCIA Compatible Flash Memory Card	Now

Gate Arrays/Embedded Arrays

Device Name	Gates	Pins	Description	Availability
ATL18 Series	4.8M	Up to 1200	0.18-Micron CMOS Gate Array/Embedded Array, 1.8-Volt Operation, 30 Versions with Various Pin & Gate Counts, Memory, Megacells	1H2000
ATL25 Series	Up to 7.3M	Up to 1038	0.25-Micron CMOS Gate Array/Embedded Array, 1.0 to 2.5-Volt Operation, 23 Versions with Various Pin & Gate Counts, Memory, Megacells	1Q99
ATL25/EE Series	Up to 7.3M	Up to 1038	0.25-Micron CMOS Embedded Array Combining Logic and EE Memory, 2.5-Volt Operation, Various Gate Counts, Megacells and Memory Configuration. Up to 4M-bit EE Memory	1H2000
ATL25/Flash Series	Up to 7.3M	Up to 1038	0.25-Micron CMOS Embedded Array Combining CMOS Logic and Flash Memory, 2.5-Volt Operation. Various Gate Counts, Megacells and Memory Configuration. Up to 64M-bit Flash Memory	2H99

Gate Arrays/Embedded Arrays (Continued)

Device Name	Gates	Pins	Description	Availability
ATL35 Series	Up to 3.7M	Up to 976	0.35-Micron CMOS Gate Array/Embedded Array, 1.0-Volt to 3.3-Volt Operation, 23 Versions with Various Pin & Gate Counts, Memory, Megacells	Now
ATL35/EE Series	Up to 3.7M	Up to 976	0.35-Micron Embedded Array combining CMOS Logic and EE Memory, 2.5-Volt Operation, Various Gate Counts, Megacells, and Memory Configurations. Up to 1M-bit EE Memory	1H99
ATL35/Flash Series	Up to 3.7M	Up to 976	0.35-Micron Embedded Array Combining CMOS Logic and Flash Memory, 2.0 and 3.3-Volt Operation, Various Gate Counts, Megacells and Memory Configurations. Up to 32M-bit Flash Memory	1Q99
ATL50 Series	Up to 590K	Up to 480	0.5-Micron CMOS Gate Array/Embedded Array, 2.0-Volt & 3.3-Volt Voltage Operation, 16 Versions with Various Pin & Gate Counts, Memory, Megacells	Now
ATL50/EE Series	Up to 1.9M	Up to 684	0.5-Micron Embedded Array Combining CMOS Logic with EE and Flash Memory, 2.0 and 3.3-Volt Operation, Various Gate Counts, Megacells and Memory Configurations. Up to 1M-bit Flash Memory and 64K-bit EE Memory	Now
ATLS60 Series	Up to 88K	Up to 256	0.6-Micron CMOS Gate Array/Embedded Array, 3.3-Volt & 5.0-Volt Operation, Staggered Row Bond Pads, 8 Versions with Various Pin & Gate Counts, Memory, Megacells	Now
ATL60 Series	Up to 590K	Up to 480	0.6-Micron CMOS Gate Array/Embedded Array, 3.3-Volt & 5.0-Volt Operation, 16 Versions with Various Pin & Gate Counts, Memory, Megacells	Now
Megacells			ARM7TDMI™, AVR® (8-bit RISC), OakDSPCore™, LodeDSPCore™ Ethernet MAC, USB Cores, PCI Cores, plus others	Now
Memory			Flash, EEPROM, SRAM, ROM, Dual Port SRAM, FIFO and CAM	Now
I/O Interfaces			CMOS, TTL, LVDS, PCI, USB, SCSI, LVD SCSI, PLL	Now

Cell-Based ICs

Part Number	Description	Availability
ATC50	0.5-Micron 3-Layer Metal CMOS, 3.3V Operation, Digital, Analog, Memory, Macrocells	Now
ATC50/EE	0.5-Micron 3-Layer Metal CMOS with Embedded EEPROM, 3.3-Volt Operation	Now
ATC35	0.35-Micron 3/5-Layer Metal CMOS 3.3-Volt Operation, Digital, Analog, Memory, Megacells	Now
ATC35/EE	0.35-Micron 3/5-Layer Metal CMOS with Embedded EEPROM, 3.3-Volt Operation	1H99
ATC35/Flash	0.35-Micron 3/5-Layer Metal CMOS with embedded Flash, 3.3-Volt Operation	1H99
ATC25	0.25-Micron 3/5-Layer Metal CMOS, 2.5-Volt Operation, Digital, Analog, Memory, Macrocells	1H99
ATC25/EE	0.25-Micron 3/5-Layer Metal CMOS with Embedded EEPROM, 2.5-Volt Operation	1H2000
ATC25/Flash	0.25-Micron 3/5-Layer Metal CMOS with Embedded Flash, 2.5-Volt Operation	1H2000
ATC18	0.18-Micron 3/5-Layer Metal CMOS, 1.8-Volt Operation, Digital, Analog, Memory, Macrocells	2H99
Macrocells	ARM/Thumb™, AVR®, OakDSPCore™, Ethernet MAC, AT8051, AT8237, AT8251, AT8254, AT8255, AT8259, AT82530, AT14818,AT16450, RAM, Dual-port RAM, ROM, Flash, EEPROM, PCI, SPI, USB, Codec, A/D, D/A, OpAmp, Comp., Osc., etc.	Now

PLDs

Part Number	Packages	Speeds	Description	Availability
5-Volt Electrically Erasable				
ATF16V8B	20-pin	10-25 ns	8 FFs, 8 I/O Pins, Standard-Power	Now
ATF16V8BQ/BQL	20-pin	10-25 ns	8 FFs, 8 I/O Pins, Quarter-Power, Low-Power	Now
ATF16V8C	20-pin	5-7.5 ns	8 FFs, 8 I/O Pins, Standard-Power	Now
ATF16V8CZ	20-pin	12-15 ns	8 FFs, 8 I/O Pins, Zero-Power	Now
ATF20V8B	24, 28-pin	7.5-25 ns	8 FFs, 8 I/O Pins, Standard-Power	Now
ATF20V8BQ/BQL	24, 28-pin	10-25 ns	8 FFs, 8 I/O Pins, Quarter-Power, Low-Power	Now
ATF20V8C	24, 28-pin	5-7 ns	8 FFs, 8 I/O Pins, Standard-Power	1H99
ATF20V8CZ	24, 28-pin	12-15 ns	8 FFs, 8 I/O Pins, Zero-Power	1H99
ATF22V10B	24, 28-pin	15-25 ns	10 FFs, 10 I/O Pins, Standard-Power	Now
ATF22V10BQ/BQL	24, 28-pin	15-25 ns	10 FFs, 10 I/O Pins, Quarter-Power, Low-Power	Now
ATF22V10C	24, 28-pin	5-10 ns	10 FFs, 10 I/O Pins, Standard-Power	Now
ATF22V10CZ	24, 28-pin	12-15 ns	10 FFs, 10 I/O Pins, Zero-Power	Now
ATF750C/CL	24, 28-pin	7.5-25 ns	20 FFs, 10 I/O Pins, Standard & Low-Power	4Q98
ATF2500C/CL	40, 44-pin	20-25 ns	48 FFs, 24 I/O Pins, Standard & Low-Power	3Q99
ATFV2500CQ/CQL	40, 44-pin	20-25 ns	48 FFs, 24 I/O Pins, Quarter-Power, Low-Power	3Q99
ATF1500/L	44-pin	7.5-25 ns	32 Macrocell, Standard & Low-Power	Now
ATF1500A/AL	44-pin	7.5-25 ns	32 Macrocell, Standard & Low-Power	Now
ATF1502AS/L	44-pin	7.5-25 ns	32 Macrocell w/ISP, Standard & Low-Power	1Q99
ATF1504AS/L	44, 68, 84, 100-pin	7.5-25 ns	64 Macrocell w/ISP, Standard & Low-Power	Now
ATF1508AS/L	68, 84, 100, 160-pin	7.5-25 ns	128 Macrocell w/ISP, Standard & Low-Power	Now
ATF1516AS/L	160, 192, 208-pin	10-25 ns	256 Macrocell w/ISP, Standard & Low-Power	2Q99
Low-Voltage (3.0V) Electrically Erasable				
ATF16LV8C	20-pin	10-15 ns	8 FFs, 8 I/O Pins, Low-Voltage	Now
ATF16LV8CZ	20-pin	15-25 ns	8 FFs, 8 I/O Pins, Low-Voltage, Zero-Power	TBA
AT22LV10/L	24, 28-pin	20-30 ns	10 FFs, 10 I/O Pins, Low-Voltage & Low-Power (EPROM-based)	Now
ATF750LVC/LVCL	24, 28-pin	10-25 ns	20 FFs, 10 I/O Pins, Low-Voltage & Low-Power	4Q98
ATF1500ABV	44-pin	12-15 ns	32 FFs, 32 I/O Pins, Low-Voltage	Now
ATF1500ABVL	44-pin	25 ns	32 FFs, 32 I/O Pins, Low-Voltage & Low-Power	TBA
ATF22LV10C	24, 28-pin	10-15 ns	10 FFs, 10 I/O Pins, Low-Voltage	Now
ATF22LV10CZ	24, 28-pin	15-25 ns	10 FFs, 10 I/O Pins, Low-Voltage, Zero-Power	Now
5-Volt EPROM-Based				
ATV750/L	24, 28-pin	20-25 ns	20 FFs, 10 I/O Pins, Standard & Low-Power	Now
ATV750B/BL	24, 28-pin	7.5-25 ns	20 FFs, 10 I/O Pins, Standard & Low-Power	Now
ATV2500H/L	40, 44-pin	25-35 ns	48 FFs, 24 I/O Pins, Standard & Low-Power	Now
ATV2500B/BL	44-pin	12-20 ns	48 FFs, 24 I/O Pins, Standard & Low-Power	Now
ATV2500BQ/BQL	40, 44-pin	20-25 ns	48 FFs, 24 I/O Pins, Quarter-Power, Low-Power	Now

PLD Tools - Software and Hardware

Part Number	Description	Availability
ATDS1100PC	Atmel – Synario Entry (Includes ABEL, Schematic Entry, Simulation)	Now
ATDS1120PC	Atmel – Synario Verilog Simulation	Now
ATDS1130PC	Atmel – Synario VHDL Synthesis	Now
ATDS1150PC	Atmel – ISP Kit	Now
ATDS1160PC	Atmel – ISP Programming Board	Now
ATDS1161PC	Atmel – 44-pin PLCC Adaptor Board	Now
ATDS1162PC	Atmel – 44-pin TQFP Adaptor Board	Now
ATDS1163PC	Atmel – 68-pin PLCC Adaptor Board	Now
ATDS1164PC	Atmel – 100-pin PQFP Adaptor Board	Now
ATDS1165PC	Atmel – 100-pin TQFP Adaptor Board	Now
ATDS1166PC	Atmel – 160-pin PQFP Adaptor Board	Now

FPGAs - AT6000

Part Number	Registers	Usable Gates	Frequency	Description	Availability
Standard Voltage (5.0V)					
AT6002	1,024	6K	350 MHz	96 I/O Pins, 5-Volt, Very Low Power	Now
AT6003	1,600	9K	350 MHz	120 I/O Pins, 5-Volt, Very Low Power	Now
AT6005	3,136	15K	350 MHz	140 I/O Pins, 5-Volt, Very Low Power	Now
AT6010	6,400	30K	350 MHz	204 I/O Pins, 5-Volt, Very Low Power	Now
Low-Voltage (3.3V)					
AT6002LV	1,024	6K	250 MHz	96 I/O Pins, 3.3-Volt, Very Low Power	Now
AT6003LV	1,600	9K	250 MHz	120 I/O Pins, 3.3-Volt, Very Low Power	Now
AT6005LV	3,136	15K	250 MHz	140 I/O Pins, 3.3-Volt, Very Low Power	Now
AT6010LV	6,400	30K	250 MHz	204 I/O Pins, 3.3-Volt, Very Low Power	Now

FPGAs - AT40K

Part Number	Registers	Usable Gates	Frequency	RAM	Description	Availability
Standard Voltage (5.0V)						
AT40K05	256	5K-10K	250 MHz	2,048	128 I/O Pins, 5-Volt, Very Low Power	Now
AT40K10	576	10K-20K	250 MHz	4,096	192 I/O Pins, 5-Volt, Very Low Power	Now
AT40K20	1,024	20K-30K	250 MHz	8,192	256 I/O Pins, 5-Volt, Very Low Power	Now
AT40K30	1,600	30K-40K	250 MHz	12,800	320 I/O Pins, 5-Volt, Very Low Power	4Q98
AT40K40	2,304	40K-50K	250 MHz	18,432	384 I/O Pins, 5-Volt, Very Low Power	Now
Low-Voltage (3.3V)						
AT40K05LV	256	5K-10K	250 MHz	2,048	128 I/O Pins, 3.3-Volt, Very Low Power	Now
AT40K10LV	576	10K-20K	250 MHz	4,096	192 I/O Pins, 3.3-Volt, Very Low Power	Now
AT40K20LV	1,024	20K-30K	250 MHz	8,192	256 I/O Pins, 3.3-Volt, Very Low Power	Now
AT40K30LV	1,600	30K-40K	250 MHz	12,800	320 I/O Pins, 3.3-Volt, Very Low Power	4Q98
AT40K40LV	2,304	40K-50K	250 MHz	18,432	384 I/O Pins, 3.3-Volt, Very Low Power	Now

FPGA Design Development Software

FPGA design tools are available across a broad range of CAE tool vendors and PC and workstation platforms. Design methods supported include: schematic capture, logic synthesis (VHDL and Verilog), PLD entry, (ABEL and CUPL), and automatic component generation of hard macros for user-parametrized structured logic (arithmetic elements, counters, registers, encoders, decoders, and other common functions). Refer to current Configurable Logic Data Book.

CAE Tool Support:

Cadence, Everest, Exemplar, Mentor, OrCAD, Synopsys, Synario, Veribest, Verilog, ViewLogic.

Platform Support:

PC (Windows 3.1, 95, NT), SUN Workstations, HP Workstations.

AT89 Series (8-bit Microcontrollers)

Part Number	Memory Size	Description	Availability
AT80F51	4K x 8	80C31 Microcontroller with 4K ROM replacement	Now
AT80F52	8K x 8	80C32 Microcontroller with 8K ROM replacement	Now
AT87F51	4K x 8	80C31 Microcontroller with 4K OTP QuickFlash	Now
AT87F52	8K x 8	80C32 Microcontroller with 8K OTP QuickFlash	Now
AT89C51	4K x 8	80C31 Microcontroller with 4K bytes Flash	Now
AT89LV51	4K x 8	2.7-Volt, 80C31 Microcontroller with 4K bytes Flash	Now
AT89C52	8K x 8	80C32 Microcontroller with 8K bytes Flash	Now
AT89LV52	8K x 8	2.7-Volt, 80C32 Microcontroller with 8K bytes Flash	Now
AT89C1051U	1K x 8	80C31 Microcontroller with 1K bytes Flash, 20-Pin Package	Now
AT89C2051	2K x 8	80C31 Microcontroller with 2K bytes Flash, 20-Pin Package	Now
AT89C4051	4K x 8	80C31 Microcontroller with 4K bytes Flash, 20-Pin Package	Now
AT89S8252	8K x 8	In-System Programmable Microcontroller with 8K bytes Flash and 2K bytes EEPROM	Now
AT89LS8252	8K x 8	Low-Voltage, In-System Programmable Microcontroller with 8K bytes Flash and 2K bytes EEPROM	Now
AT89S53	12K x 8	In-System Programmable Microcontroller with 12K bytes Flash	Now
AT89LS53	12K x 8	Low-Voltage, In-System Programmable Microcontroller with 12K bytes Flash	Now
AT89C55	20K x 8	80C32 Microcontroller with 20K bytes Flash	Now
AT89LV55	20K x 8	2.7-Volt, 80C32 Microcontroller with 20K bytes Flash	Now

AT91 Series (16/32-bit Microcontrollers)

Part Number	Processor	Description	Availability
AT91M40100	ARM7TDMI®	General Purpose, 16/32-bit RISC Microcontroller with 1K bytes RAM, 100-lead TQFP package	4Q98
AT91M40400	ARM7TDMI	General Purpose, 16/32-bit RISC Microcontroller with 4K bytes RAM, 100-lead TQFP package	Now
AT91M4040x	ARM7TDMI	General Purpose, 16/32-bit RISC Microcontroller with 4K bytes RAM and up to 2M-bit ROM, 100-lead TQFP package	Now

AT91 Series Development Tools

Part Number	Description	Availability
AT91SDT	ARM Software Development ToolKit	Now
AT91DB01	AT91 Development Board	Now
AT91EICE	ARM Embedded ICE Box	Now
AT91EB01	AT91 Evaluation Board	4Q98

AT90 Series AVR® (8-bit Microcontrollers)

Part Number	Processor	Description	Availability
AT90S1200	AVR	AVR RISC, In-System Programmable Microcontroller with 1K byte FLASH and 64 bytes EEPROM; 20-pin PDIP, 20-pin SOIC and 20-pin SSOP packages	Now
AT90S2313	AVR	AVR RISC, In-System Programmable Microcontroller with 2K bytes FLASH,128 bytes SRAM, 128 bytes EEPROM and UART; 20-pin PDIP and 20-pin SOIC packages	Now
AT90S2323	AVR	AVR RISC, In-System Programmable Microcontroller with 2K bytes FLASH,128 bytes SRAM and 128 bytes EEPROM; 8-pin PDIP and 8-pin SOIC packages	Now
AT90LS2323	AVR	Low-Voltage, AVR RISC, In-System Programmable Microcontroller with 2K bytes FLASH, 128 bytes SRAM and 128 bytes EEPROM; 8-pin PDIP and 8-pin SOIC packages	Now
AT90S2343	AVR	AVR RISC, In-System Programmable Microcontroller with 2K bytes FLASH, 128 bytes SRAM and 128 bytes EEPROM; 8-pin PDIP and 8-pin SOIC packages	Now
AT90LS2343	AVR	Low-Voltage, AVR RISC, In-System Programmable Microcontroller with 2K bytes FLASH, 128 bytes SRAM and 128 bytes EEPROM; 8-pin PDIP and 8-pin SOIC packages	Now
AT90S2333	AVR	AVR RISC, In-System Programmable Microcontroller with 2K bytes FLASH, 128 bytes SRAM, 128 bytes EEPROM, UART, 6 Channel 10-Bit ADC; 28-pin PDIP, 28-pin SOIC, 32-pin TQFP packages	4Q98
AT90LS2333	AVR	Low-Voltage, AVR RISC, In-System Programmable Microcontroller with 2K bytes FLASH, 128 bytes SRAM, 128 bytes EEPROM, UART, 6 Channel 10-Bit ADC; 28-pin PDIP, 28-pin SOIC, 32-pin TQFP packages	4Q98
AT90S4414	AVR	AVR RISC, In-System Programmable Microcontroller with 4K bytes FLASH, 256 bytes SRAM, 256 bytes EEPROM, UART; 40-pin PDIP, 44-pin PLCC and 44-pin TQFP packages	Now
AT90S4433	AVR	AVR RISC, In-System Programmable Microcontroller with 4K bytes FLASH, 128 bytes SRAM, 256 bytes EEPROM, UART, 6 Channel 10-Bit ADC; 28-pin PDIP, 28-pin SOIC packages. 32-pin TQFP packages	4Q98
AT90LS4433	AVR	Low-Voltage, AVR RISC, In-System Programmable Microcontroller with 4K bytes FLASH, 128 bytes SRAM, 256 bytes EEPROM, UART, 6 Channel 10-Bit ADC; 28-pin PDIP, 28-pin SOIC, 32-pin TQFP packages	4Q98
AT90S4434	AVR	AVR RISC, In-System Programmable Microcontroller with 4K bytes FLASH, 256 bytes SRAM, 256 bytes EEPROM, UART, 8 Channel 10-Bit ADC; 40-pin PDIP, 44-pin PLCC and 44-pin TQFP packages	4Q98
AT90LS4434	AVR	Low-Voltage, AVR RISC, In-System Programmable Microcontroller with 4K bytes FLASH, 256 bytes SRAM, 256 bytes EEPROM, UART, 8 Channel 10-Bit ADC; 40-pin PDIP, 44-pin PLCC, 44-pin TQFP packages	4Q98
AT90S8515	AVR	AVR RISC, In-System Programmable Microcontroller with 8K bytes FLASH, 512 bytes SRAM, 512 bytes EEPROM, UART; 40-pin PDIP, 44-pin PLCC, 44-pin TQFP packages	Now
AT90S8535	AVR	AVR RISC, In-System Programmable Microcontroller with 8K bytes FLASH, 512 bytes SRAM, 512 bytes EEPROM, UART, 8 Channel 10-Bit ADC; 40-pin PDIP, 44-pin PLCC, 44-pin TQFP packages	Now
AT90LS8535	AVR	Low-Voltage, AVR RISC, In-System Programmable Microcontroller with 8K bytes FLASH 512 bytes SRAM, 512 bytes EEPROM, UART, 8 Channel 10-Bit ADC; 40-pin PDIP, 44-pin PLCC, 44-pin TQFP packages	Now

ATmega Series AVR FLASH Microcontrollers

Part Number	Processor	Description	Availability
ATmega603	AVR	AVR RISC, In-System Programmable Microcontroller with 64K bytes FLASH, 4K bytes SRAM, K bytes EEPROM, UART, RTC, 8 Channel, 10-Bit ADC; 64-pin TQFP package	4Q98
ATmega603L	AVR	Low-voltage, AVR RISC, In-System Programmable Microcontroller with 64K bytes FLASH, 4K bytes SRAM, 2K bytes EEPROM, UART, RTC, 8 Channel, 10-Bit ADC; 64-pin TQFP package	4Q98
ATmega103	AVR	AVR RISC, In-System Programmable Microcontroller with 64K bytes FLASH, 4K bytes SRAM, 2K bytes EEPROM, UART, RTC, 8 Channel, 10-Bit ADC; 64-pin TQFP package	Now
ATmega103L	AVR	Low-voltage, AVR RISC, In-System Programmable Microcontroller with 64K bytes FLASH, 4K bytes SRAM, 2K bytes EEPROM, UART, RTC, 8 Channel, 10-Bit ADC; 64-pin TQFP package	Now

AT90/ATmega Series AVR Development Tools

Part Number	Description	Availability
ATMCU00100	AT89S/AT90S FLASH MCU Starter Kit	Now
ATSTK200	Enhanced AT89S/AT90S Flash MCU Starter Kit	Now
ATSTK300	megaAVR Starter kit with Application Builder Software	Now
AT90ICEPRO	In-Circuit Emulation System for AVR AT90S Microcontrollers	Now
ATmegaICE	In-Circuit Emulation System for megaAVR Microcontrollers	Now
ATasicICE	In-Circuit Emulation System for Embedded AVR Core Development	Now
AT90STDPOD	AT90ICEPRO Standard Pod Replacement Kit	Now
AT90ADCPOD	AT90ICEPRO Analog Replacement Kit	Now
ATmegaPOD	ATmegaICE Pod Replacement Kit	Now

Secure ICs for Smart Cards - Memory

Part Number	Memory Size	Description	Availability
AT88SC101	1024 x 1	1K-bit Serial EEPROM with Security, 1 Memory Zone, 1024 Bits	Now
AT88SC102	1024 x 1	1K-bit Serial EEPROM with Security, 2 Memory Zones, 512 Bits Each	Now
AT88SC1003	1024 x 1	1K-bit Serial EEPROM with Security, 3 Memory Zones, 256 + 256 + 512 Bits	1Q99
AT88SC153	192 x 8	1.5K-bit Serial EEPROM with Security and Authentication, 3 Memory Zones, 512 Bits Each	1Q99
AT88SC1601	15,872 x 1	16K-bit Serial EEPROM with Security, 1 Memory Zone, 15,872 Bits	Now
AT88SC1604	15,968 x 1	16K-bit Serial EEPROM with Security, 3 Memory Zones, 4096 Bits Each, and 1 Memory Zone, 3680 Bits	Now
AT88SC1608	2048 x 8	16K-bit Serial EEPROM with Security and Authentication, 8 Memory Zones, 2048 Bits Each, and 1 Configuration Zone, 1024 Bits	Now

Secure ICs for Smart Cards - Microcontrollers

Part Number	Flash	EEPROM	RAM Bytes	T = 0 Hardware	Power Supply	Availability
AT89SC168	16K Bytes	8K Bytes	256 Bytes	Yes	5.0V	Now
AT89SC168A	16K Bytes	8K Bytes	512 Bytes	No	2.7 - 5.5V	Now
AT89SC1616A	16K Bytes	16K Bytes	512 Bytes	No	2.7 - 5.5V	Now
AT89SC248A	24K Bytes	8K Bytes	512 Bytes	No	2.7 - 5.5V	Now

Secure ICs for Smart Cards - Cryptocontrollers

Part Number	Program Memory	User Memory Flash/EEPROM	RAM Bytes	Power Supply	Crypto Engine	RF Interface	Availability
AT90SC1616C	16K Flash	16K Bytes	1K Bytes	2.7 - 5.5V	Yes	No	4Q98
AT90SC3232C	32K Flash	32K Bytes	1K Bytes	2.7 - 5.5V	Yes	No	4Q98
AT90SC3232CR	32K ROM	32K Bytes	1K Bytes	2.7 - 5.5V	Yes	No	4Q98
AT90SC3232CRF	32K ROM	32K Bytes	1K Bytes	2.7 - 5.5V	Yes	Yes	4Q98

Secure ICs for Smart Cards - Contactless (RFID)

Part Number	EEPROM Memory	Features	Availability
AT88RF256	256 x 1	Read/Write RFID Transponder with Passwords and Data Locking	4Q98
AT88RF8714	2K x 8	Contactless Card IC with AVR Microprocessor, 8K Bytes ROM, 256 Bytes SRAM	4Q98
AT24RR08	1K x 8	Dual Access EEPROM: RFID and Serial	Now

Storage Products

Part Number	Description	Package	Availability
Hard Disk Drive			
AT78C1000	Hard Disk Drive Manager (HDDM/Servo System)	128-lead TQFP	Now
AT78C1001 (Core)	HDDM Core	N/A	N/A
AT78C1002	HDDM II (HDDM plus 1M-Bit Flash)	208-lead TQFP	4Q98
Digital Video Drive			
AT78C1501	DVD-RAM Interface Controller Ultra DMA 33MB/s	144-lead TQFP	1Q99
AT78C1502	DVD-RAM Servo Controller	128-lead TQFP	4Q98
AT78C1503	DVD-RAM Read Channel 160M-Bits	64-lead TQFP	4Q98
AT78C1504	DVD-RAM Laser Power Controller	48-lead TQFP	4Q98
AT78C1505	DVD-RAM Read Pre-Amp	48-lead TQFP	4Q98
High Capacity Floppy			
AT78C1201	Full Custom Mixed Signal + Flash	128-lead TFP	1Q99